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Microelectronic Design of Pulse Discriminator Circuits for the LHCb Detector

Corrected version

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Disseny microelectrònic de circuits discriminadors de polsos pel detector LHCb

Memòria de la tesi presentada per David Gascón Fora per optar al grau de Doctor en Enginyeria Electrònica

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Agraïments

Més enllà d'agrair la col·laboració de la gent que es citarà, el propòsit d'aquestes línies es reconèixer la seva participació en la tasca que aquí es presenta. En primer lloc al Sebastià i al Lluís, directors de la tesi, que han tingut la paciència de llegir-se-la. Agraïment que faig extensiu a tots els que també ho facin, i que redoblaré si, a més, em fan arribar els seus comentaris.

El treball relacionat amb aquesta tesi s'ha dut a terme en el si del grup experimental de física d'altes energies que va crear en Lluís al departament d'Estructura i Constituents de la Matèria de la UB.

En el disseny que presentem han participat en Sebastià Bota i l'Àngel Diéguez, quan ambdós estaven al Departament d'Electrònica de la UB. I en les discussions sobre el circuit molta més gent, pertanyents a l'experiment LHCb en la major part, com a mínim: en Jacques Lefrançois, l'Alex Hrisoho i en Dominique Breton del LAL (Paris); en Jacques Lecoq, en Pascal Perret, en Gerard Bohner, en Remi Cornat i en Cyrill Trouilleau del LPC (Clermont-Ferrand); l'Andreas Schopper i en Jorgen Christiansen del CERN (Ginebra), en Xavier Vilasís, na Mar Rosselló i en Jordi Riera d'Enginyeria La Salle (Barcelona) i en Lluís Garrido, en Ricardo Graciani, l'Atilà Herms i en Santi Marco de la UB.

Molta gent ha participat en les proves del circuit: l'Albert Comerma, l'Eduard Picatoste, en Rafael Ballabriga, en Xavier Xirgu, en Sebastià Tortella, en Jordi Riera, la Sònia Luengo, l'Alvaro Gaspar, en Carlos Abellan i segur que alguns més. Els estudis relatius a la caracterització dels efectes de la radiació els van dur a terme principalment en Xavier Cano i en Ricardo Graciani. I molts han aportat dades de mesures i simulacions Monte Carlo que han servit per fixar les especificacions: en Dani Peralta, l'Ernest Aguilò, la Míriam Calvo, en Jordi Garra i en Stephane Monteil.

Abstract

The aim of this thesis is to present a solution for implementing the front end system of the Scintillator Pad Detector (SPD) of the calorimeter system of the LHCb experiment that will start in 2008 at the Large Hadron Collider (LHC) at CERN. The requirements of this specific system are discussed and an integrated solution is presented, both at system and circuit level. We also report some methodological achievements. In first place, a method to study the PSRR (and any transfer function) in fully differential circuits taking into account the effect of parameter mismatch is proposed. Concerning noise analysis, a method to study time variant circuits in the frequency domain is presented and justified. This would open the possibility to study the effect of *1/f* noise in time variants circuits. In addition, it will be shown that the architecture developed for this system is a general solution for front ends in high luminosity experiments that must be operated with no dead time and must be robust against ballistic deficit.

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Resum

1 Introducció

En aquesta tesi es descriu el procés de disseny, fabricació i caracterització d'un circuit integrat d'aplicació específica (ASIC) que forma part de LHCb, un dels experiments del Large Hadron Collider (LHC) del CERN. Més concretament, l'ASIC que hem dissenyat és l'encarregat de realitzar la lectura d'un mòdul del detector LHCb anomenat "Scintillator Pad Detector" (SPD). En primer lloc, descriurem el detector LHCb i especialment el subsistema del que l'esmentat circuit ha de realitzar la lectura. Farem èmfasi en les característiques del senyal i del mateix detector que condicionaran el disseny del circuit. En el segon apartat descriurem el circuit a nivell de blocs i després passarem a presentar els blocs a nivell de transistor. En el tercer apartat presentarem les mesures més rellevants per caracteritzar el circuit. Finalment, conclourem resumint els assoliments més importants de la tesi i apuntant possibles línies de continuació del treball.

L'experiment LHCb (Figura 1, veure [1],[2],[3]) està dissenyat per a estudiar la violació de *CP* a les desintegracions rares en el sistema de mesons B en col·lisions protó-protó al futur accelerador LHC, amb una energia del centre de masses de *14* TeV i una freqüència d'interaccions de *40* MHz. Amb una secció eficaç de producció de $b\bar{b}$ de *0,5* mb i una lluminositat instantània de $\mathcal{L}=2\cdot10^{32}$ cm^{-2}s^{-1}, s'espera de l'ordre d'un bilió de successos amb producció de $b\bar{b}$ per any. LHCb només cobreix un petit rang angular a un costat del punt d'interacció, això hauria de ser suficient per detectar la majoria de partícules provinents de la meitat de les parelles de mesons B creats (cap aquell costat).

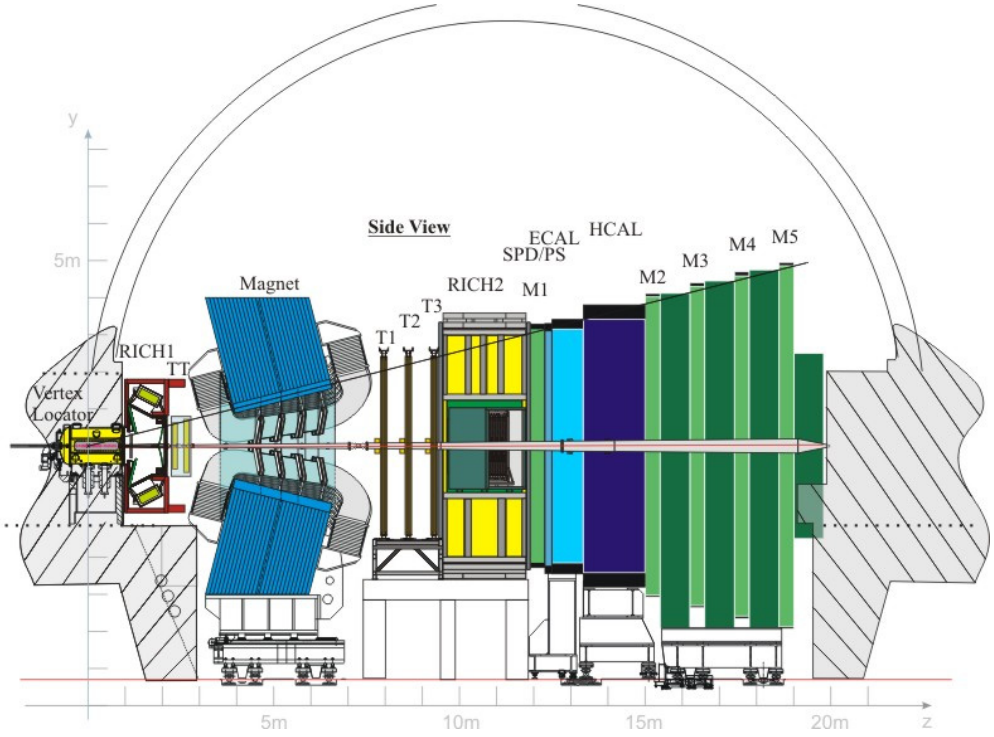

Figura 1. Diagrama del detector LHCb.

LHCb consta de:

- VELO (Vertex Locator), que localitza els vèrtexs i en separa els vèrtexs secundaris (de desintegracions de B's) dels primaris (de la col·lisió). Consta de 21 mòduls disposats longitudinalment al voltant del punt d'interacció que mesuren les coordenades polars de les partícules que les travessen.
- RICHs (Ring Imaging Cherenkov detectors), que s'encarreguen d'identificar partícules carregades, principalment de la separació de pions i kaons, mesurant l'angle Cherenkov (angle entre els fotons emesos i la mateixa partícula) quan passen per gasos de diferents índex de refracció. N'hi ha dos, un després del VELO per partícules de baixa energia i un altre després del sistema de reconstrucció de trajectòries per les d'alta energia.
- Sistema de reconstrucció de trajectòries, que mesura la direcció de les traces de les partícules carregades i n'extreu el moment lineal a partir de la seva curvatura deguda al camp magnètic produït per l'imant, que proporciona un camp integrat de *4* T·m. Consta del seleccionador de trajectòries disparador ("trigger tracker", TT) abans de l'imant i de tres mòduls després, compostos d'una part interior (``inner tracker", IT) i d'una exterior ("outer tracker", OT).
- Els calorímetres, situats després del segon RICH, mesuren l'energia de les partícules a partir de les cascades electromagnètiques i hadròniques que aquestes hi produeixen. Consta de quatre elements: el scintillator pad detector (SPD), el preshower (PRS), el calorímetre electromagnètic (ECAL) i el calorímetre hadrònic (HCAL). Per mesurar la posició de les cascades electromagnètiques i hadròniques, els calorímetres han d'estar dividits en cel·les en el pla transversal a la direcció del feix de protons: SPD, PRS i ECAL estan dividits en tres zones on les mides de les cel·les són de 4x4 cm^2 (zona interior), 6x6 cm^2 (zona mitja) i 12x12 cm^2 (zona exterior), mentre que HCAL només està dividit en dues zones amb cel·les de 13x13 cm^2 (interior) i 26x26 cm^2 (exterior).
- Les cambres de muons (M1-M5) estan situades, M1 entre el segon RICH i el calorímetre, i les altres després del calorímetre. S'utilitzen per identificar els muons, que són les úniques partícules que tenen una alta probabilitat de travessar-les totes (aquesta probabilitat és propera a 1 per muons de més de 8 GeV).

Les col·lisions amb producció de mesons B es poden distingir d'altres col·lisions inelàstiques protó-protó per l'existència de vèrtexs secundaris i l'alt moment transvers dels productes de les desintegracions. Malgrat això, les desintegracions interessants des del punt de vista físic succeeixen amb una probabilitat molt petita comparada amb la resta de desintegracions de mesons B. Per tant, el sistema de disparador (o trigger) s'encarrega de seleccionar amb la màxima eficiència les col·lisions amb successos interessants. Consta de dos nivells:

- Nivell zero (L0): completament implementat a l'electrònica de l'experiment degut a l'alta velocitat de procés requerida (latència inferior a 4 μs) que selecciona successos amb electrons, fotons, muons i hadrons d'alt moment transvers i rebutja successos amb interaccions múltiples (més d'un vèrtex primari). Redueix el ritme d'arribada de dades de 40 MHz a 1 MHz.
- Alt nivell (HLT): confirma les decisions del L0 amb la informació dels mòduls de reconstrucció de trajectòries i aplica algoritmes de selecció de canals de desintegració particulars. Redueix el ritme d'adquisició de dades de 40 kHz a uns 10 Hz per canal (2 kHz finals incloent-hi altres successos). Els algoritmes del HLT, seran implementats a un grup d'unes 1800 CPUs.

Per a la identificació de partícules carregades, cada subdetector proporciona un nivell de versemblança (likelihood: $\mathcal{L}$) per a cada hipòtesi de partícula: el RICH (K, π, e, μ), els calorímetres (e, no-e) i les cambres de muons (μ, no-μ). Aquestes versemblances són combinades per estimar la identitat de les partícules.

Els fotons i els pions neutres, que tenen una vida mitja molt curta i es desintegren a la regió d'interacció, principalment a dos fotons, són identificats a partir de la informació dels calorímetres.

El sistema de calorimetria ([134], Figura 2) de LHCb està dividit en 4 elements: el calorímetre hadronic (HCAL), el calorímetre electromagnètic (ECAL), el "Preshower" (PS) i el SPD. A la Figura 2 podem veure imatges dels diferents elements del sistema. Els calorímetres de LHCb proporcionen candidats a hadrons, electrons i fotons d'altes energies al primer nivell del sistema disparador ("L0 trigger").

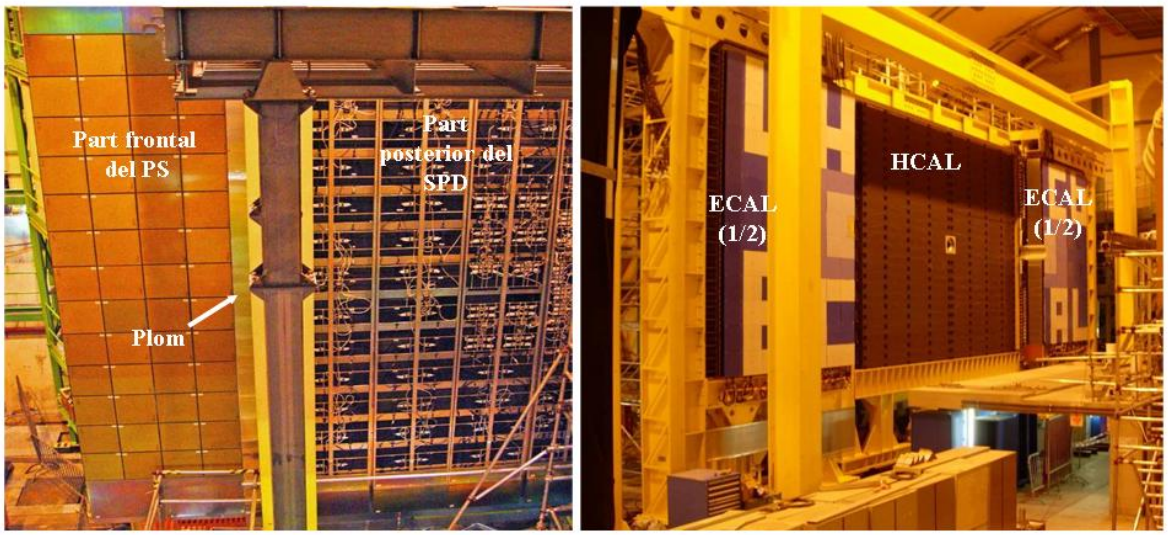

Figura 2. Imatges del sistema de calorimetria de LHCb. Esquerra: PS i SPD. Dreta: ECAL (obert) i HCAL abans de la instal·lació del PS i el SPD.

El SPD està dissenyat per a distingir els candidats a electrons dels candidats a fotons en el nivell L0 del disparador. És un detector amb sortida binaria. Tant el SPD com el PS estan situats abans de l'ECAL i estan separats per un capa de plom de 1,4 cm de gruix. Ambdós estan formats per una capa de cel·les de material escintil·lador plàstic (Bicron BC-408) amb fibra del tipus WLS (wavelength shifting) enrotllada en el seu interior per recollir la llum emesa pel material escintil·lador quan una partícula carregada el travessa. La Figura 3 mostra una cel·la i un mòdul amb 16 cel·les, utilitzat per agrupar-les i facilitar la seva instal·lació. El PS i el SPD estan dividits cadascun en unes 6000 cel·les de diferent mida per obtenir major resolució a prop del feix i uniformitzar l'ocupància. Les partícules carregades ionitzen l'escintil·lador, mentre que les neutres no. Aquesta ionització produeix un pols de llum, part del qual és recollit per la fibra WLS enrotllada a l'interior de l'escintil·lador. La llum és transmesa a l'electrònica de lectura del SPD mitjançant una fibra clara.

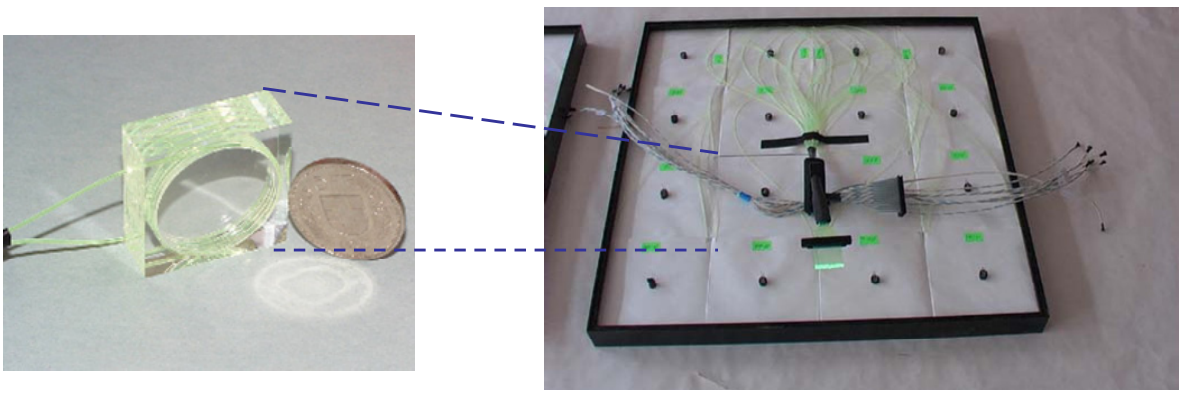

Figura 3. Cel·la escintiladora amb fibra WLS (esquerra) i mòdul amb 16 cel·les (dreta).

La Figura 4 mostra l'esquema de l'electrònica de lectura del SPD. El senyal lluminós dels escintil·ladors és processat en uns mòduls electrònics anomenats "Very Front End" (VFE). Els elements principals del VFE són: un tub fotomultiplicador ("photomultiplier" PMT) per convertir el pols de llum en un pols de corrent, l'electrònica analògica per discriminar el senyals de partícules carregades del de les neutres, un receptor del rellotge que dóna la sincronia amb les col·lisions, una unitat de control i un serialitzador per transmetre la informació binària a les targes que combinen la informació del SPD amb la del PS. Cada mòdul de VFE processa el senyal de 64 cel·les. Per reduir el cost per canal s'empra un PMT multi-ànode (MaPMT) de 64 canals, el R7600-M64 de Hamamatsu [135].

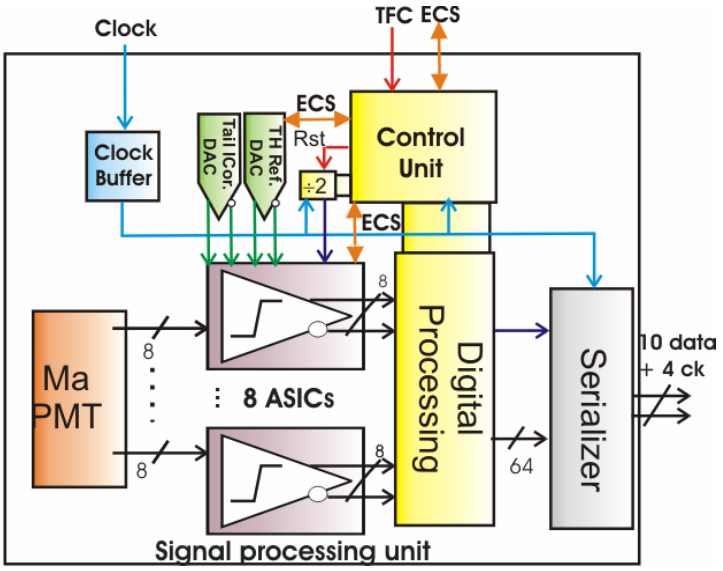

Figura 4. Diagrama de blocs de l'electrònica de lectura del SPD.

Cada mòdul de VFE està format per tres plaques: una amb el MaPMT, una altra amb la circuiteria analògica i una tercera amb la unitat de control, els serialitzadors i els connectors; veure la Figura 5. Gràcies a l'alt guany que pot proporcionar el MaPMT és habitual transmetre el seu senyal a zones allunyades del detector, on es processat. En aquest cas es va decidir fer el processat analògic dels senyals del MaPMT en el mateix detector per maximitzar la relació senyal-soroll (veurem que en aquesta aplicació el guany del PMT està limitat pel seu envelliment) i per simplificar les connexions mitjançant transmissió digital multiplexada en el temps.

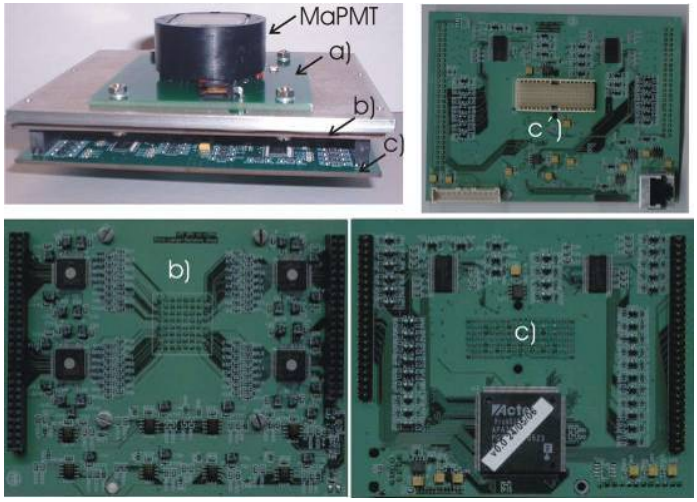

Figura 5. Unitat de VFE a) Placa amb el MaPMT, b) placa amb la circuiteria analògica i c) placa amb la unitat de control (c' és la vista de l'altra cara de c).

El processament analògic de les senyals del fotomultiplicador es realitza mitjançant circuits integrats d'aplicació específica (ASICs), del disseny dels quals tracta aquesta tesi. S'empren dos convertidors digital-analògics (DAC) externs per proporcionar els senyals de referència que requereixen els ASICs. La unitat de control, el processat digital i la divisió del rellotge de col·lisions per obtenir el rellotge de 20 MHz que empren els ASICs s'implementen mitjançant un dispositiu lògic programable, la FPGA ProAsic Plus APA 300 d'Actel. El processat digital consisteix en reordenar els 64 canals de diverses formes per fer coincidir cada canal del SPD amb el seu corresponent del PS i en injectar patrons de test arbitraris per comprovar el flux de dades en el detector.

El R7600 de Hamamatsu presenta importants no-uniformitats en el guany per canal, típicament un factor 2 entre el canal de menys guany i el de més, i pot arribar a un factor 3. Els escintil·ladors i les connexions òptiques presenten també no-uniformitats. El sistema de lectura del SPD ha de ser capaç de tractar aquest problema.

En principi només les partícules carregades haurien de generar senyal. El senyal corresponent a l'energia típica que diposita una partícula carregada mínimament ionitzant[a] s'anomena en anglès "Minimum Ionizing Particle" (MIP). Tanmateix, els fotons d'altes energies poden crear electrons mitjançant processos com l'efecte Compton o la creació de parells. Aquests fenòmens produeixen un espectre d'energia per les partícules neutres que té un màxim al zero però amb una petita cua a altes energies, veure la Figura 6, on 1 MIP correspon a 2,85 MeV aproximadament. Aquest fet provoca errors d'identificació en prendre fotons com a electrons, tal i com es va mesurar en un feix de proves de l'accelerador SPS del CERN ([136] i [137]). Aplicar un tall entre 0,3 i 0,75 MIPs és un bon compromís per filtrar al màxim el senyal dels fotons, tot minimitzant la pèrdua d'eficiència en la detecció de partícules carregades. Per tant, l'electrònica ha de ser capaç de realitzar amb la màxima precisió possible aquest tall, tenint en compte fins i tot les no-uniformitats del detector.

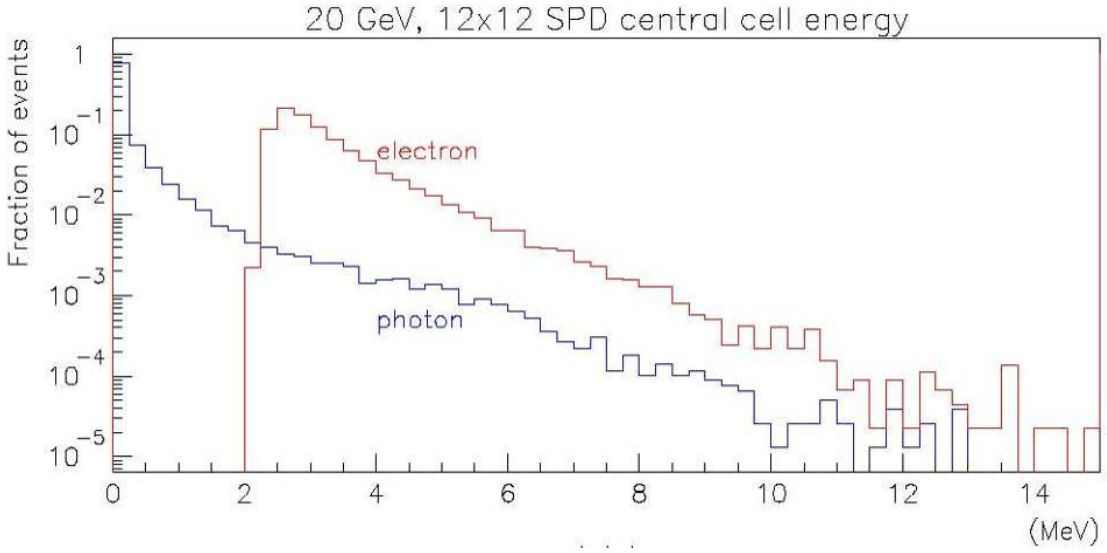

Figura 6. Espectre de l'energia dipositada en una cel·la central del SPD per electrons i fotons.

Només s'obtenen 25 fotoelectrons per MIP en promig. Aquesta baixa foto-estadística i l'efecte del mecanisme d'excitació-desexitació de la fibra WLS, que té una resposta exponencial amb una constant de temps d'uns 12 ns, provoquen que el pols de llum tingui una forma irregular on les fluctuacions estadístiques són apreciables, tal i com es pot observar a la Figura 7.

[a] L'energia que diposita una partícula en el medi depén dels seu moment. Un MIP és una particula que té el moment on es produeix la mínima ionització.

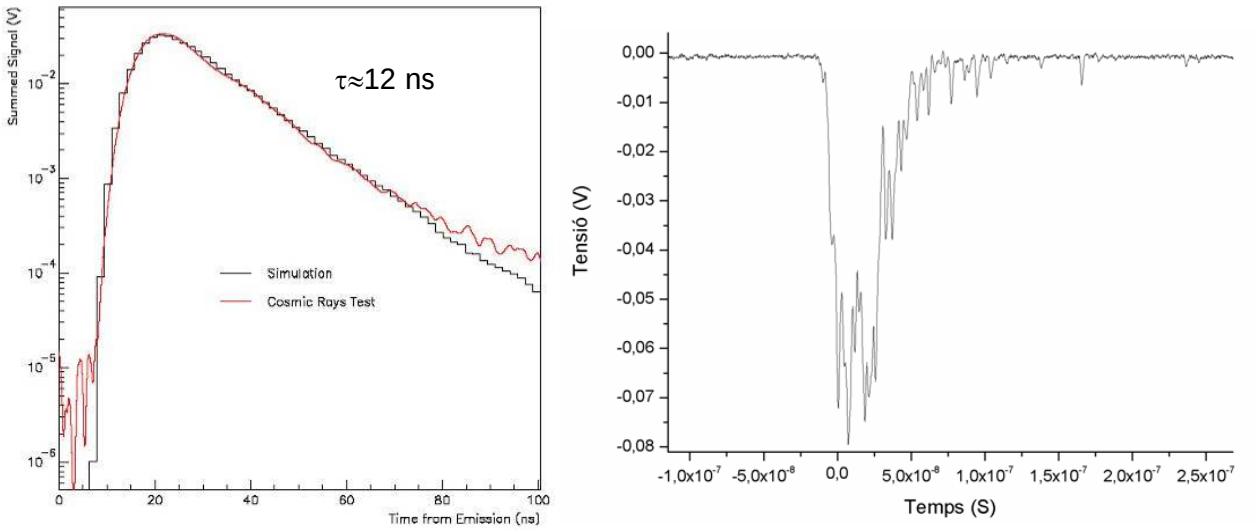

Figura 7. Forma del senyal de MIP: promig (esquerra) vers un esdeveniment aïllat (dreta).

La "lenta" resposta de la fibra també fa que el senyal es prolongui més enllà dels 25 ns, que és el període entre creuament de feixos a LHC. Aproximadament el 80 % del senyal està en el primer període. Això vol dir que l'electrònica de lectura haurà d'estar preparada per corregir problemes d'apilament: la cua d'un senyal de gran amplitud (>3 MIPs) o la suma amb el fons de fotons podria superar el llindar de discriminació i provocar un fals dispar en l'esdeveniment posterior. Aquest fet és coneix com a apilament de polsos.

Tot i que els PMTs poden treballar a guanys de 10^6 i fins i tot 10^7, l'elevada ocupància del detector fa que s'hagi d'operar a un guany de $3 \cdot 10^4$. Altrament l'elevat corrent anòdic faria envellir el PMT ràpidament ([139], [140]). La conseqüència és que el senyal per MIP serà només d'uns 100fC. Perquè el soroll electrònic no degradi la resolució del sistema, aquest haurà de ser molt inferior a les fluctuacions estadístiques del senyal del PMT. Es pot demostrar que el soroll electrònic ha de ser inferior a 2 fC r.m.s., és a dir a una càrrega equivalent de soroll de 12500 electrons, obligant a optimitzar i estudiar acuradament el soroll introduït per l'electrònica de lectura malgrat treballar amb un fotosensor de guany potencialment elevat com és el PMT.

2 Disseny del circuit

La Figura 8 mostra l'arquitectura proposada per dur a terme el processat analògic del senyal. Es tracta d'una configuració basada en dos subcanals per tal d'evitar introduir temps morts i per poder corregir els efectes d'apilament del senyal. El senyal del PMT, després d'ésser amplificat, és integrat mitjançant un integrador commutat durant el màxim de temps possible per maximitzar el senyal i minimitzar l'efecte de les fluctuacions estadístiques en la seva forma. Aquest temps màxim és el període entre col·lisions donat que volem discernir a quina col·lisió pertany el senyal. L'integrador necessita un cert temps de restauració per descarregar els condensadors d'integració i si no disposéssim de dos subcanals funcionant alternadament el sistema tindria un cert temps mort mentre es realitza aquesta descàrrega. Hi ha altres mètodes per descarregar l'integrador sense introduir temps morts [148], aquests estan basats, però, en línies de retard i per raons d'àrea aquesta solució es va descartar.

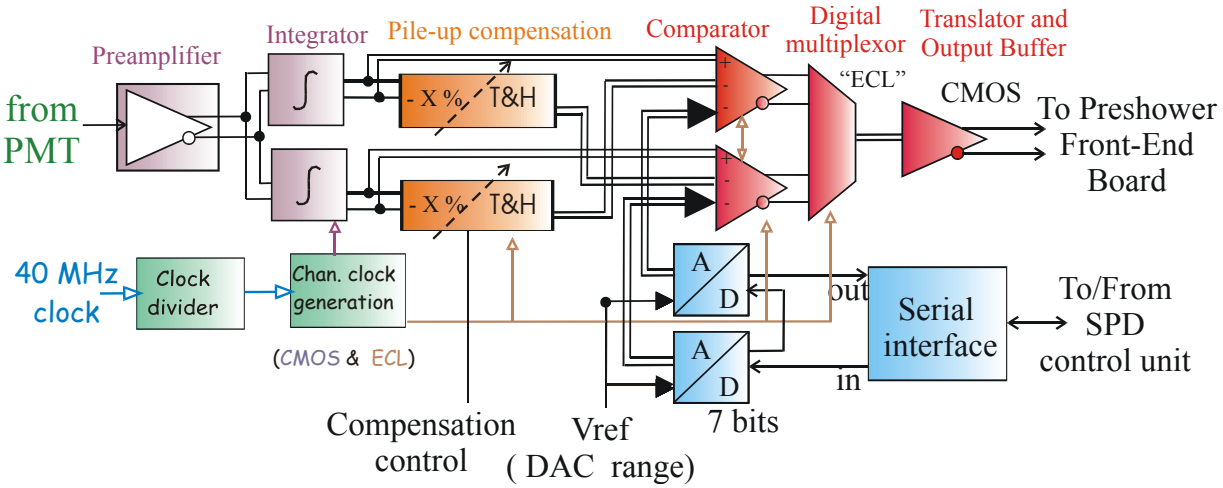

Figura 8. Diagrama de blocs d'un canal del sistema de processat analògic.

La freqüència del rellotge de col·lisions es divideix per dos i el rellotge resultant s'empra per multiplexar per nivell els dos subcanals cada 25 ns. Per prevenir la possible diafonia que poden provocar els senyals digitals de variació ràpida en els senyals analògics dels blocs de major sensibilitat, la majoria dels circuits són diferencials. Aquesta solució també minimitza l'efecte de la injecció de càrrega en els interruptors analògics. El major inconvenient d'emprar circuits diferencials rau en el fet que l'àrea i el consum pràcticament es dupliquen.

La Figura 9 mostra el funcionament del circuit. Malgrat que el senyal del PMT és unipolar, el primer bloc del circuit l'amplifica i la converteix en diferencial. Mentre un integrador està en fase de descàrrega, l'altre integra la sortida del preamplificador durant 25 ns, la seva sortida és corregida (efecte d'apilament) i comparada amb un nivell llindar programat a través d'un DAC. El resultat de la comparació es mostreja just abans de la fi del període d'integració. El sistema de correcció d'apilament o correcció de la cua pren una fracció del senyal a la sortida de l'integrador (la fracció del senyal que es trobaria en el següent període si el senyal no tingués fluctuacions estadístiques i seguís la forma mitja presentada en la Figura 7) i l'emmagatzema en un circuit de mostreig i manteniment. La fracció del senyal que es pren es pot ajustar mitjançant un senyal de control analògic per poder corregir diferències en la resposta temporal degut a diferències en la mida de la cel·la, en la longitud de les fibres o als efectes de la radiació.

El valor de llindar es programa mitjançant un DAC de 7 bits. Cada subcanal empra un DAC independent per poder compensar diferències en l'òfset de cada subcanal. És un conversor multiplicador que empra una tensió de referència que proporciona un DAC extern. Això permet variar el fons d'escala del nivell llindar i calibrar i testejar tot el rang d'operació intern del circuit. Els DACs interns es programen mitjançant una interfície sèrie per tal de minimitzar el nombre de pins del chip.

Els elements de memòria de la part digital empren mecanismes de redundància per prevenir canvis en el seu contingut degut a la radiació (*Single Event Upsets SEU*). En la part analògica, especialment allà on s'empren transistors MOS, s'han fet servir tècniques de disseny com per exemple anells de guarda per prevenir possibles curtcircuits en les alimentacions degut a l'activació de transistors paràsits per la radiació (*Single Event Latchup SEL*).

El consum de potència en sistemes on la densitat d'electrònica és bastant alta acostuma a ser un altre aspecte a tenir en compte. En aquest cas després d'estudiar la disposició dels VFE i els sistemes de refrigeració possibles, es va decidir limitar el consum de cada chip a 500 mW. Per assolir aquest objectiu els blocs analògics i digitals treballen a una tensió d'alimentació de 3,3 V.

Es va escollir la tecnologia BiCMOS de 0,8 μm de Austriamicrosystems perquè els transistors bipolars són adequats per les parts analògiques, per la seva millor relació transconductància vers consum i pel seu millor aparellament respecte als transistors MOS, mentre que els transistors MOS s'empren com elements de commutació analògica i per dissenyar blocs digitals de baix consum.

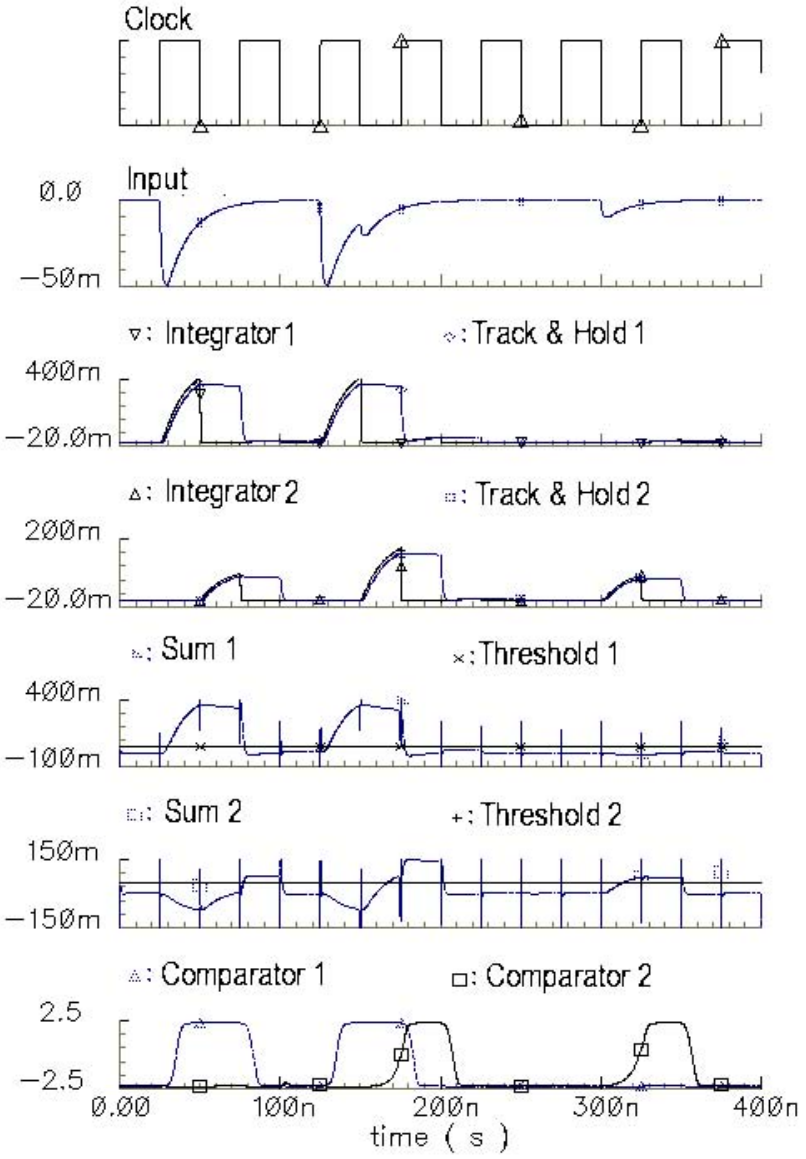

Figura 9. Simulació del funcionament dels dos subcanals.

El pols de corrent a la sortida del PMT, que correspon al senyal mitjà d'un MIP es pot aproximar per un pols de corrent de baixada exponencial amb una constant de temps τ d'uns 12 ns:

$$i_{PMT}(t) = -\frac{Q_{MIP}}{\tau} e^{-\frac{t}{\tau}} u(t) \qquad (1)$$

El pols és negatiu, Q_{MIP} és la càrrega total corresponent a un MIP i *u(t)* és la funció esglaó de Heaviside. Com es mostra a la Figura 10, una resistència de càrrega (R_{PMT}) a l'ànode del MaPMT, transforma el pols de corrent en un pols de tensió que serà processat per l'ASIC. La forma del senyal de voltatge ve determinada també per la capacitat paràsita (C_{stray}) i la capacitat d'entrada del ASIC (C_{in}). La resistència d'entrada del ASIC és molt major que R_{PMT} i, per tant, pot ser menyspreada.

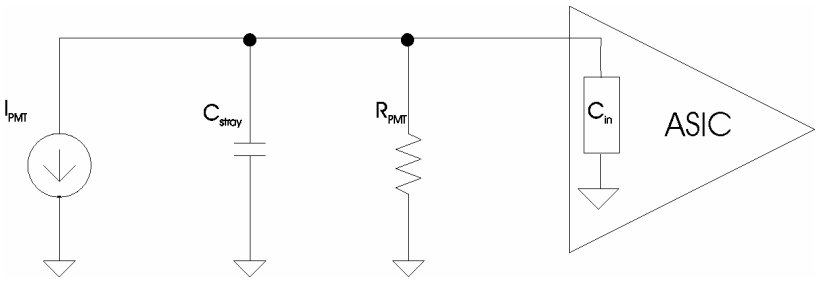

Figura 10. Model circuital de l'ànode del PMT.

Resolent l'equació diferencial corresponent al circuit de la Figura 10 i suposant que la constant de temps τ_C deguda a les capacitats paràsites i a R_{PMT} és molt més petita que τ, el PMT treballa en mode corrent i el senyal a l'entrada del ASIC és

$$v_i(t) \simeq\Big|_{\tau_C \ll \tau} -\frac{Q_{MIP}}{\tau} R_{PMT} e^{-\frac{t}{\tau}} u(t) \qquad (2)$$

Veient l'equació (2) hom podria tenir la temptació d'incrementar arbitràriament el valor de R_{PMT} tan com fos necessari per assolir un nivell de senyal d´1 MIP, fàcilment tractable per l'electrònica[b]. Tanmateix incrementar R_{PMT} comporta un increment de τ_C i si el seu valor comença a ser comparable a 12 nanosegonsel PMT deixa d'operar en mode corrent. Això vol dir que $v_i(t)$ ja no es pot aproximar per (2) i que la fracció de senyal que es troba dins el període d'integració comença a disminuir i les cues del senyal a augmentar. Considerant un capacitat parasita total d'uns 10 pF, el límit aproximat per R_{PMT} és de 500 Ω.

La Figura 11 mostra l'esquema del preamplificador, que és bàsicament un parell diferencial bipolar amb degeneració d'emissor i carrega passiva. El guany del circuit s'ha ajustat a 4,6 i ve donat aproximadament per la raó de la resistència de col·lector vers la resistència d'emissor. La linealitat de l'etapa és prou bona pel marge de senyals a processar sense que calgui cap compensació addicional. El circuit té sortida diferencial, a cada sortida s'empra un seguidor d'emissor per obtenir baixa impedància de sortida i minimitzar els efectes de la càrrega en les prestacions del circuit. L'ample de banda del circuit és d'uns 200 MHz per capacitats de càrrega inferiors a 1 pF, d'acord amb simulacions "post-layout" del circuit. S'ha dissenyat per assolir un ample de banda d'integració major que l'ample de banda del senyal del fotomultiplicador, que és d'uns 100 MHz. El coeficient de temperatura (CT) del bloc és inferior al 0,1 %/K, gràcies a la cancel·lació dels CTs de les resistències de col·lector i d'emissor, ja que ambdues estan fetes amb el mateix tipus de poli-sil·lici. Aquest tipus d'etapa diferencial s'ha emprat també en altres blocs de l´ASIC, ja que permet assolir gran ample de banda, impedància d'entrada alta, baix CT, evita problemes d'inestabilitat en treballar en bucle obert i l'àrea ocupada és relativament petita.

[b] Un estudi acurat del soroll del circuit mostra que el soroll també és proporcional a R_{PMT}, però creix molt més lentament que el senyal. Parlant en termes de relació senyal-soroll, també seria positiu maximitzar R_{PMT}.

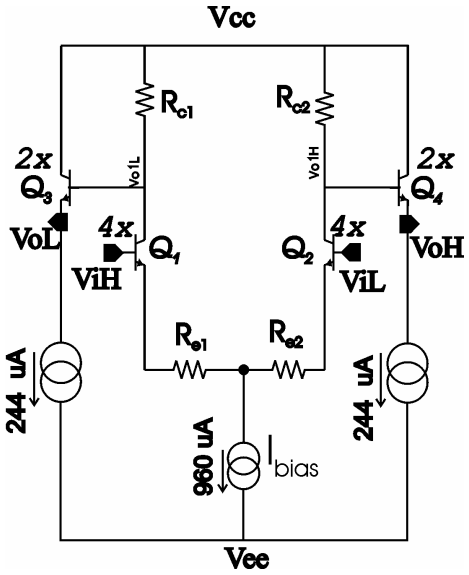

Figura 11. Esquema del preamplificador.

L'esquema de l'integrador es mostra a la Figura 12. L'etapa d'entrada, que és també un parell diferencial bipolar amb degeneració d'emissor (R_E), actua com a transconductor convertint el voltatge d'entrada ($v_{iD}=v_{iH}-v_{iL}$) en corrent (I_{oD}), ambdós diferencials. Aquest corrent és integrat per un amplificador d'entrada i sortida diferencials amb realimentació capacitiva (C_1 - C_2). Els interruptors s'implementen com un interruptor clàssic CMOS i permeten descarregar les capacitats d'integració C en el període que marca el rellotge de cada subcanal.

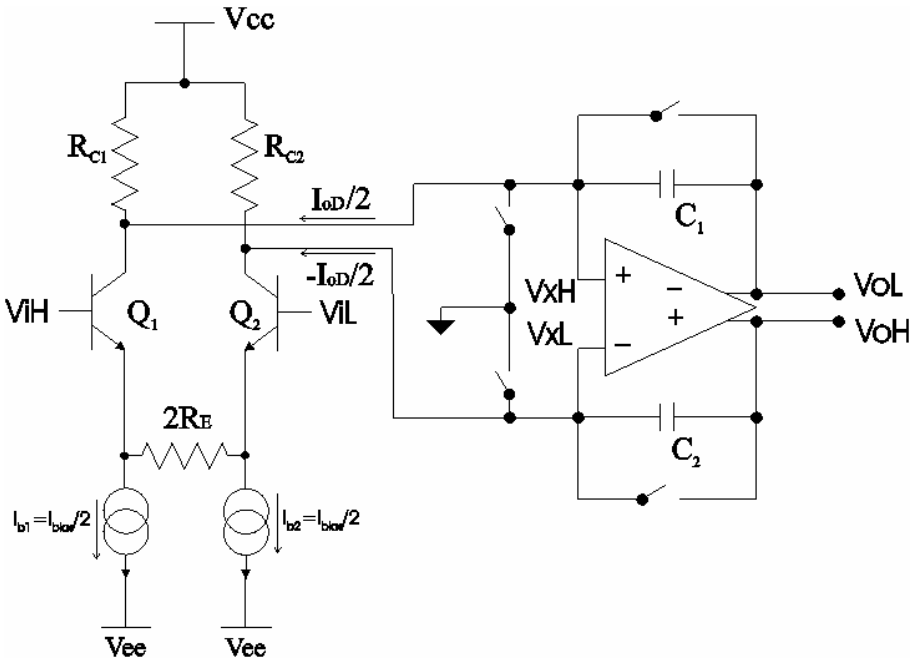

Figura 12. Esquema de l'integrador

Per senyals d'alta freqüència, com els polsos del PMT, pràcticament tot el corrent del parell diferencial circula pels condensadors de realimentació i no per les resistències de col·lector del parell diferencial. La tensió en els borns d'un condensador és proporcional a l'integral del corrent; com aquest corrent es proporcional al senyal d'entrada i com podem aplicar curtcircuit virtual entre els terminals de

l'amplificador operacional, aleshores la tensió de sortida serà proporcional a la integral de la d'entrada. Aquesta descripció qualitativa del funcionament del circuit es veu reflectida en la resposta freqüencial del circuit que es mostra a la Figura 13. La constant de temps del circuit ve donada pel producte R_EC.

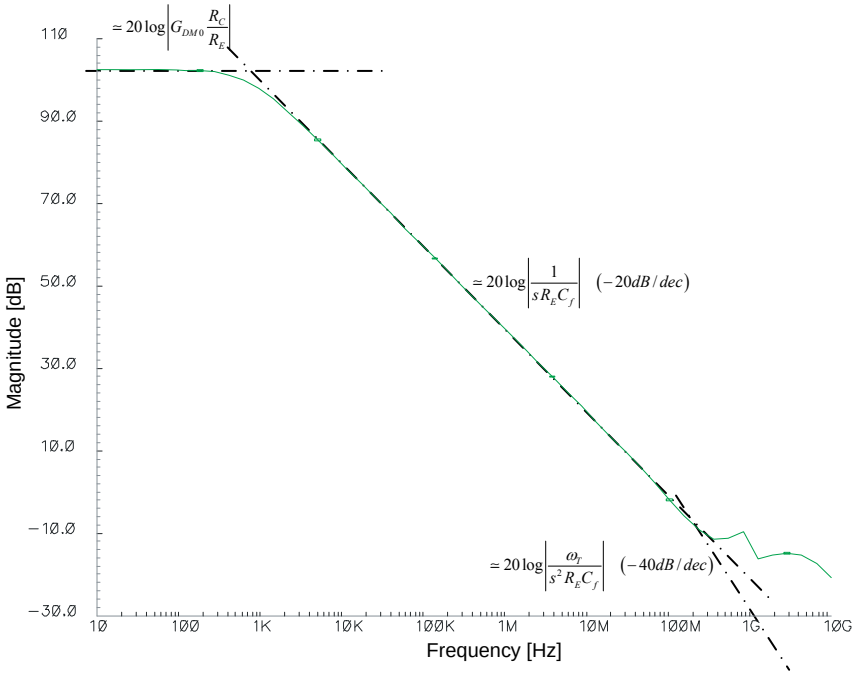

Figura 13. Simulació de la resposta en freqüència de l'integrador.

L'ample de banda de l'amplificador operacional introdueix un pol a uns 200 MHz, tal i com es pot apreciar a la Figura 13. Aquest pol es correspon amb la freqüència de guany unitari de l'amplificador operacional, essent un requeriment de disseny assolir un ample de banda d'integració de 200 MHz, major que l'ample de banda dels senyals d'entrada. La Figura 14 mostra el resultat d'una simulació "post-layout" de l'amplificador operacional. S'ha assolit l'ample de banda desitjat i el marge de fase és de 70º, prou alt per garantir l'estabilitat del circuit. El guany de baixa freqüència és de 90 dB, més que suficient perquè els errors deguts a la no idealitat de la realimentació siguin menyspreables. L'amplificador operacional empra un circuit de realimentació del mode comú per fixar el punt de treball adequadament. S'empra un amplificador d'error per controlar acuradament el mode comú de la sortida.

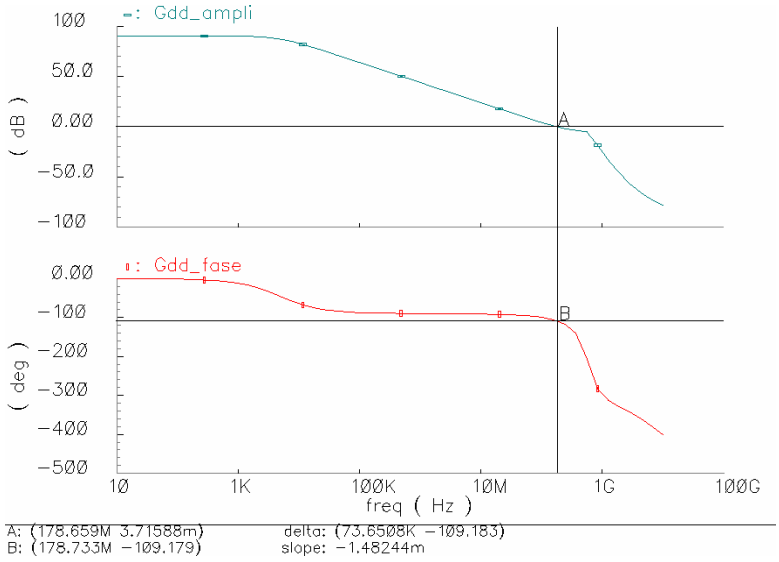

Figura 14. Resposta en freqüència de l'amplificador operacional: mòdul (dalt) i fase (baix).

El diagrama de blocs del sistema de correcció d'apilament es mostra a la Figura 15. Els blocs anomenats "Voltage Buffer" dupliquen el senyal diferencial d'entrada tot introduint un desplaçament en el mode comú de les dues rèpliques. Aleshores, un transconductor CMOS ("Cross coupled transconductor"), la transconductància del qual és funció d'aquesta diferència en el mode comú, permet ajustar la fracció de senyal que s'emmagatzema en la següent etapa: un circuit de seguiment i manteniment ("Track & Hold").

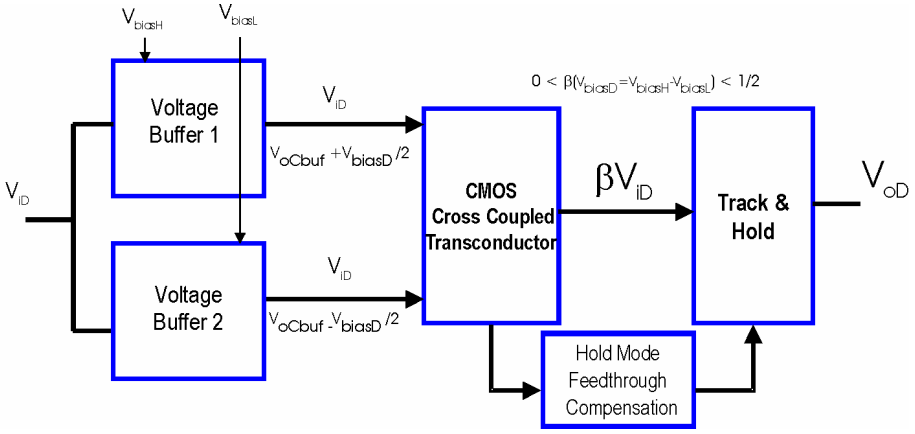

Figura 15. Diagrama de blocs del circuit de correcció de la cua del senyal.

Els dos blocs "voltage buffer" estan formats bàsicament per un parell diferencial amb degeneració d'emissor i inclouen compensació de linealitat. L'esquema de la resta del circuit encarregat de la correcció dels efectes de cua del senyal es mostra a la Figura 16. Com s'ha comentat, l'element ajustable és un transconductor MOS (transistor M_{ijj}) de guany controlable per tensió mitjançant l'introducció d'un desplaçament en el nivell de mode comú de cadascuna de les dos entrades diferencials (veure [153]).

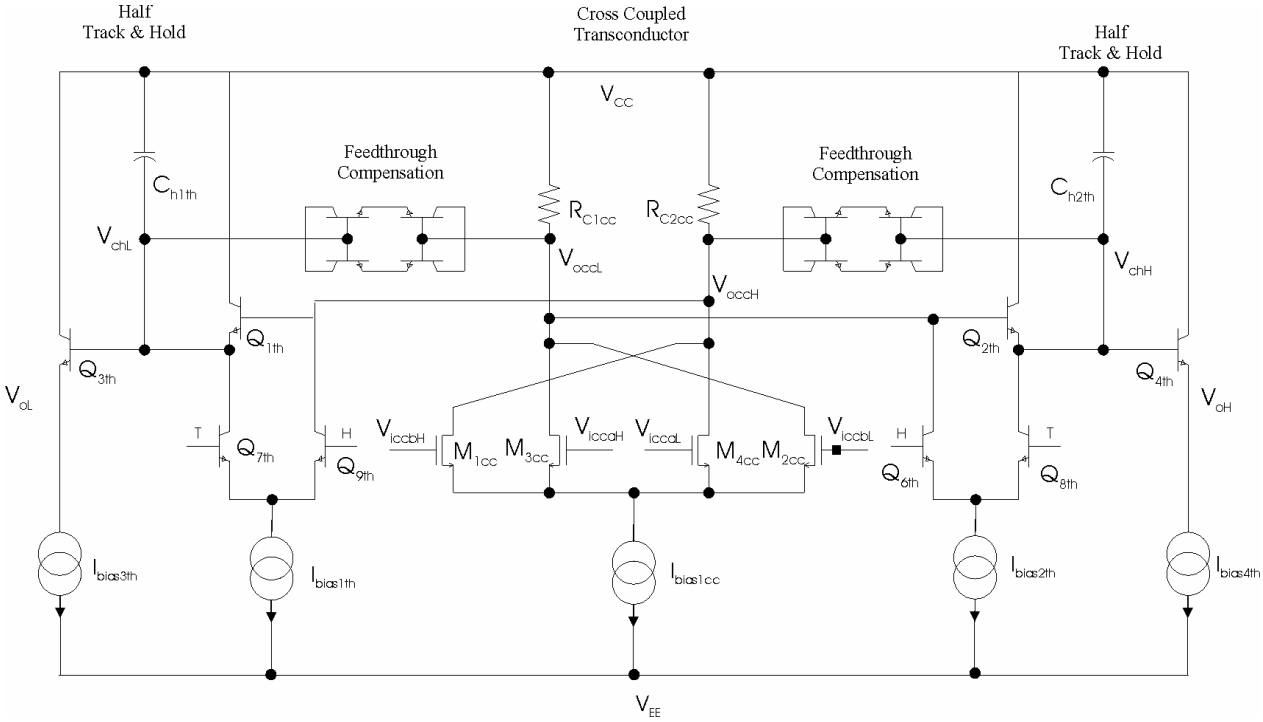

Figura 16. Esquema del transconductor i del circuit de mostreig i manteniment del bloc de correcció de la cua.

El circuit de seguiment i manteniment és una variació d'un conegut circuit diferencial que realitza aquesta funció [156]. La principal diferència rau en que amb una tensió d'alimentació de 3,3 V no es pot fer servir l'etapa d'entrada proposada en [156]. Tot i que existeixen diverses propostes per

solucionar aquest problema ([157] o [158]), en el nostre disseny el transconductor controlable actua també d'etapa d'entrada de circuit de seguiment i manteniment.

Després del transconductor MOS trobem un seguidor d'emissor (Q_{1th} i Q_{2th}), que ataca el condensador de manteniment (C_{h1th} i C_{h2th}). Aquest seguidor es polaritza mitjançant un interruptor diferencial bipolar Q_{6th}-Q_{8th} i Q_{7th}-Q_{9th} controlat per un rellotge diferencial (T-H) que es deriva del rellotge del subcanal (20 MHz). En l'etapa de seguiment (T), la tensió en els nodes v_{chH} i v_{chL} segueix la sortida del transconductor. El condensador de manteniment es va carregant a aquesta tensió. En l'etapa de manteniment (H) l'interruptor deixa de polaritzar el seguidor i els condensadors mantenen aproximadament la tensió emmagatzemada en els nodes v_{chH} i v_{chL}. El temps de manteniment de la tensió en el condensador té un límit, ja que el corrent de base del seguidor d'emissor que dóna baixa impedància de sortida al bloc (Q_{3th} i Q_{4th}) contribueix a la seva descàrrega. S'ha minimitzat, però, aquest corrent i segons simulacions la descàrrega del condensador de manteniment és inferior a 2 mV en 25 ns. Les capacitats paràsites dels seguidors (Q_{1th} i Q_{2th}) provoquen una injecció de càrrega directament des de la sortida del transconductor al condensador de manteniment. S'aprofita la simetria del circuit i que els senyals dels dos camins diferencials són perfectament simètrics (sense tenir en compte efectes de desaparellament de dispositius) per compensar aquesta injecció amb una injecció de signe contrari provinent dels blocs anomenats "Feedthrough compensation", que no són més que una unió sèrie-paral·lel de 4 transistors que intenten emular el valor de les capacitats paràsites responsables de la injecció de càrrega.

La Figura 17 il·lustra el comportament del circuit de correcció de la cua. Es pot apreciar la dependència de la sortida del transconductor i de la tensió emmagatzemada en el circuit de mostreig i manteniment amb la tensió de control (V_{subD}), que és la diferència en el mode comú entre les entrades del transconductor.

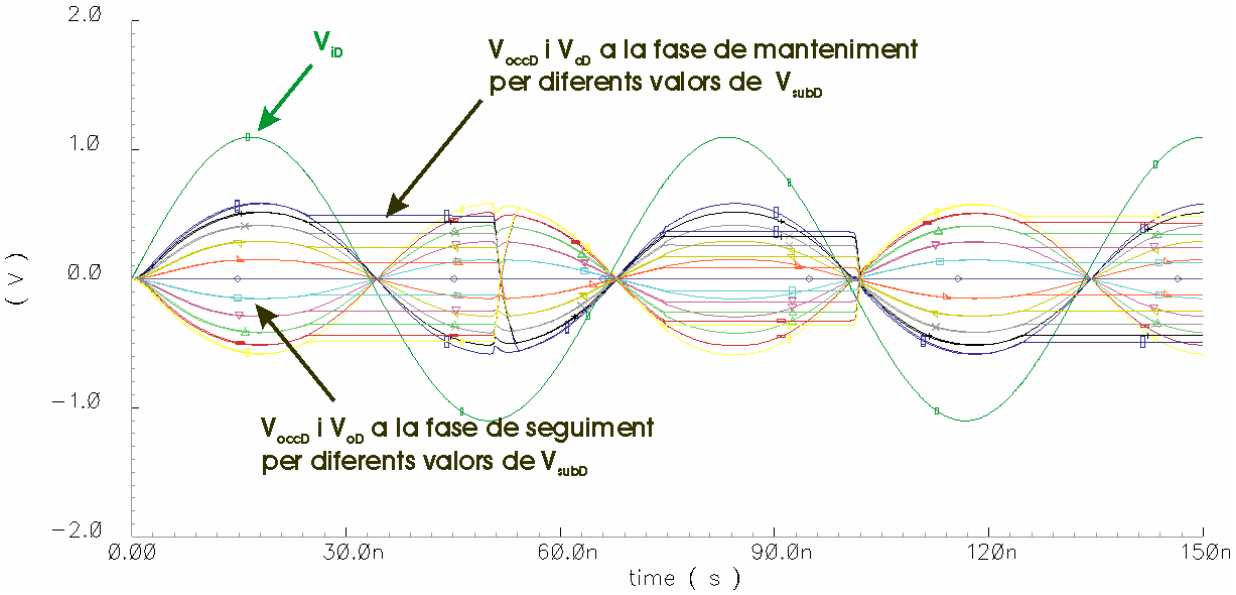

Figura 17. Resultats de la simulació de transitori del bloc de correcció de la cua per una sinusoïdal.

No entrarem en una descripció detallada de la resta de blocs del ASIC, ja que el seu funcionament segueix bastant clarament la funcionalitat indicada i la seva complexitat, a nivell de disseny, no és tan crítica com la dels blocs que hem descrit en detall. A la Figura 18 podem veure una vista general del ASIC de 8 canals, l'àrea ocupada és de 5,254 mm x 5,500 mm (30 mm^2).

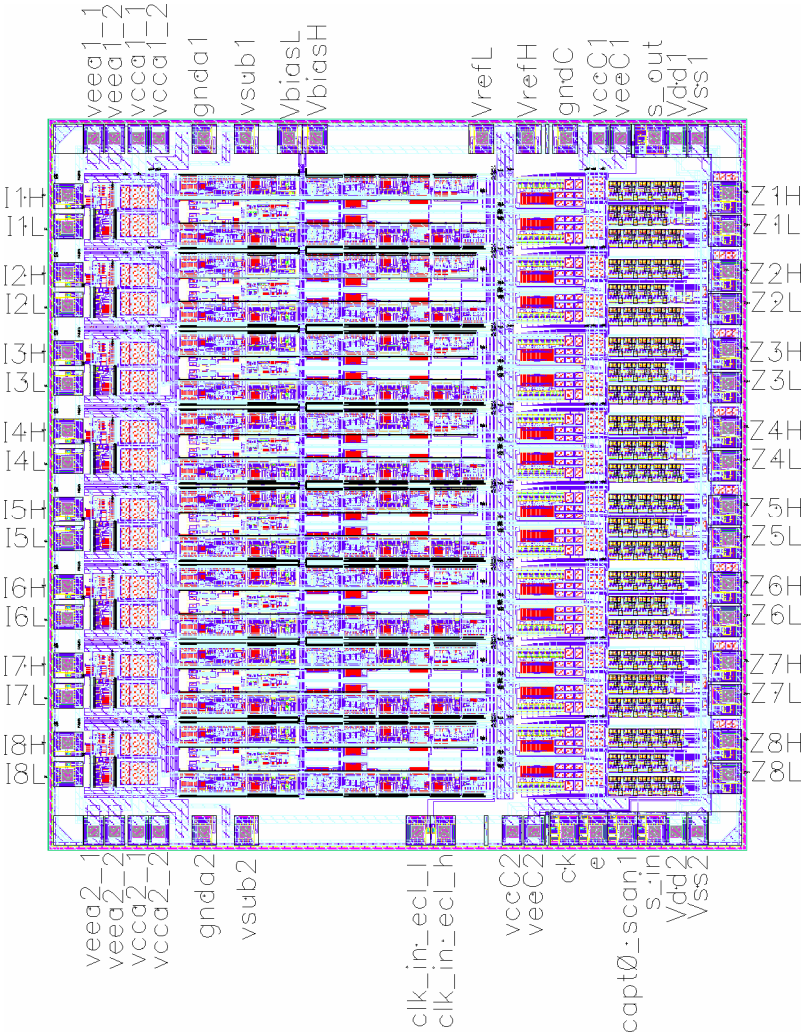

Figura 18. Vista general del "layout" de l'ASIC de 8 canals.

Les alimentacions del circuit integrat es separen en tres grups amb distribució i connexió independents per minimitzar interferències en mode comú:

- Alimentació analògica (*Veea, Vcca)* i massa (*gnda*). El substrat es polaritza mitjançant una connexió dedicada (*Vsub*) per minimitzar la injecció de soroll en el substrat.
- Alimentació digital (*Vdd,Vss*). En aquesta part els contactes al substrat estan connectats a *Vss*.
- Alimentació pels blocs de generació i distribució de rellotges (*VccC, VeeC*) i massa (*gndC*).

Els dos camins de senyal duplicats en un canal, anomenats subcanals, es mostren en la Figura 19. El subcanal comprèn des de l'integrador fins al comparador i el DAC. La interfície digital, el multiplexor, la generació de rellotges i el preamplificador són elements únics. Els detall de la part d'entrada del canal es mostra en la Figura 20.

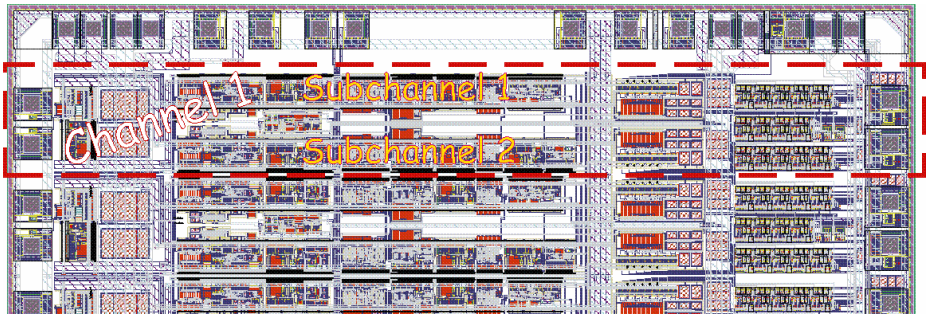

Figura 19. Detall dels subcanals del primer canal del xip.

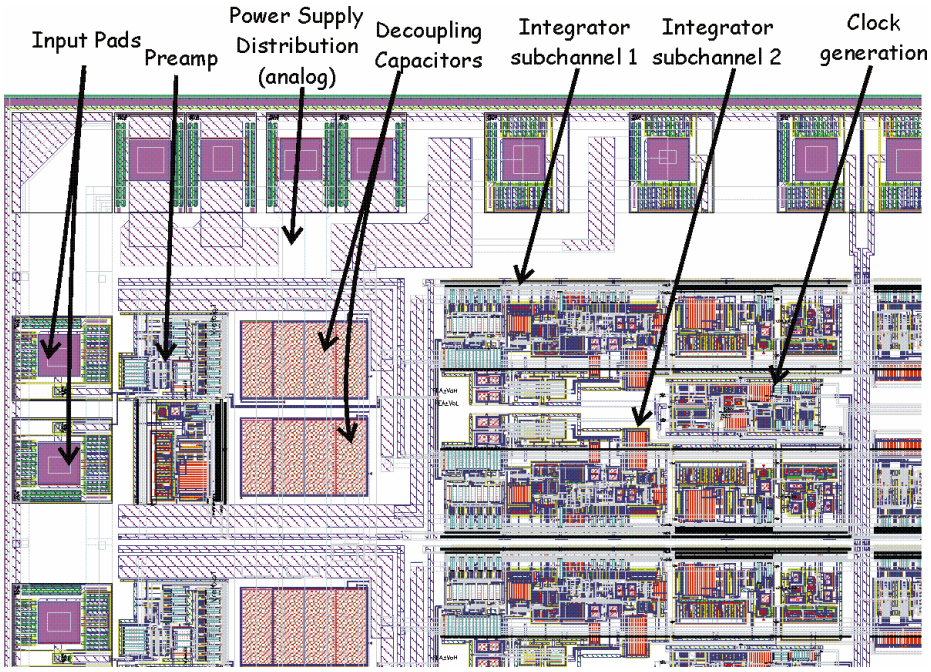

Figura 20. Detall de l'entrada del canal.

3 Resultats

En aquesta secció presentarem mesures tant dels blocs analògics més rellevants com del canal complert, incloent-hi la part digital. Quan en un ASIC s'empren blocs fets a mida que no han estat provats anteriorment, és important caracteritzar cada bloc per separat per ser capaç d'entendre el funcionament del sistema i validar els models i els resultats de les simulacions. És important tenir en compte que els models dels dispositius proporcionats pel fabricant no són completament fiables. Fins i tot suposant els models siguin plenament correctes, les condicions fixades en el banc de proves del simulador poden diferir de les condicions experimentals i la interpretació dels resultats de la simulació pot ser errònia.

Totes les mesures de blocs s'han realitzat en condicions de laboratori, mentre que les mesures de sistema s'han obtingut també utilitzant feixos de partícules en àrees de prova de l'accelerador SPS al CERN.

És també important esmentar que el xip s'ha qualificat per operar en les condicions de radiació esperades de LHCb. Presentarem també un breu resum sobre aquesta tasca.

Els senyals diferencials s'han mesurat utilitzant la sonda diferencial P6146 d'1 GHz d'ample de banda i l'oscil·loscopi d'emmagatzematge digital TDS3034 de 300 MHz d'ample de banda i 2,5 GS/s, els dos de Tektronix. Els senyals d'entrada, els rellotges i els senyals de control han estat generats mitjançant el generador de formes d'ona arbitràries AWG2021 de Tektronix, que pot treballar fins a 250 MS/s. A la Figura 21 veiem una placa de test d'un xip de blocs, amb una sonda diferencial i altres sondes de multímetres.

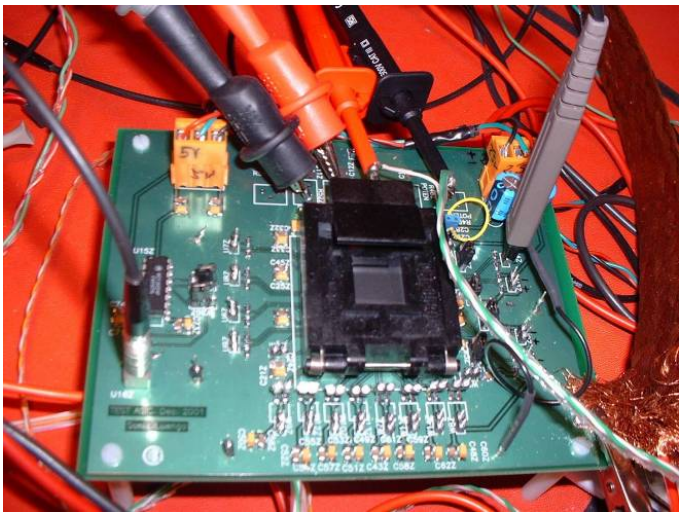

Figura 21. Fotografia d'una placa de test d'un circuit integrat que conté blocs individuals.

L'òfset del preamplificador s'ha mesurat per a 10 circuits, mostrant un valor mitjà de 0,7 mV ± 1.5 mV i una desviació estàndard de 5 mV r.m.s ± 1,2 mV. El guany és 4,35, mentre que segons càlculs i simulacions hauria d'estar al voltant de 4,6. La diferència és provocada per l'amplificador que ataca la sortida del xip (seguidor d'emissor) i que és necessari degut a l'elevat valor de les capacitats paràsites a carregar. L'ample de banda mesurat està per sobre de 100 MHz, però també està limitat per l'amplificador de sortida. L'ample de banda de l'amplificador que ataca la sortida es limita per evitar oscil·lacions. La tolerància relativa en el guany (desviació estàndard) està al voltant d'un 0,9%.

A la Figura 22 veiem la resposta del preamplificador a un senyal sinusoïdal de 10 kHz. La saturació comença a ser evident per a V_{oD}>500mV.

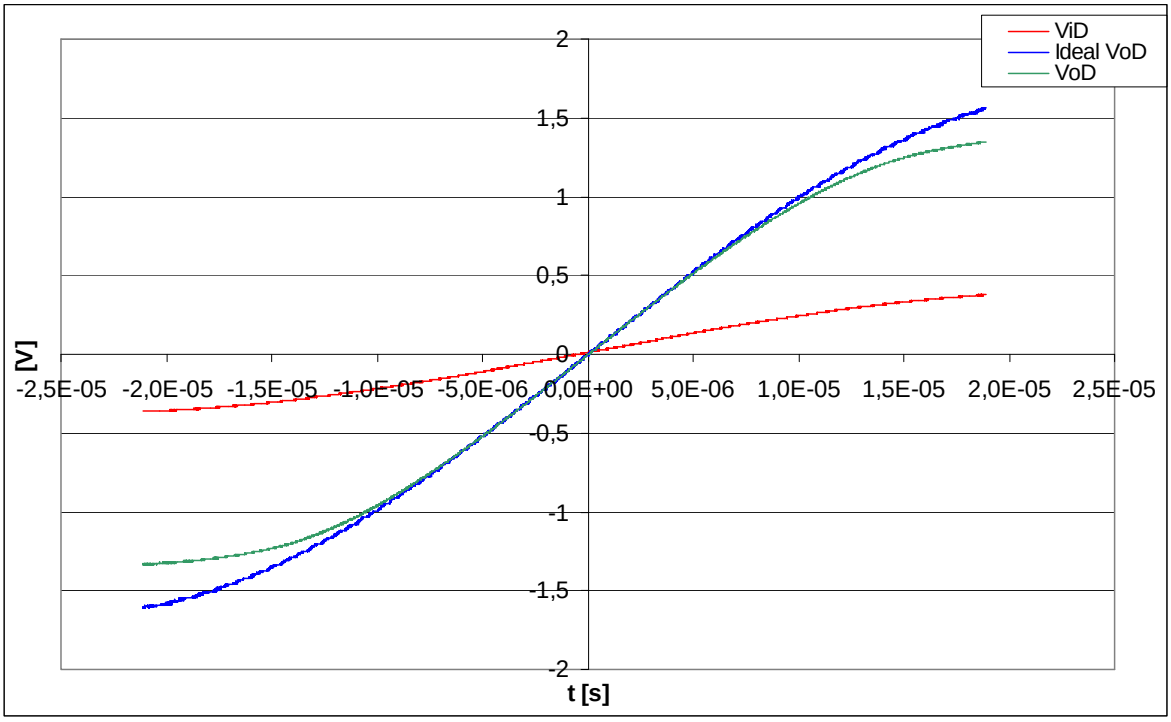

Figura 22. Resposta del preamplificador. V_{iD} és el senyal d'entrada diferencial, V_{oD} és el senyal de sortida diferencial i *Ideal* V_{oD} és el senyal de sortida ($A \cdot V_{iD}$) d'un amplificador perfecte de guany A.

En la Figura 23 podem apreciar la sortida de l'integrador per a un impuls d'entrada típic. Quan el rellotge és en nivell baix, l'integrador és en el mode actiu i quan el rellotge és a nivell alt el condensador de l'integrador es descarrega. El temps per a la reinicialització és menor de 12 nanosegonds per a un senyal d'entrada màxim. Com el temps de baixada del senyal supera dos cicles de rellotge, una part de la cua del senyal s'integra després de la reinicialització.

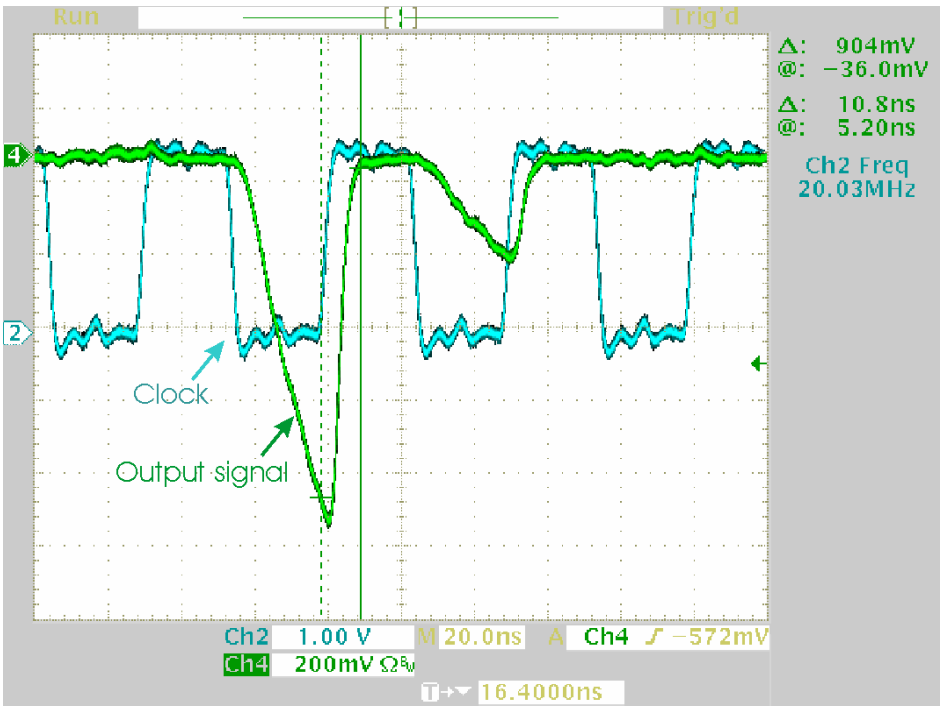

Figura 23. Sortida de l'integrador (verd) i rellotge de control dels interruptors (blau).

El mòdul i la fase de la resposta en freqüència de l'amplificador operacional es mostren a la Figura 24. El producte guany-ample de banda és d'uns 125 MHz, mentre que segons les simulacions fetes tenint en compte les capacitats paràsites de l'amplificador aquest valor hauria d'estar al voltant dels 150 MHz. Si tenim en compte també les capacitats paràsites dels contactes d'entrada, model·lant-les com una capacitat mútua (entre senyals diferencials) d'uns 500 pF, aleshores el resultat de les simulacions és compatible amb les mesures. El rebuig del mode comú (CMRR) és d'uns 70 dB en contínua.

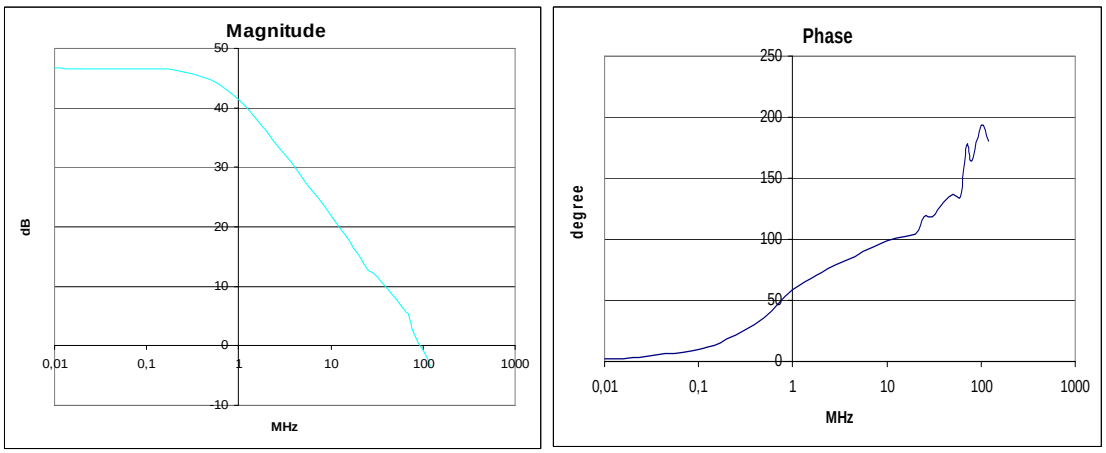

Figura 24. Mòdul (esquerra) i fase (dreta) de la resposta en freqüència de l'amplificador operacional treballant en bucle tancat (guany en DC 220 o 46 dB).

A la Figura 25 veiem els senyals de sortida del bloc de correcció de la cua en mode de seguiment (Track) i en mode de seguiment i manteniment (Track and Hold), per un senyal d'entrada sinusoïdal d'uns 12 MHz i ajustant el guany del transconductor controlable a un 25 %. L'error de linealitat està per sota de 5 mV en una escala de ± 500 mV per qualsevol guany. Per un guany típic de 0,25 o menys, l'error està per sota de 20 mV en l'escala màxima de ± 1 V.

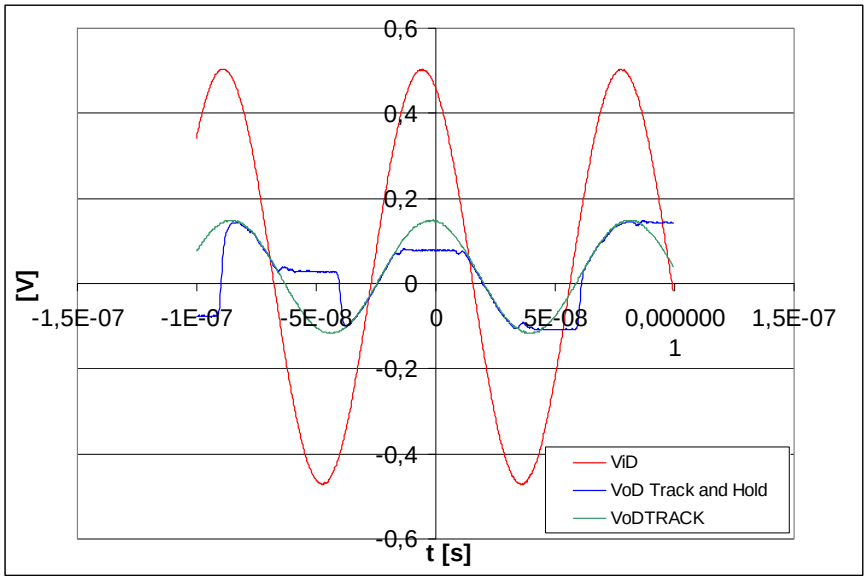

Figura 25. Funcionament del circuit de correcció de la cua.

L'ample de banda del circuit és d'uns 100 MHz, per sota del valor esperat d'acord amb les simulacions (170 MHz), degut probablement a la presència de capacitats paràsites addicionals en l'ASIC pel test de blocs. En qualsevol cas, un ample de banda de 100 MHz és més que suficient una vegada el senyal ja ha estat integrat. Aquesta és l'etapa més crítica en relació a la deriva amb la temperatura. Després d'un ajust acurat dels coeficients en temperatura dels components del bloc, s'ha

aconseguit que el coeficient en temperatura del guany del bloc sigui de -0,29 %/ºC, lleugerament major que el que s'esperaria segons les simulacions (-0,15 %/ºC). Aquest valor és suficientment baix per les variacions de temperatura esperades durant el funcionament, que haurien de ser inferiors a 5º C.

En la Figura 26 veiem una microfotografia del xip complet de 8 canals, l'àrea del qual és d'uns 30 mm^2. L'encapsulat del xip, l'EDQUAD TQFP, té un dissipador de potència connectat al substrat per facilitar el refredament del circuit.

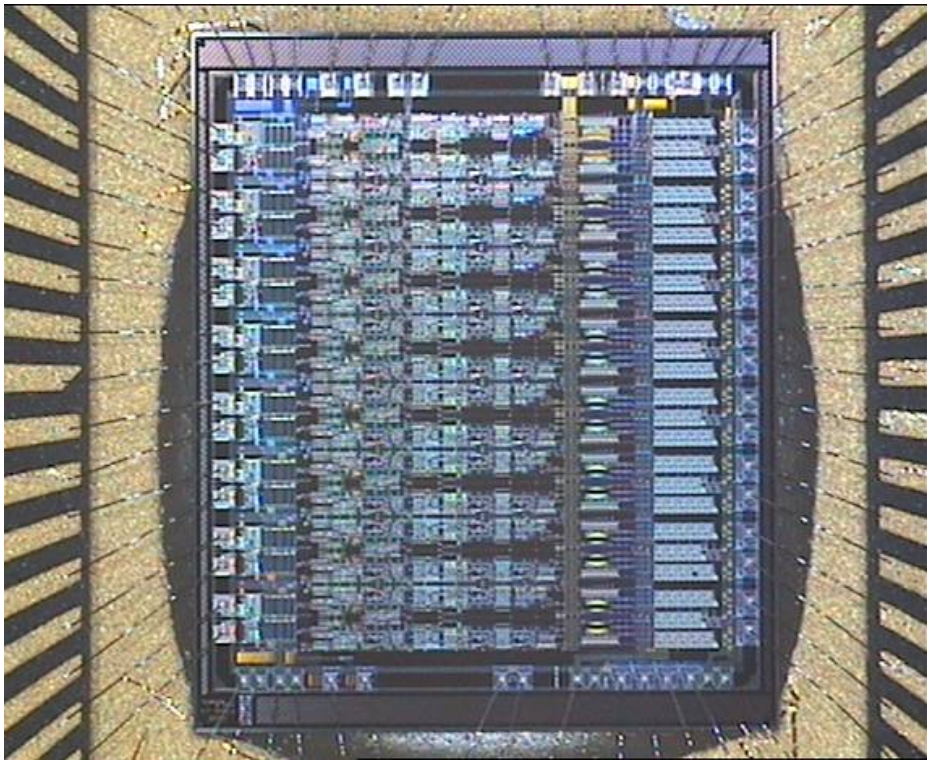

Figura 26. Microfotografia del ASIC de 8 canals.

Per a la caracterització del canal complet s'han utilitzat senyals d'entrada tant elèctrics com òptics (utilitzant un MaPMT com transductor). Els paràmetres més importants per a la caracterització del sistema són:

- Òfset. Es necessita saber l'òfset de cada subcanal per fixar el llindar de discriminació correctament i per controlar que la resolució del sistema està dins les especificacions.
- Soroll. Determina la relació senyal/soroll i la resolució mínima assolible pel sistema.
- Guany. El valor mitjà del guany es necessita per calibrar el sistema, i la seva dispersió ha de ser prou petita.
- Linealitat. L'error de linealitat del canal ha de ser més petit que el del MaPMT.
- Diafonia. La diafonia elèctrica ha de ser més petita que l'òptica.

La Figura 27 mostra l'esquema del sistema de test pels ASICs, que inclou:

- Generació dels senyals de control digital i analògics pels ASICs.
- Recepció i divisió del rellotge de 40 MHz.
- Injecció d'impulsos de càrrega emprant un condensador d'acoblament.
- Adaptació de nivells entre l'ASIC i la circuiteria de lectura.

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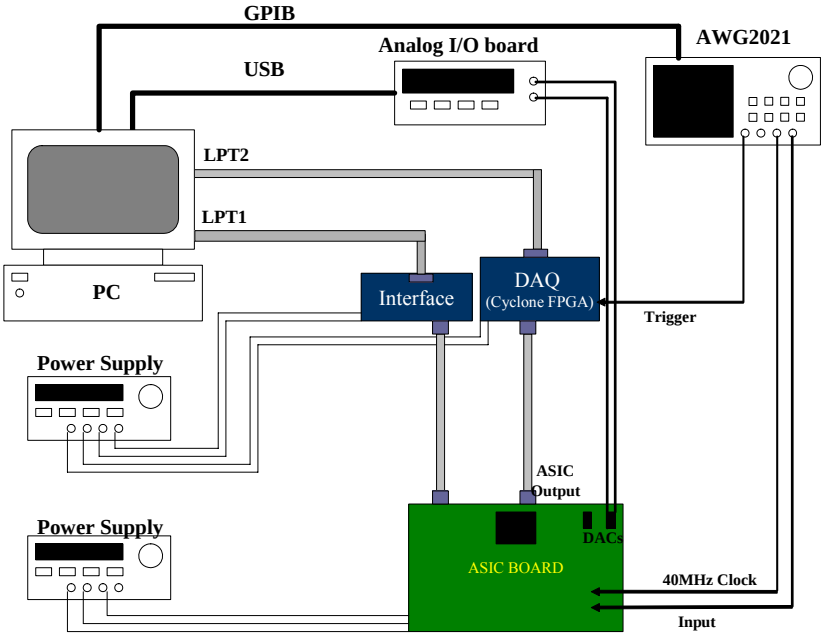

Figura 27. Esquema del sistema de test

El nucli del sistema de lectura és un dispositiu de lògica programable, la FPGA Cyclone d'Altera, que adquireix els senyals de sortida de 4 ASICs, genera els senyals de control digitals dels ASICs i es comunica amb els DACs MAX5822 de Maxim que generen els senyals analògics de referència pels ASICs. Aquest dispositiu es comunica amb un PC a través del bus USB. A la Figura 28 veiem una imatge del sistema de test amb 4 ASICs.

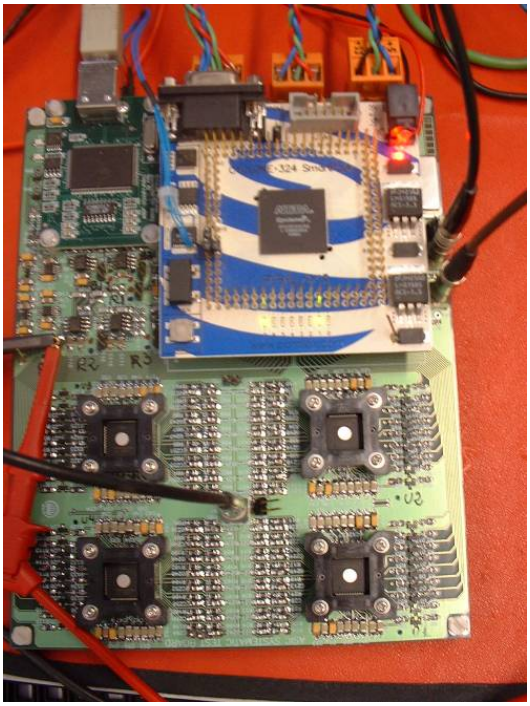

Figura 28. Fotografia del sistema de test dels ASICs.

El generador de formes d'ona arbitràries AWG2021 de Tektronix permet la generació síncrona del rellotge, de l'impuls d'entrada i d'un senyal d'activació del sistema d'adquisició. L'impuls d'entrada és

un senyal graó , que es connecta a l'entrada del ASIC mitjançant un condensador de 1,5 pF. El generador es connecta al PC a través del GPIB de cara a automatitzar el sistema de test.

Com que la sortida del canal és binària, no hi ha cap accés al valor dels senyals analògics previs al comparador. El mètode convencional per mesurar el rendiment de sistemes amb sortida binària consisteix a fer un escombrat del nivell llindar tot injectant un impuls de càrrega conegut a l'amplificador. D'aquesta forma obtenim l'ocupació de la sortida d'un canal com a funció del seu llindar de discriminació; l'anomenada corba S ([177] i [178]). Un exemple de corba S es mostra en Figura 29. Totes les mesures d'òfset, soroll i amb senyal es basen en aquest procediment. L'òfset i el nivell de senyal es dedueixen del valor mitjà de la derivada de la corba S, i el soroll, de la desviació estàndard de la derivada de la corba S.

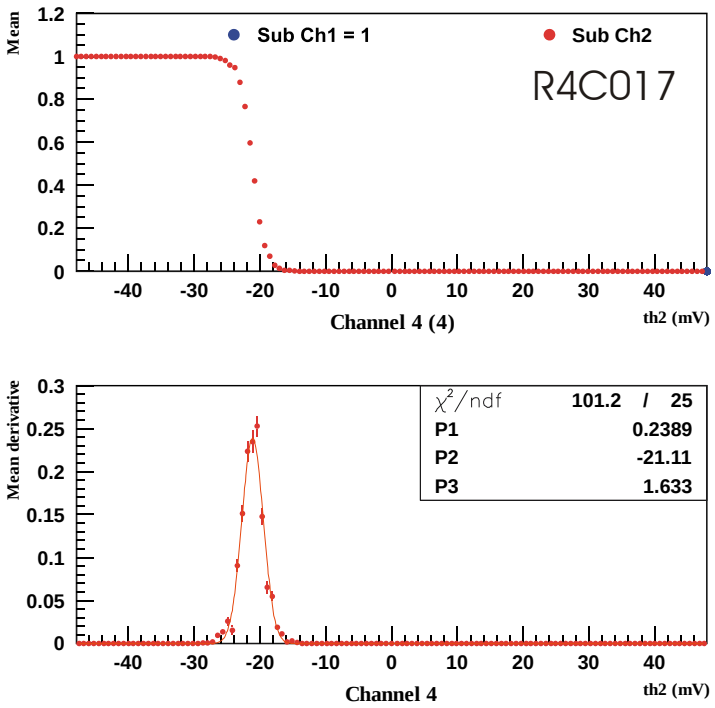

Figura 29. Exemple de corba S obtinguda mitjançant un escombrat de nivell llindar. A dalt: corba S. A baix: derivada de la corba S amb ajust d'una funció Gaussiana.

El valor de l'òfset de cadascun dels 8 canals mesurat en 500 xips es mostra a la Figura 30. El valor promig és d'uns - 65 mV, mentre que segons les simulacions hauria de ser de – 50 mV. Probablement, la diferència és deguda a l'elevat valor d'òfset que s'ha mesurat en l'integrador. Aquest valor està per sobre de les estimacions i del resultat de les simulacions Monte Carlo i probablement és degut a l'acoblament del rellotge per injecció de càrrega en els interruptors de l'integrador. El valor mesurat de la desviació estàndard de l'òfset és de 61 mV, mentre que d'acord a les simulacions Monte Carlo hauria de ser de 55 mV. Aquesta petita diferència pot ser deguda a efectes de segon ordre com gradients en variacions de paràmetres en l'oblea, que no són variacions locals i no es tenen en compte en el simulador. També podrien haver efectes no tinguts en compte a la simulació relacionats amb la correlació de paràmetres dels dispositius actius del preamplificador i de l'integrador.

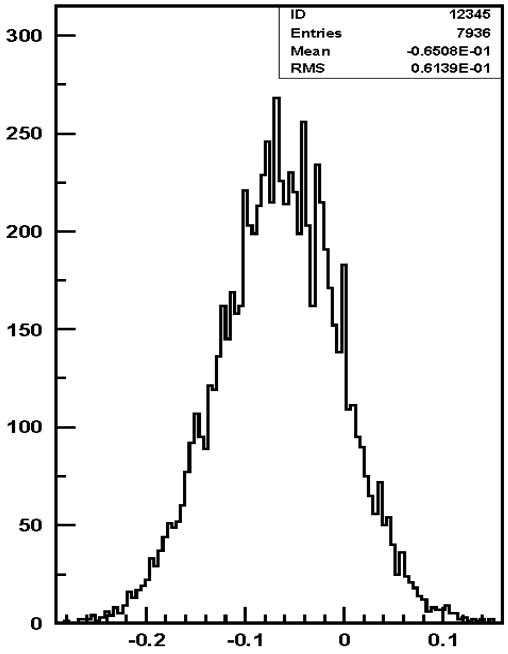

Figura 30. Distribució del valor d'òfset (en mV) per 500 xips i V_{subD}=0.

L'òfset del canal depèn linealment del guany del circuit de correcció de la cua del senyal, i per tant de V_{subD}. En el funcionament normal del circuit aquest guany és negatiu, ja que restem una fracció del cicle *n* al cicle *n+1*, de forma que el bloc de correcció de la cua ajuda a disminuir l'òfset que es veu a l'entrada del comparador, tal i com es pot comprovar a la Figura 31.

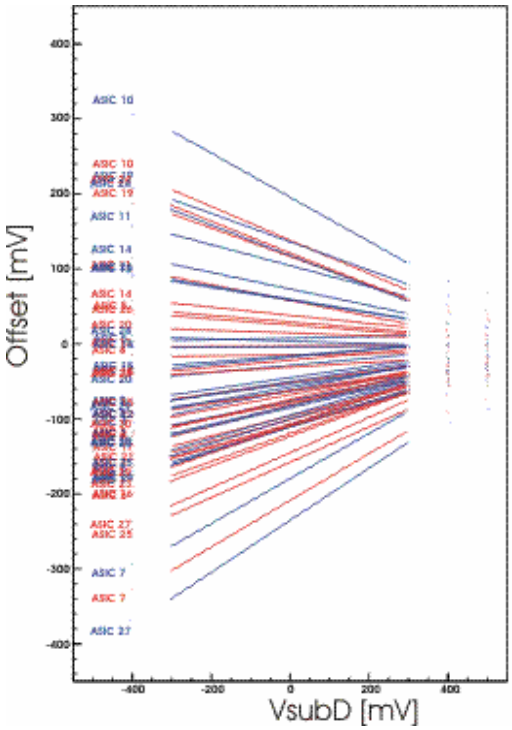

Figura 31. Òfset per 30 canals en funció de V_{subD}.

El soroll promig mesurat en 500 canals és d'uns 2,2 mV r.m.s. per V_{subD}=-200 mV, molt a prop del valor esperat segons els nostres càlculs i les simulacions: 2,3 mV r.m.s. La dependència del valor del soroll amb V_{subD} és molt petita, per sota de 1 mV r.m.s. No han aparegut diferències de soroll

sistemàtiques entre subcanals ni entre canals quan s'ha mesurat el soroll dels ASICs en els VFE. Sí s'han observat diferències sistemàtiques en el soroll mesurat en diferents canals de la placa de test dels ASICs, degut a l'acoblament de soroll en algunes pistes d'entrada en la placa. No s'ha observat un increment apreciable en el soroll quan els VFE s'han instal·lat al detector LHCb, això vol dir que el sistema d'alimentació, de connexió a massa i d'apantallament és eficient. Aquest fet també es pot comprovar en l'estabilitat de l'òfset, a la Figura 32 es mostra la mesura d'aquest valor durant unes 12 hores i veiem que la variació es inferior a 2 mV. Durant els primers 10 minuts (encerclat) es pot apreciar una forta variació de l'òfset del circuit degut al canvi de temperatura (escalfament en alimentar el circuit). No s'ha observat tampoc increment en el soroll en connectar el MaPMT, ni tan sols quan ha estat alimentat a la màxima tensió de funcionament (-800 V).

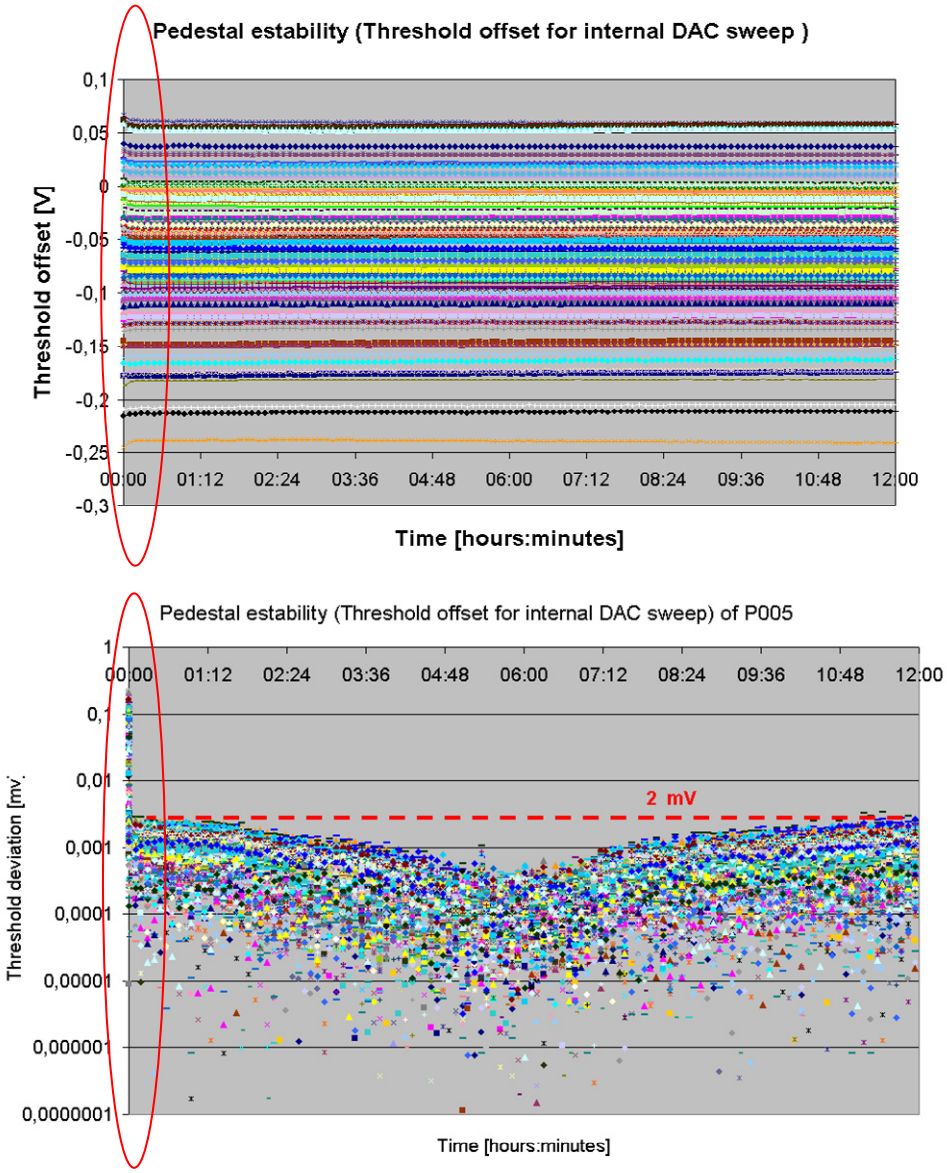

Figura 32. Estabilitat de l'òfset a curt termini. A dalt: òfset. A baix: variació de l'òfset.

A la figura Figura 33 es mostra el senyal promig pels 64 canals d'un VFE en 8 cicles de rellotge consecutius quan s'il·lumina el MaPMT amb un pols de llum produït per un LED que es controla mitjançant un circuit que emula la forma del pols que dóna l'escintil·lador. Veiem senyal en 2 cicles de rellotge, 50 ns, degut a que el sistema de correcció de la cua estava desactivat.

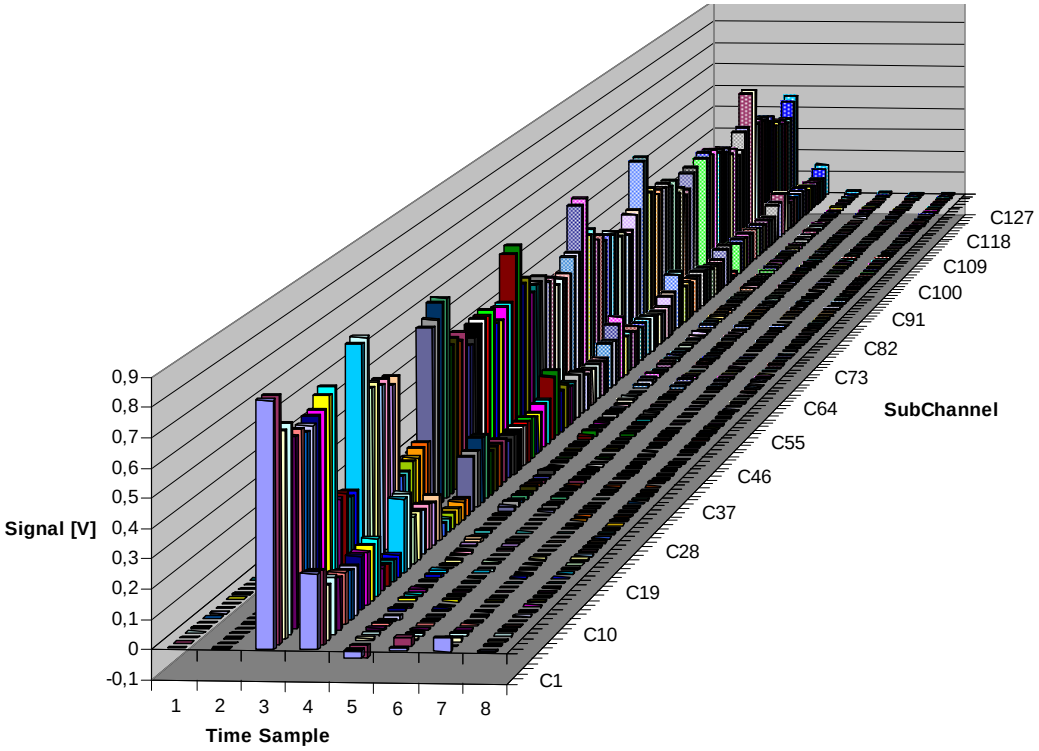

Figura 33. Senyal pels 64 canals d'un VFE en 8 cicles de rellotge consecutius.

A la Figura 34 podem comprovar el funcionament del sistema de correcció de cua. En aquest cas el canal mesurat s'il·lumina amb un fibra connectada a una cel·la escintil·ladora. La cel·la s'irradia amb partícules carregades en un feix de proves de l'accelerador SPS al CERN. Per tant, la forma del senyal s'ha de correspondre al senyal d'1 MIP, o sigui al senyal que es pot esperar en el detector LHCb. Veiem com en promig s'aconsegueix eliminar els efectes de cua del senyal.

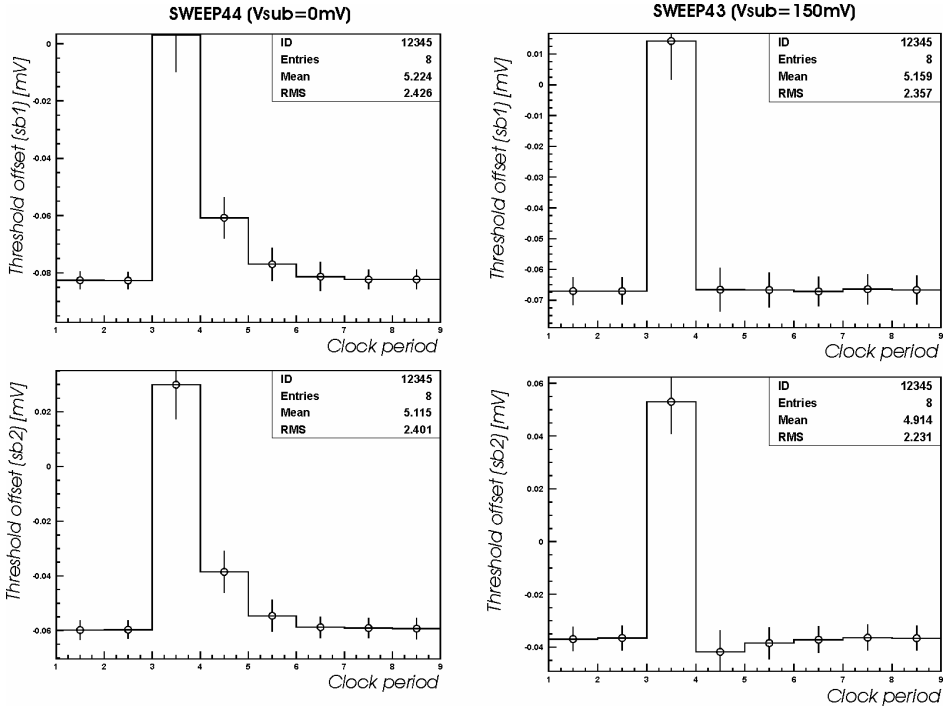

Figura 34. Senyal promig en un canal per 8 cicles de rellotge consecutius sense (esquerra) i amb (dreta) correcció de la cua. Subcanal 1 a dalt i subcanal 2 a baix.

En la mateixa sèrie d'experiments també es va obtenir una mesura de l'espectre del senyal de MIP a partir d'un escombrat del nivell llindar, mostrat a la Figura 35. L'espectre corresponent a un senyal de MIP s'obté a partir de la derivada de la mesura de l'escombrat. Veiem que en aquest cas un MIP correspon a uns 50 mV.

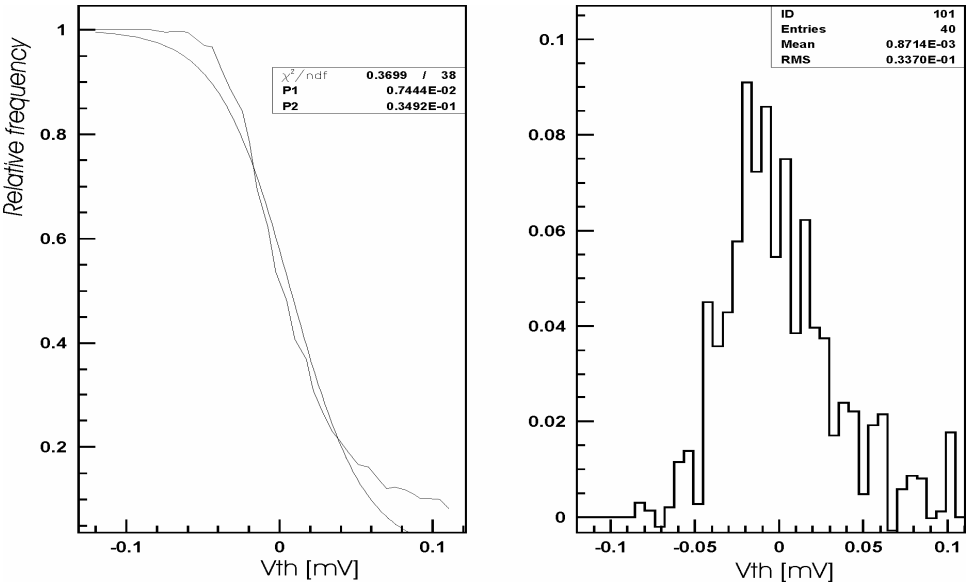

Figura 35. Resultat d'un escombrat de nivell de llindar (esquerra) i espectre del senyal de MIP (dreta).

En un nou experiment, hem fet servir un sistema de dispar extern per activar l'adquisició de manera que hem pogut estudiar l'eficiència de dispar del VFE i l'ASIC respecte aquest sistema. El sistema de dispar consisteix en un escintil·lador acoblat a un fotomultiplicador mitjançant una guia de llum d'alta eficiència. Com que la quantitat de llum que arriba al fotomultiplicador del sistema de dispar és molt gran i aquest treballa a alt guany, el senyal de dispar té una gran eficiència. A la Figura 36 veiem com el nivell llindar haurà d'estar comprès entre els 0,4 i 0,7 MIPs, per obtenir una eficiència de dispar superior al 90 % i mantenir propera a 0 la fracció de falsos dispars provocats pel soroll electrònic, per l'efecte de la cua del senyal o per senyals de fons (fotons o diafonia).

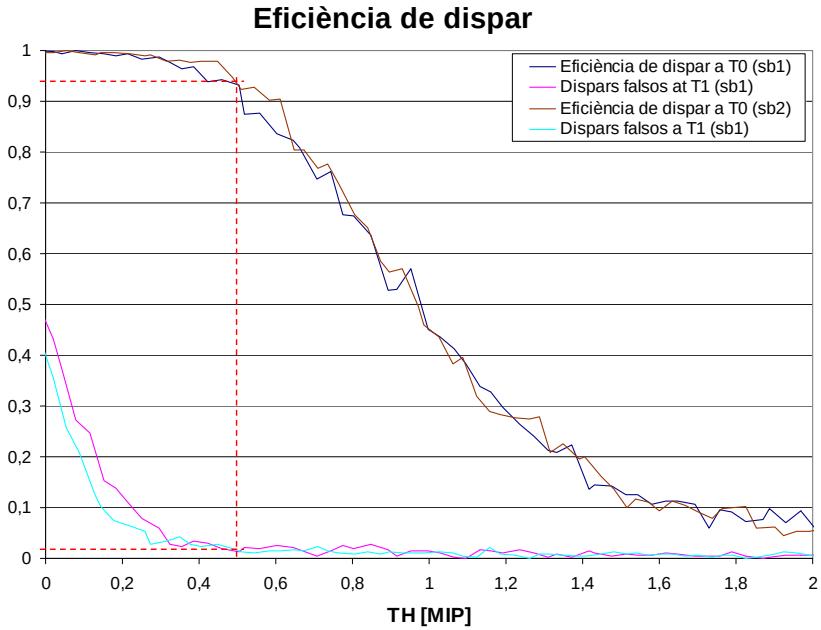

Figura 36. Eficiència de dispar i fracció de falsos dispars del sistema en funció del nivell llindar.

L'ASIC s'ha irradiat amb ions pesats. L'experiment es va fer al *Gran Accelerateur National d'Ions Lourds* (GANIL) a Caen en combinació amb els grups del LAL i el LPC. Aquestes mesures van permetre estudiar l'efecte combinat de dany de desplaçament (NIEL), dosi total ionitzant (TID) i els fenòmens de SEU o SEL. Amb aquest mètode, els dos primers efectes no són distingibles entre sí ja que els dos produeixen el mateix tipus d'alteració en les característiques de funcionament del circuit, aquests efectes romanen una vegada que l'exposició ha acabat.

La Figura 37 mostra la secció eficaç de SEUs, amb l'aproximació de la funció de Weibull. Sumant els efectes de tots els tipus d'ions que es poden obtenir en les col·lisions, la probabilitat màxima dóna un resultat de $1{,}0148 \cdot 10^{-13}$ SEU cm^2/neutró. Tenint en compte que es preveu que la fluència en les coordenades de LHCb on s'instal·laran els ASICs és de $4{,}2 \cdot 10^9$ neutrons·cm^{-2}any^{-1}, podem esperar uns 3 SEUs/any pels 6000 canals del SPD.

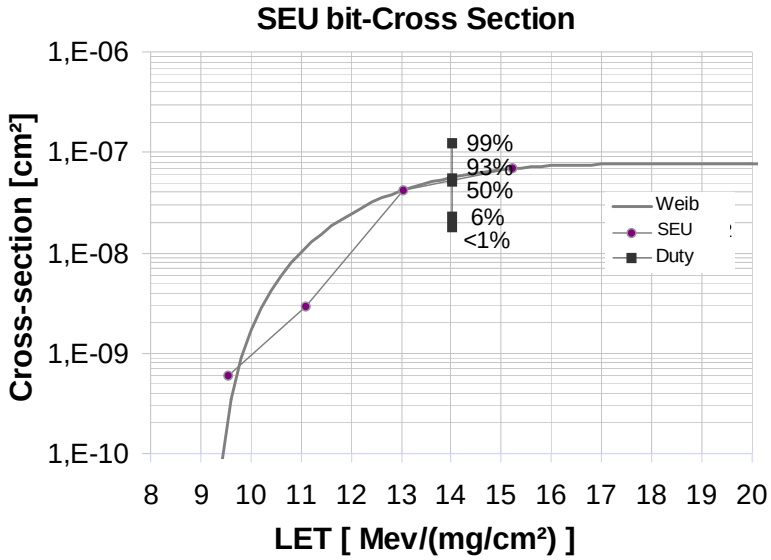

Figura 37. Secció eficaç de SEUs del ASIC.

Respecte el SEL, per una energia dispositada de 15 MeV·cm^2·mg^{-1}, que és la que es preveu que com a màxim dipositarà una partícula en LHCb, no se'n va detectar cap, de forma que amb un nivell de confiança del 90% s'espera trobar un SEL cada 20 anys. El circuit es pot considerar com a qualificat, ja que el temps de funcionament de l'actual LHCb serà com a màxim de 10 anys.

Respecte als efectes acumulatius, NIEL i TID, no es va trobar cap degradació significativa en el funcionament del circuit un cop irradiat. Els límits de radiació previstos són de 58 Gy màxim i 35 Gy en promig. És habitual aplicar alguns factors de seguretat sobre aquest nombres. El factor d'incertesa en la simulació ja està inclòs. Considerant un factor 2 per la variació de component a component i la pròpia incertesa del test, obtenim un màxim de 232 Gy i un valor promig de 140 Gy, valors que es van sobrepassar àmpliament en el test, on els diferents ASICs van acumular dosis entre 237 Gy i 450 Gy.

Una descripció molt més detallada dels tests de radiació la podem trobar a [185] i a [186].

4 Conclusions

S'ha dissenyat, fabricat i comprovat el funcionament d'un ASIC per dur a terme la lectura del SPD de LHCb. L'arquitectura del circuit ha estat optimitzada per poder treballar en experiments de física de partícules d'alta lluminositat en els que no és acceptable tenir temps mort i en els que el temps de captació del senyal és comparable al temps de mesura, el període de creuament de feixos en el cas de LHC. L'ús d'un integrador commutat per mesurar la càrrega del pols de corrent corresponent al senyal de l'escintil·lador permet minimitzar l'efecte de les fluctuacions estadístiques en la forma del senyal. Aquesta solució, juntament amb el fet de duplicar el sistema de processament analògic, de manera que els dos sistemes resultants treballen alternativament, permet integrar el senyal durant pràcticament tot el temps disponible sense introduir temps morts i també realitzar una correcció de la cua del senyal que es perllonga més enllà dels 25 nanosegonscorresponents al temps de creuament de feixos.

La tolerància a la radiació s'ha tingut en compte des del primer moment a nivell de disseny:

- Us extensiu de mecanismes de realimentació local per minimitzar les conseqüències principals de la radiació acumulada en els transistors bipolars (degradació del guany de corrent β).
- Prevenció de SELs mitjançant l'ús d'anells de guarda allà on s'empren circuits CMOS.
- Redundància en la part digital per prevenir SEUs. S'empren sistemes de lògica de votació triple.

Les mesures experimentals realitzades validen el funcionament del circuit dins dels requeriments inicials que s'havien fixat. El disseny d'aquest ASIC no ha estat únicament un exercici de simulació o prototipatge, se n'han fabricat i comprovat al voltant de 1500 unitats, obtenint un rendiment d'un 80 %. En aquest sentit, l'estudi de l'efecte de la variabilitat dels paràmetres de fabricació en el funcionament del circuit ha estat clau, ja que ha permès aplicar des d'un principi els criteris de disseny necessaris per assolir un rendiment acceptable.

És important assenyalar alguns punts on aquest treball aporta certes novetats metodològiques que queden fora de l'abast d'aquest resum però que es poden trobar exposades en major detall en els capítols 2 i 5. En primer lloc, i en relació amb el que es comentava a l'anterior paràgraf, s'ha proposat un mètode per estudiar la resposta a les variacions de la tensió d'alimentació en circuits diferencials tenint en compte l'aparellament dels dispositius (veure també [171]). Per una altra banda, respecte a l'anàlisi del soroll, s'ha presentat un mètode per estudiar circuits variants en el domini de la freqüència. Aquest fet obre la possibilitat d'estudiar l'efecte del soroll *1/f* en circuits variants amb el temps, fet que ha estat qüestionat per diversos autors ([94],[126]) .

Pel que fa a les línies de futur d'aquest treball, com s'ha comentat anteriorment, l'arquitectura proposada pot ser molt apropiada per experiments d'alta lluminositat on el període entre col·lisions sigui molt petit i es tingui una ocupància relativament alta. Aleshores, és possible pensar en utilitzar aquesta arquitectura en futurs projectes com SLHC (una millora de LHC que està en estudi [187]) o fins i tot al CLIC (Compact Linear Collider [188]), on el període entre col·lisions estaria per sota del ns. Per aquests projectes caldrà emprar tecnologies nanomètriques, en les que el soroll *1/f* comença a ser un factor a tenir molt en compte. Tanmateix, les tècniques presentades en aquest treball podrien ser una eina per afrontar aquest problema.

Les possibles millores del circuit començarien segurament per dissenyar una nova etapa d'entrada, i possiblement bona part de la circuiteria, en mode corrent. El senyal de molts detectors es pot modelar com una font de corrent, sembla aleshores raonable pensar en implementar una entrada en corrent, és a dir, de baixa impedància, que permet eliminar pols que poden limitar la resposta en freqüència del circuit i minimitzar acoblaments capacitius, i per tant problemes com el soroll acoblat o la diafonia. El segon pas seria tractar de reduir el soroll equivalent a l'entrada (ENC), permetent que el circuit s'utilitzi per llegir sensors que tenen un guany inferior al PMT, com els fotodíodes d'allau, o fins i tot, anant més enllà, detectors de silici i de gas en general.

Reemplaçar el discriminador per un conversor analògic-digital permetria emprar el circuit en calorimetria o en sistemes de traces de lectura no binària.

Podem apuntar algunes línies de futur més ambicioses. Recentment s'ha demostrat la possibilitat de fabricar dispositius de comptatge de fotons i fotomultiplicadors de silici basats en fotodíodes d'allau treballant en mode Geiger mitjançant tecnologies CMOS estàndard [189], així doncs seria possible pensar en integrar l'arquitectura proposada juntament amb el sensor, que podria ser un fotomultiplicador de silici.

1 Introduction

On the one hand, the aim of this thesis is to present a solution for implementing the front end system of the Scintillator Pad Detector (SPD) of the calorimeter system of the LHCb ([1], [2] and [3]) experiment that will start in 2008 at the Large Hadron Collider (LHC) [5] at CERN. The requirements of this specific system are presented in the third chapter. On the other hand it will be shown that the architecture developed for this system is a general solution for front ends in high luminosity experiments that must be operated with no dead time and must be robust against ballistic deficit.

This chapter presents background concepts on the field of particle physics instrumentation. In section 1.1 general concepts about front end electronics for Nuclear and High Energy Physics (HEP) detectors will be introduced. Afterwards, in section 1.2, it is presented the motivation for the monolithic implementation of front end system of complex High Energy Physics experiments, using Application Specific Integrated Circuits (ASICs).

1.1 Front end systems: Analogue processing of detector signals

Although many different devices such as scintillator counters, gas chambers or semiconductors sensors are employed both in Nuclear Sciences and in High Energy Physics (see [7], [8] and [9]), the procedures to amplify and measure the detector signals for all the detectors are similar, and some general considerations can be made (see [7], [8] ,[9],[10] and [11]).

In most of the detectors a charge Q is produced at the time that radiation is detected, thus, a detector produces not a continuous signal but a series of discrete pulses of current occurring randomly in time. The amount of charge produced by the detector is proportional to the energy distribution[c] of the incident radiation. The charge generation in the detector has statistical fluctuations which are often referred as 'noise in signal'. These fluctuations are convoluted with the energy spectra in the measured spectra.

The detector signal is amplified in order to be measured. In modern systems, to measure means to convert the detector signal to a digital signal, either to a pulse carrying position and time information either to a digital word where the amount of charge is coded. The intrinsic electronic noise of this system is also convoluted with the energy spectra, and should be controlled in order to not degrade the energy resolution.

1.1.1 Preamplifiers

The basic function of a preamplifier is to amplify weak signals from a detector and to drive it through the next stage. At the same time, it must add the least amount of noise possible: the first stage determines the Signal to Noise Ratio (SNR) of the whole electronic chain if its gain for the bandwidth of the system is large enough. Preamplifiers are normally mounted as close as possible to the detector so as to minimize cable length. In this way, pick-up (interference) of stray electromagnetic field is reduced and cable capacitance, which usually decreases the SNR, minimized. Figure 1-1 shows a

[c] In Nuclear and High Energy Physics the deposited energy by an incident radiation in a detector is defined as a probability distribution and the measurement of this distribution is called radiation spectroscopy or spectrometry.

schematic representation of the detector (modeled as the current source I_{det}) and preamplifier connection.

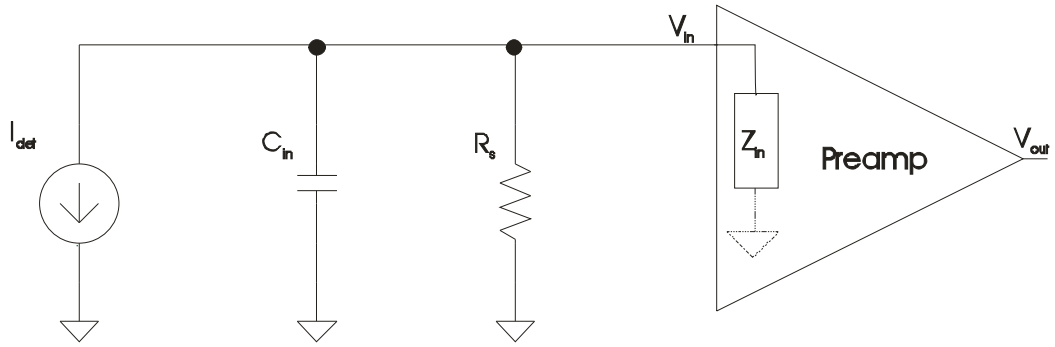

Figure 1-1. Schematic representation of the detector and preamplifier inter-connection.

The rise time of the output pulse of the preamplifier is kept as short as possible, consistent with the charge collection time in the detector itself (which gives the rise time of the input signal). The decay time of the output pulse of the preamplifier depends on the preamplifier configuration. There are three typical preamplifier configurations:

1. Voltage sensitive configuration. Historically, this type is the more conventional in many electronic applications and consists simply of a configuration that provides an output pulse whose amplitude is proportional (by the amplifier gain) to the amplitude of the voltage pulse supplied to its input terminal and with the same shape (provided that preamplifier bandwidth is higher than input voltage signal bandwidth). Its input impedance (Z_{in}) is high (ideally infinity). Since no current flows into the preamplifier, the shape of the voltage pulse depends on the capacitance at the input C_{in} (which includes detector, stray and preamplifier input capacitances) and the load resistor R_s. If the charge collection time is large compared with the time constant of the input circuit ($C_{in} \cdot R_s$) the input (and output) voltage follows the current shape $V=I \cdot R_s$. If the time constant of the input circuit is large compared with the charge collection C_{in} is charged by the detector current and $V=Q/C_{in}$. The last situation is dangerous in detectors whose input capacitance is not constant, like semiconductor diode detectors.
2. Current sensitive configuration (transimpedance preamplifiers). The amplitude of the output pulse of the preamplifier is proportional to its input current by a certain constant called transimpedance. The input impedance (Z_{in}) should be much smaller than the input circuit impedance for the signal bandwidth (to be independent from the input circuit), in that case the detector current flows into the preamplifier and the amplitude of the output voltage is proportional to the detector signal and has the same shape (provided that preamplifier bandwidth is higher than the bandwidth of the detector signal).
3. Charge sensitive configuration. The input impedance (Z_{in}) should be much smaller than the input circuit impedance for the signal bandwidth, in that case the detector current flows into the preamplifier and it is integrated. The preamplifier output amplitude is proportional to the total integrated charge. The preamplifier output shape does not keep the detector signal shape. The decay time of the preamplifier output is made quite large so that the full collection of the charge is reflected in the output amplitude.

1.1.2 Shapers or main amplifiers

The main purpose of this stage is to shape the signal from the preamplifier to a convenient form for further processing preserving the information of interest. If timing information is required, a fast response is necessary. If pulse height or charge information is desired, a strict proportionality between

input and output amplitudes must be preserved (linear amplifier), or at least, the shaper transfer function must be stable and precisely known.

In order to ensure that complete charge collection occurs, charge sensitive preamplifiers are normally adjusted to provide a decay time for the pulse which is quite long. If the rate of pulse generation in the detector is high enough, these pulses will tend to overlap one another and give rise to a pulse train that has the appearance shown in Figure 1-2(a). Because it is the amplitude that carries the basic information, for charge preamplifiers, the "***pile-up***" of pulses on the tails of preceding pulses, which have not fully decayed to the "zero" or "***baseline"*** level, can be a serious problem. Because the time spacing in pulses is random, each pulse can be superimposed on a different residual tail and the resulting amplitude no longer is a good measure of the charge Q from that event. The ideal solution is to shape the pulses in such a way to produce a pulse train similar to that shown in Figure 1-2 (b).

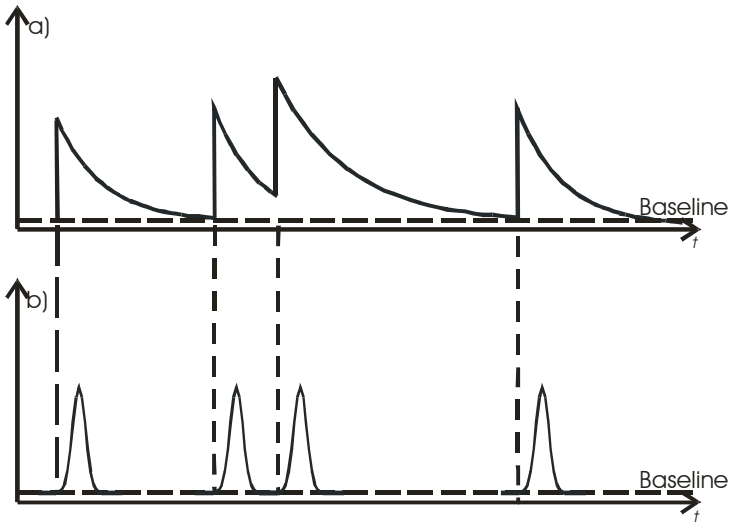

Figure 1-2. The pulses with long tails shown in part (a) illustrate the apparent variation in amplitude due to a pulse pile-up. These effects can greatly be reduced by shaping (schematic representation) the pulses as in (b).

A second reason for pulse-shaping is the optimization of the signal to noise ratio. For a given noise spectrum, there usually exists an optimum pulse shape in which the signal is least disturbed by noise. The relation between pulse shape and noise can be best understood by looking at the signal in terms of their Fourier components. Optimizing the SNR, involves narrowing the bandwidth without disturbing the relevant frequency components of the signal.

The range of the methods of implementation of shapers is wide: through active or passive networks, through time invariant or time variant systems, through analogue or digital filters. Regardless of the method of implementation, the properties of the most common shapers can be enounced as follow:

a) ***Differentiator (CR) or high pass filter***. Step response is $e^{-\frac{t}{\tau}}$, it has a sharp rising edge and exponential decay of τ=CR time constant. The sharply pointed top makes subsequent pulse height analysis difficult. High frequency noise is not rejected.

b) ***Integrator (RC) or low pass filter***. Step response is $1-e^{-\frac{t}{\tau}}$, the output voltage approaches the input step as a limit. Low frequency noise is not rejected.

c) ***CR-RC shaping (band pass filter)***. Combination of a single stage differentiation (τ_1) and single stage integration (τ_2). With impedance isolation step response is: $\frac{1}{\tau_1-\tau_2}\left(e^{-\frac{t}{\tau_1}}-e^{-\frac{t}{\tau_2}}\right)$, usually both time constants are made equal. Equation for step response becomes

indeterminate, a particular solution is: $\frac{t}{\tau} e^{-\frac{t}{\tau}}$. The time constant of the shaper must be small enough to return to baseline as fast as possible to avoid pile-up and must be much larger than the collection time of the detector (the rising time of the charge preamplifier output). If last condition is not meet, the input of the shaper no longer appears as a step voltage and some of its amplitude is lost. This loss is called is ***ballistic deficit*** and it is especially dangerous if the collection time is not constant because it will appear as noise in the signal. At the same time, the SNR characteristics are influenced by the choice of shaping time as described in section 2. The proper choice for shaping time for a given circumstance thus becomes a complex balance between factors involving ballistic deficit, electronic noise and pulse pile-up.

d) ***Gaussian or CR-(RC)^n shaping***. If a single CR differentiation is followed by several RC integrations, a pulse shape that approaches a mathematical Gaussian is realized. If the differentiation and n integration time constants are all the same value τ, the particular solution of the corresponding circuit equation is $\left(\frac{t}{\tau}\right)^n e^{-\frac{t}{\tau}}$. In practice four stages of integration are sufficient so that the difference between the resulting pulse and the Gaussian is negligible. The time required for the shaped pulse to reach its maximum amplitude (often called *peaking time*) is equal to $n\tau$. For equal time constants throughout, a CR-(RC)^4 network results in a peaking time that is factor of 4 longer than that for a simple CR-RC network. However, if the time constants are adjusted to give equal peaking times for the two methods, the more symmetric shape of the Gaussian pulse results in a faster return to the baseline. Pulse pile-up at high counting rates is thereby reduced. Gaussian shaping also has the advantage of better SNR characteristics. For these two reasons, Gaussian shaping has become a popular choice.

e) ***Triangular shaping***. The discussion of SNR behaviour of different pulse-shaping schemes given in chapter 2 points out the theoretical advantage that a shaper with a triangular step response has over the Gaussian shape.

f) ***Trapezoidal shaping.*** For detectors in which the charge collection time is variable, the potential problem of ballistic deficit favours pulse shaping methods that lead to a shaped pulse with a flat top, such as a trapezoidal step response.

Thus far our comments on pulse shaping have assumed that the input pulse from the preamplifier consists of a step voltage. Although the decay of the preamplifier pulse is usually long, it is not infinite and the finite decay will have a measurable effect on the response of the networks discussed above. If the shaping network includes a differentiation, there will be a slight zero crossover or *undershoot* of the pulse, which the recovers to zero with a decay time characteristic of the preamplifier decay time. The term ***pole-zero cancellation*** describes a technique in which the network is modified to include a zero in its Laplace transfer function to cancel the pole related to the time constant of the preamplifier fall.

This effect is part of a more general problem related to the presence of differentiations in the transfer function of the whole measurement system: ***the baseline shift***. Differentiations are related either to zeros (differentiators) of the shaping networks either to alternate current (AC) coupling in the measurement chain, usually both are related to the presence of series capacitances. Because the capacitor cannot conduct direct current (DC), the average DC voltage after the capacitor must be zero. Therefore, the baseline on which the pulses are superimposed must be shifted below the true zero level such that the areas enclosed by the output waveform above the zero axis are equal. The amount by which this apparent baseline is depressed below the true zero is and will obviously become more severe as the average spacing between pulses is made smaller. Spacing between detector pulses is random, therefore the degree of baseline shift is not constant and it will affect as a noise.

In principle, baseline shifts can be eliminated if the pulse shape is made to be bipolar rather than monopolar. Bipolar pulses contain negative and positive lobes and if both lobes are of equal area, its average DC value can be zero and it can be passed by a capacitor without alteration of the baseline. The SNR is generally poor after bipolar shaping compared with monopolar shaping that results in the same pulse width. Thus a logical choice is to use monopolar shaping for better SNR characteristics at low counting rates and bipolar shaping only when required for baseline restoration performance at high count rates. A common implementation of a bipolar shaping is the ***double differentiation or CR-RC-CR shaping***. The bipolar shape makes baseline shifts less severe, but because the two lobes of the pulse are not of exactly equal area, some baseline shift will remain.

Another solution is making use of an active electronic circuit to eliminate the baseline shift: a ***baseline restorer***. A schematic representation of a baseline restorer circuit is shown in Figure 1-3 [11]. The switch S1 is open only during the duration of each pulse, and its closing restores the output voltage to the baseline. Gated baseline restorer are based on the same principle used for auto-zero circuits in instrumentation. The stability of baseline restoration at very high counting rates with the gated baseline restorer depends on the ability of the gating control circuits to distinguish between the pulses and the baseline. In the simpler circuits, this is accomplished with a discriminator whose threshold is manually adjusted to sit just above the noise that surrounds the baseline. The more sophisticated amplifiers include automatic noise discriminators and more complicated pulse detection methods to perform this task more effectively. In other modern circuits, the role of the switch is carried out by diodes or by more complex nonlinear circuitry [11].

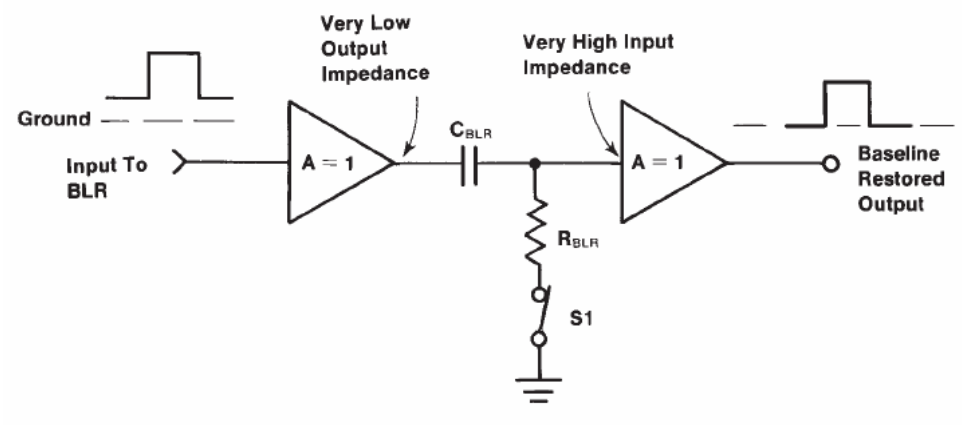

Figure 1-3. Simplified diagram of a baseline restorer. Figure taken from [11].

Another way of making shaper circuits is the ***Delay line shaping.*** Amplifiers employing delay-line pulse shaping are well suited to the pulse processing requirements of scintillation detectors. The propagation delay of distributed or lumped delay lines can be combined into suitable circuits to produce an essentially rectangular output pulse from each step-function input pulse. For pulse pile-up prevention, this shaping method is close to ideal because an immediate return to baseline is obtained. SNR characteristic of delay-line shaping is inferior to that obtained with simple CR-RC or semi-Gaussian shaping. There are many circuits that can be used for delay-line shaping, and the circuit shown in Figure 1-4 is typical[d] of one that is very tolerant of delay-line imperfections. The step pulse from the preamplifier is inverted, delayed, and added back to the original step pulse. The result is a rectangular output pulse with a width equal to the delay time of the delay line. In practice, the value of the resistor labelled $2R_D$ is made adjustable over a small portion of its nominal value to allow compensation for the exponential decay of the input pulse. With proper adjustment, the output pulse will return to baseline promptly without undershoot.

[d] Other delay line shapers use open stubs to make the pulse clipping.

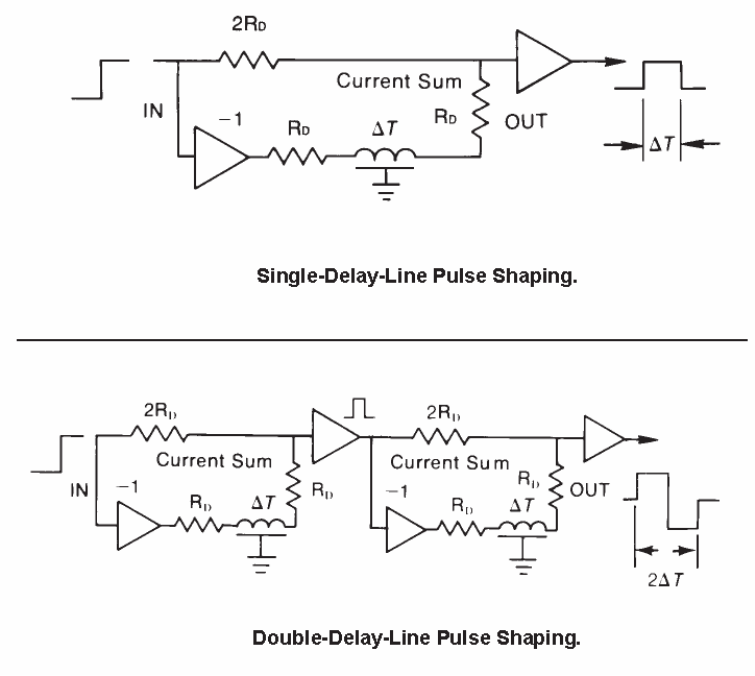

Figure 1-4. Delay line shaping. Figure taken from [11].

By following one delay-line shaper with a second, a doubly differentiated delay-line shape is obtained, as illustrated in Figure 1-4. The result is an output pulse shape that has a positive rectangular lobe followed by a negative rectangular lobe with equal amplitude and duration. The double-delay-line shaping is ideal for use with scintillation detectors in systems incorporating AC-coupling. The baseline shift caused by changing counting rates in AC-coupled systems is virtually eliminated by the two lobes having equal area above and below the baseline. This benefit is gained at the expense of doubling the pulse width. Double-delay-line shaping is often useful for simple zero-crossover timing with scintillation detectors at low or high counting rates. Double-delay-line shaping is not a good choice for detectors having a substantial preamplifier noise. Its signal-to-noise ratio is worse than single-delay-line shaping, and much worse than semi-Gaussian shaping.

In the previous few pages the functions incorporated in linear pulse-shaping amplifiers have been described in terms of analogue signal processing components. Alternatively, most of these functions can be implemented by means of ***Digital Signal Processing (DSP)***. Basically, the DSP method converts the continuous analogue signal at the output of the preamplifier to a stream of digital numbers representing the history of the preamplifier output voltage. The technique is implemented by using a flash ADC to repeatedly sample and digitize the preamplifier signal. The constant interval between samples is typically small so that the digital numbers represent the pulse profiles with reasonable accuracy. For every analogue pulse processing function in the continuous time domain, one can construct an equivalent function in the discrete time domain of the digital representation. Thus, the equivalent signal processing can be implemented in a computer. Because software computation would be too slow to keep up with the data rates, the processing is typically done in Digital Signal Processors or using re-programmable hardware (FPGAs, PLDs, etc). The benefits of digital signal processing are greater flexibility in realizing the optimum pulse-shaping filter over the entire range of shaping time constants, improved temperature stability and ballistic deficit correction at short shaping time constants and optimum energy resolution at long shaping time constants. Drawbacks are increase in system complexity, size and power dissipation which is especially problematic for large experiments.

1.1.3 Discriminators and analogue to digital converters

Modern HEP experiments use complex data acquisition systems that combine results of millions of detector channels. Relevant data is triggered and stored to be analyzed by processor farms. Thus, it is mandatory to change the signal domain from analogue to digital.

For detectors that only provide the number or rate of pulses from radiation detector a ***discriminator*** circuit is used to convert the pulse information to a digital signal. The discriminator is a device which responds only to input signals with a pulse height greater than a certain threshold value. If this criterion is satisfied, the discriminator responds by issuing a standard logic signal; if not, no response is made. The value of the threshold can usually be adjusted by a potentiometer or by another digital or analog interface. The pulse width depends on the type and implementation of discriminator. Two important parameters measuring the speed of the discriminator are the double pulse resolution and the continuous pulse train or cw rate. The double pulse resolution is the smallest time separation between two input pulses for which two separate output pulses will be produced. For fast discriminators, this is usually on the order of a few nanoseconds. The continuous pulse train rate is the highest frequency of equally spaced pulses which can be accepted by the discriminator.

An ***analog-to-digital converter (ADC)*** measures the maximum amplitude of an analog pulse and converts that value to a digital number. The digital output is a proportional representation of the analog amplitude at the ADC input. Three types of ADCs are used often in HEP and nuclear electronics: the flash ADC, the Wilkinson ADC, and the successive-approximation ADC. Only the latter two are used for high-resolution pulse-height spectroscopy. The advantage of flash ADCs is speed, conversion times are in the nanosecond range. The disadvantage is large differential nonlinearity (non-uniformity of channel widths of a multichannel analyzer).

1.2 Considerations on monolithic implementations

To analyze the role of monolithic implementations of the read out electronics for particle detectors it can be useful to have a brief look on the short history of the low noise electronics in radiation detection. Studies of noise in charge amplification had started concurrently with the use of gas ionization chambers and proportional detectors. The advent of silicon and germanium detectors in the 1960s and the development of junction field-effect transistors (JFETs) provided an impetus to the development and understanding of low-noise techniques for charge measurements. In connection with this work, methods for analyzing noise in the time domain were developed. This was particularly useful for understanding time-variant (switched parameter) signal-processing circuits.

In the mid-1970s, experiments in high-energy physics started to make use of low-noise techniques, benefiting considerably from the state of the art developed for low-energy nuclear physics. The detectors particularly dependent on optimization of signals and noise were total absorption devices (calorimeters), particle-tracking detectors based on gas drift chambers and on position sensing by charge division, and transition radiation detectors. From that time to the 1980s the electronics was based on discrete or hybrid implementations and the JFET was the device more used for a wide range of applications.

At mid 1980s the advent of the first vertex detectors for collider-type accelerators in particle physics made it clear that a front-end based on a monolithic approach was the only way to solve the problem of extracting and processing the signals from the high-density configurations of electrodes. At the same time the diffusion of imaging techniques in highly diversified fields was setting the request for even more finely segmented detectors, also needing high density multichannel signal processors. In either case, the front-end circuits are mixed-signal architectures combining an analog section and a digital section with a generally high functional density. Understandably, the first readout chips for segmented detectors relied upon CMOS as a readily available technology.

It became clear soon, however, that the CMOS processes of that time, featuring a gate length of a few microns and a thickness of the gate oxide of some tens of nanometres did not suit the most demanding applications. Noise was a serious limitation. The *1/f* noise associated with the channel current brought about a substantial contribution to the total equivalent noise charge (ENC) at the input (see chapter 2). Secondly, those CMOS processes were not radiation resistant to the extent required in several applications.

The noise issue conveyed the attention on monolithic processes featuring, along with the complementary MOSFETs devices, like junction field-effect transistors (JFET) or bipolar transistors, outperforming the MOSFETs from the noise standpoint.

Technologies like JFET-CMOS (Fraunhofer, Max Planck Institute, Pavia) and Bi-JFET-CMOS (DMILL) were developed and employed in some applications. The same technologies also provided upgraded radiation hardness as compared to the CMOS processes of the older generations. DMILL was conceived to be intrinsically radiation hard. The JFET-CMOS process would lend itself to a radhard design by a judicious circuit conception. It was recognized, indeed, that in the older CMOS processes, the most radiation-sensitive device was the N-MOS, so a design entirely based on N-JFET and P-MOS proved to lead to suitably radhard chips.

New trends [13] in the front-end design have appeared as a consequence of the advancement in CMOS processes known as *device scaling*. The device scaling has considerably reduced the gate length, entering the submicron and deep submicron regions, by virtue of which devices with gate length down to 60 nm are nowadays available. Perhaps even more importantly, it acted also in the sense of reducing the thickness of the gate oxide to a few nanometres and its replacement by new high-k dielectric materials. The result of a shorter gate and a thinner gate oxide is a remarkable improvement in noise and radiation hardness features of the CMOS processes, such to make them fully adequate for front-end design. A drawback of the reduction of the thickness of the gate oxide is the increase in leakage currents.

It is obvious to wonder where we stand now with the front-end design, as the upgraded CMOS processes are confining the JFET to a few, though scientifically relevant applications and new achievements, like CMOS processes featuring a high frequency Si-Ge bipolar transistor have appeared on the scene. Also new devices such as the FINFET [14] have appeared.

1.2.1 Space, power and cost requirements and implementation alternatives: Microelectronic Integration

A modern HEP experiment is typically composed of several detector layers: the vertex detector, the tracker, the calorimeter, and finally the muon detector. Sometimes a Ringing Image Cherenkov (RICH) detector is also present to improve the particle identification. The vertex detector determines the position of the primary and sometimes of the secondary interactions of the event. The tracking detector reconstructs the particle tracks which are curved for charged particles due to a 4 T (for CMS [15]) solenoidal magnetic field parallel to the beam axes. This way, the momentum of the particles can be measured and it can also be determined whether they originated from the collision itself or from a particle decay very shortly thereafter. The calorimeter determines the energy of both neutral and charged particles. Muons, very penetrating particles which are not stopped in the calorimeter, are detected in the muon detector.

Designs of front end electronics for different tracker or vertex detectors with binary output indicating the position of the energy are reported in [16] and [17]. Often the output provides information of the amount of charge deposited in each channel (when a particle deposits signal in more than one channel) in order to compute the center of gravity of the particle track, thus, increasing the position and momentum resolution. Designs of front end electronics for calorimeter detectors, with a digital output indicating the position and the amount of detected energy are reported in [18]. Table 1-1 summarizes key features of the detectors of a HEP experiment (CMS) [23].

Pixel vertex detector	
Number of channels	100 M
Power / channel	< 100 μW
Area channel	50 by 400 μm^2
Track position resolution	15 μm
Total area	.8 m^2
Radiation dose (10 yrs)	10-30 Mrad + 10^{13} neutrons/cm^2
Tracker	
Number of channels	12 M
Power / channel	< 3mW
Track position resolution	50-100μm
Radiation dose (10 yrs)	10 Mrad + 10^{14} neutrons/cm^2
Calorimeter	
Number of channels	100 K
Sampling rate	12 bit at 40 MHz
Radiation dose (10 years)	500 Krad + 10^{14} neutrons/cm^2
Muon detector	
Number of channels	300K
Timing resolution	0.7 ns
Radiation dose (10 years)	10 Krad + 10^{12} neutrons/cm^2
Date rate after level 1 trigger	1 Tbit/s

Table 1-1. System parameters for the CMS experiment

Considering all these parameters there are some reasons to think on a monolithic implementation:

- A high number of different detector channels must be processed in a constrained area. Especially in the case of vertex detectors.
- Power consumption should be minimized for the same reason.
- A digital preprocessing is necessary to reduce the amount of data.

Serial copper or optical link are used to send the data from detector to the "counting house" where tens of electronic racks house the Data Acquisition (DAQ) cards and processor farms. Anyway, data rate must be reduced selecting relevant information. If this were not done, taking only the calorimeter, 48 Tbit/sec should be transmitted and processed. There are two typical solutions to reduce the data rate:

a) A central system uses the key information of a reduced group of fast detectors to generate a trigger signal to select interesting data. On that case a buffer memory on the front end modules is needed to wait for the generation of the trigger.

b) Each front end module pre-processes the data without instruction of a central system. The preprocessing can be zero suppression, sparsification and even pattern reconstruction [19].

Figure 1-5 shows a typical front-end electronics system of modern HEP experiment (in this case LHCb [4]). LHCb is an experiment with trigger, according to the initial design shown in Figure 1-5 with two levels of hardwired trigger. First level, called L0, was designed to reduce the data rate to 1 MHz and second level produce a further reduction to 40 kHz so that the information can be processed by successive software trigger levels. The evolution of the computation power made possible to eliminate the second hardware trigger level, and the experiment has been build up with only one hardware trigger level. Furthermore, studies for future upgrades of the experiment consider the possibility of acquiring the full experiment data at 40 MHz, i.e. without any hardware trigger. This

shows and evolution from the architecture a) to a design close to b). A good introduction of HEP data acquisition (DAQ) and optical systems can be found in [6].

Figure 1-5 shows also how digital systems are included in the front end, and very often in the same chip that houses the analog front end. As was commented before, this fact favored the use of CMOS technologies from mid 1980s. The development of ASICs for HEP electronics instrumentation started in the eighties, and has been a key technology for the construction of the silicon micro-vertex detectors and silicon strip trackers during the LEP era. For the LHC electronics, the development of ASICs is now a pervasive design approach that has been utilized not only for tracker systems that require highly optimized and dense readout electronic channels, but also for all electronic systems ranging from front end electronics for calorimeter and muon systems to timing and trigger processors. For example, there are digital read-out architectures in which the analog data flowing from the analog front-end circuit is digitized in an array of analog-to-digital converters integrated in the same chip. This approach, employed for the silicon drift detector of ALICE (PASCAL)[16], has been possible thanks to the low power analog design and the 10-bit 4 Msamples/s ADC that has a power dissipation below 2mW.

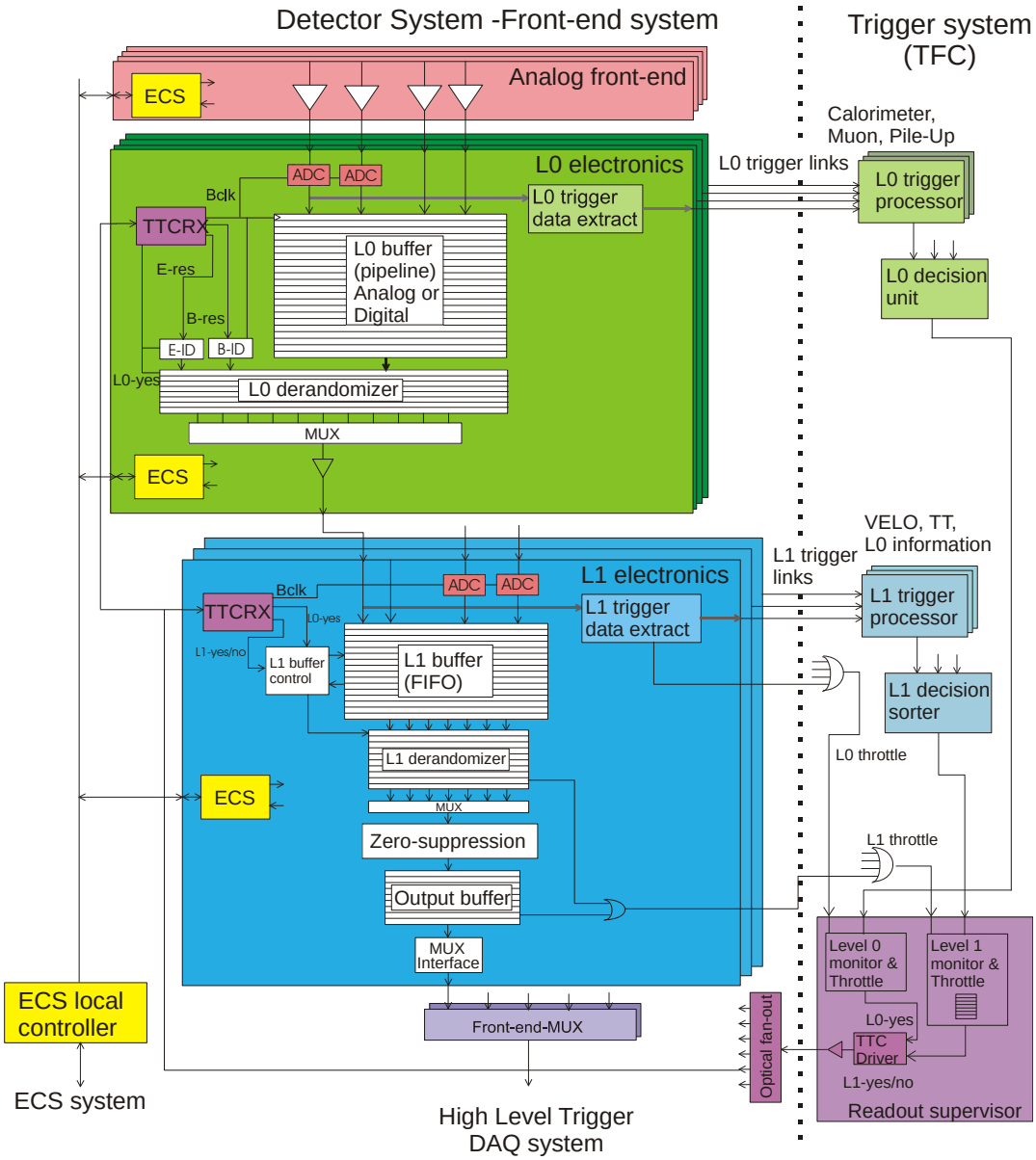

Figure 1-5. Front electronics architecture of the LHCb experiment. Figure taken from [20].

Some HEP experiments are performed in the space (Cosmic Ray experiments such as AMS [21] which will be installed in the international space station) or in the deep of the sea (Neutrino experiments such as Antares [22]). In those cases it is obvious the necessity of using a compact and low-power instrumentation.

1.2.2 The radiation qualification

Total Ionising Dose (TID) effects, are due to the energy deposited in the electronics by radiation in the form of ionisation. The unit for TID in the International System is the Gray (Gy)[e]. Ionisation in the silicon dioxide, used in semiconductor devices for isolation purposes, generates electron-hole pairs that can be separated by a local electric field. The defects appear in the device as trapped charges in the silicon dioxide. The consequent macroscopic effect varies with the technology. In CMOS technologies the threshold voltage of transistors shifts, their mobility and transconductance decrease, their noise and matching performance degrades, and leakage currents appear. In bipolar technologies, transistor gain decreases and leakage currents appear.

Non-Ionising Energy Losses (NIEL) in silicon cause atoms to be displaced from their normal lattice sites, seriously degrading the electrical characteristics of semiconductor devices. For displacement damage, it is common practice to express the radiation environment in terms of the particle fluence (particles/cm^2). The induced damage is a function of the particle nature and energy, and the Non-Ionising Energy Loss is used as a parameter to correlate the effects observed in different radiation environments. Though this correlation is not free from uncertainties and fails in some cases, it is still commonly used to translate a complex radiation environment into a simpler mono-energetic equivalent, namely 1 MeV neutrons. The macroscopic effect of displacement damages varies with the technology. CMOS transistors are practically unaffected up to particle fluences much higher than those expected at LHC. In bipolar technologies, displacement damage increases the bulk component of the transistor base current, leading to a decrease in gain. Other devices being sensitive to displacement damage are some types of light sources, photodetectors and optocouplers.

Single Event Effects (SEEs) effects are due to the direct ionisation of a single particle, able to deposit sufficient energy in the ionisation processes to disturb the operation of the device. In the LHC, the charged hadrons and the neutrons of the primary particle environment do not directly deposit enough energy to generate a SEE. Nevertheless, they might induce a SEE through nuclear interaction in the semiconductor device or in its close proximity. The recoils from the interaction are indeed often capable of a sufficient energy deposition.

Most available SEE data refer to heavy ion irradiation tests, and expresses the sensitivity of the components as a function of the Linear Energy Transfer (LET)[f] of the incoming particle. Devices with threshold LET below 15 MeVcm^{2}mg^{-1} can be sensitive to SEE in the LHC environment. Below this value, the lower is the threshold, the higher the sensitivity of the component.

Due to their statistical nature, it is possible to speak of SEEs only in terms of their probability to occur, which will depend on the device, and the flux and nature of particles. Therefore, the best one can do is to estimate their rate in the expected radiation environment.

The family of SEE is very wide; but the main members are Permanent SEEs, Static SEEs and Transient SEEs:

- **Permanent SEEs**, also known as “Hard errors”, may be destructive. The best known is Single Event Latchup (SEL) which occurs in CMOS technologies, when the parasitic npnp thyristor is triggered by the ionising energy deposition in a sensitive region of the circuit. This leads to an almost short-circuit current on the power lines, which can permanently damage the

[e] 1 Gy is equivalent to 100 Rad.

[f] The LET is defined as the energy lost by the particle to the material per unit path length (MeV/cm) divided by the density of the material (mg/cm^3).

device. Sometimes, this condition can be local and the current limited (microlatchup), the effect can still be destructive. Some others effects like the Single Event Burnout (SEB) and the Single Event Gate Rupture (SEGR) are typical for power devices and can also lead to permanent damage. Stuck Bits have been observed in SRAM and DRAM circuits irradiated with heavy ions [28]. The state of the memory point is permanently changed to a logic value, without the possibility to rewrite the correct value. This event was traced back to the ionisation energy deposition of a single ion with high LET. Modern technologies should not be very sensitive to this effect.

- **Static SEEs** are not destructive, and happen whenever one or more bits of information stored by a logic circuit are overwritten by the charge collection following the ionisation event. These effects are known as Single Event Upsets (SEU). A special case of SEU is the Single Event Functional Interrupt (SEFI). This happens in complex circuits due to an error induced on a bit of information controlling a special function of the circuit, often special test mode or state machines where the error condition leads to loops or hangs the device. A reset is necessary to bring the circuit back to the operational condition. The effect on modern FPGAs may be even worst, because most use SRAM to store configuration and a SEE on the configuration SRAM will require a reconfiguration of the device.

- **Transient SEEs**, charge collection from an ionisation event creates a spurious signal that can propagate in the circuit. This may happen in most technologies, and its effects vary significantly with the device, the amplitude of the initial current pulse, and the time of the event with respect to the circuit synchronizing signals. Typical examples are transient pulses in combinatorial logic, which can propagate and ultimately be latched in a register, and rail-to-rail voltage pulses at the output of operational amplifiers (SET).

Concerning ionizing damage, deep submicron CMOS technologies become increasingly interesting for the High-Energy Physics community for the design of ASICs to be used in the harsh radiation environment of the LHC experiments and even on Super LHC (SLHC), a possible upgrade of LHC with increased luminosity [41]. It has been verified that the thin oxides of deep sub micron technologies, below 7nm thickness, exhibit excellent intrinsic radiation hardness with tiny threshold voltage drift and mobility change after radiation exposure up 100 MRads levels. This hardness results from electron tunnelling in thin gate oxides, the same effect that becomes a major obstacle for ultra-thin gate in nanoscale technology. To eliminate radiation-induced leakage currents in the still vulnerable lateral and field oxides, a special layout technique has been developed: the Enclosed Layout Transistor (ELT) [23]. Multi-Mrad total dose levels of radiation tolerance have been achieved in this way. Furthermore, a deep submicron (DSM) technology can more easily satisfy the strict requirements in terms of circuit density and power consumption of the ASICs for particle detector readout. Nevertheless, very DSM technologies present serious drawbacks for analogue design: very high leakage currents and large variability of the parameters.

Concerning JFETs and bipolar, some technologies like DMILL were conceived to be intrinsically radiation hard. Some commercial BiCMOS technologies like Austriamicrosystem (AMS) 0.8 μm have been proved to radiation tolerant: usable up to a TID of 50 to 100Krads. High speed bipolar technologies have been seen to be less sensitive than slower standard technologies.

Regarding SEEs, previous work shows that guard rings are very effective against latchup. It is possible to electrically induce latchup (by a pulse on Vdd) on standard ring oscillators in a 0.5-μm technology, but not on the ring oscillators with guard rings. No radiation-induced latchup was observed for either type of ring oscillator up to an incident linear energy transfer (LET) of 60 $MeVcm^2mg^{-1}$ (Iodine 240 MeV).

Following expectations, dynamic registers are more sensitive to SEU than static registers. However, due to the additional capacitance on the storage nodes, dynamic flip-flops using enclosed nMOS transistors are less sensitive than their standard counterparts. For static registers, both additional capacitance and the increased current drive capability increase SEU immunity. This immunity can be further improved for registers with a major impact on system operation (e.g., bias or operating-mode settings) by requiring in the design that two nodes have to be upset simultaneously

for their content to be altered which was the approach in [29]. Redundancy for increased SEU immunity can also be added in other ways [30], such as majority-voting schemes, for instance.

Further information about radiation effects can be found in [25], [26], [27] and [20].

1.2.3 The effects of scaling down trends

1.2.3.1 Technological trends

The already consolidated industrial CMOS technology node for analoge design, the 130nm CMOS process, uses thermal oxide to form the gate insulator. Subsequent technology nodes, 90 nm, 65 nm and below, employ novel high-k gate dielectrics with unproven radiation hardness. One can expect that the radiation hardness of 130 nm technology will be at least as good as the 250 nm technology, since the SiO2 gate dielectric will be the same. The thinner oxide (2nm) will even increase radiation tolerance because electron tunneling will be more efficient in neutralizing radiation-induced trap charges. Initial radiation tests performed for MOS transistors in 130nm technologies from three different vendors show, however, that the effects of parasitic transistors to the NMOS transistors are still significant [31]. Both, the resulting threshold voltage shift and the leakage current are significant. Thus, based on these results one would conclude that in order to provide reliable radiation resistance one has to add hardening by design using NMOS transistors with enclosed gate and guard rings in a similar way as it has been done for the 250nm technologies. On the other hand, intrinsic speed of deep submicron technologies, like the 130nm one, is very high and provides a significant margin for possible speed degradation in digital circuits due to radiation effects. Thus, many digital circuits using standard rectangular transistors, if designed with sufficiently high-speed margins, may stand required radiation levels. However, for digital blocks containing a large number of transistors one should expect an increase of the power dissipation due to additional leakage current induced by radiation. An upgrade of the LHC is under study, in this Super LHC (SLHC) the luminosity will be at least one order of magnitude higher. In addition to the total dose effects, in the Super LHC environment the SEE will become a major concern due to much higher fluxes of particles compared to the LHC. Due to low voltage and low gate capacitance, transistors in deep submicron technologies are expected to show higher sensitivity to SEE compared to older technologies. Indeed, the tests performed for 130 nm technology indicate very low threshold in LET of 1.6 $MeVcm^2mg^{-1}$ [31]. This should be compared with a threshold of 6 $MeVcm^2mg^{-1}$ measured for 250 nm technology hardened by design. This low LET threshold indicates clearly that the SEE issue has to be addressed very seriously in readout ASICs using a 130 nm technology for Super LHC environment

In addition, variability, low-voltage operation (1.2V) and gate leakage will become an issue for the design of analog front-end circuits, and the development of adapted analog design techniques is certainly necessary ([32], [33]). The technology scaling down does not only affect the transistor and interconnect, but also the circuit modeling and the matching; a comprehensive discussion can be found in [35] and [36]. Scaling of CMOS technologies from micron to submicron range has resulted in significant improvements of noise performance of MOS transistors used in the front end circuits, see [35], [36], [37], [38] and [39]. Thanks to increased transistor cut-off frequencies in submicron technologies the geometry and bias conditions of the input transistor can be driven by optimization of noise performance and not by the bandwidth requirements of the preamplifier, as was often the case for the circuits designed in older CMOS technologies. As a result, the input transistor in a typical front-end circuit in 250nm technology optimized for detector capacitance in a range of 10–20 pF is biased close to weak inversion [35]. This rule will be maintained also in the designs using 130 nm technologies. In weak inversion the transconductance of the input transistor, which defines the equivalent input voltage noise, does not depend on the transistor sizes anymore but only on the bias current. This dependence is linear like in a bipolar transistor.

For the sub-100nm CMOS process, 90 nm and below, radiation hardness of high-k dielectrics it is not yet determined and it is difficult to predict, and sub-1V supply voltage will make the design of any analog circuit extremely difficult. Pixel detectors could be the only remaining route to design front-end electronics in these future technologies, because binary readout could be still feasible and gain in noise and pixel density would be quite substantial. Monolithic integration of the pixel detector will be certainly an interesting approach for high-density pixel detectors.

Some particular low-noise situations may benefit from the availability of the bipolar transistor in BiCMOS technologies: for fast shaping times or for non-capacitive detectors with low parallel noise. Also BiCMOS processes that feature a SiGe transistor as bipolar device or Heterojunction Bipolar Transistors (HBTs) or GaAs MESFETs can be useful in some situations due to his high f_T (tens of GHz) as pointed out in section 2.6.7. The ratio transconductance vs bias current becomes similar for DSM MOS transistor in weak inversion and BJTs or HBTs. This comparison shows that with respect to the noise vs. power, figure of merit performance of MOSFETs in deep submicron technologies becomes comparable with performance of BJTs or HBTs, especially for short pulse shaping times, like for example 25 nanoseconds in the circuits optimized for LHC applications, when the shot noise of the base current in BJTs does not contribute significantly to the ENC.

In comparison of MOSFETs and BJTs or HBTs to be used as front-end devices one has to take into account two other aspects [35]. In order to keep a MOSFET in weak inversion for a given level of the bias current one has to keep the current density below a certain level, which requires using a relatively wide transistor. Thus, the input capacitance of such a transistor will be typically larger than the input capacitance of a BJT or a HBT that delivers the same transconductance. This will result in higher ENC in the circuit using a MOSFET compared to the circuit using a BJT or a HBT. On the other hand, in BJTs and HBTs one has to take into account an additional source of voltage noise due to base spread resistance, which scales with the emitter area. In order to keep the base spread resistance low one has to use a transistor with large emitter area, which results in large input capacitance and in low current density. As a result, the cut-off frequency f_T of the input transistor is usually much lower compared to the peak f_T specified for a given technology. In typical front end circuits for silicon strip detectors the cut-off frequency of the input transistor is about one order of magnitude lower that the peak f_T [35]. This is usually not a problem when using modern HBTs with peak f_T in a range of 100GHz or higher. However, a low current density in bipolar devices results in higher sensitivity to radiation displacement damage. It is well known that degradation of the current gain factor β scales with the current density; the lower the current density the larger the degradation of β. Although it has been demonstrated experimentally that new generations of HBTs with very high f_T exhibit higher radiation resistance compared to conventional BJTs, the lifetime of bipolar devices in radiation environment, like the one foreseen for the Super LHC, will be determined by degradation of β due to radiation damage. For small emitter areas, the degradation remains acceptable up to fluences of 10^{16}cm^{-2} and shows promise for SLHC applications, as this would allow optimum usage of both bipolar and CMOS technology for minimum power dissipation [36].

Future applications of nanoelectronics in HEP still remain unclear [33]. So far applications of single electron circuits have been limited to quantum electrometers and single-photon detection. The adaptation of the single electron transistor to analog front-end amplifier turns out to be extremely difficult. The single electron transistor cannot be used as a "detector impedance adapter" as is done with bipolar and MOS transistors, because its geometry is not scalable with the detector capacitance. Therefore, to be compatible, the detector should be segmented into nanoscale sizes, which is not an obvious approach.

1.2.3.2 Trends in Calorimeter electronics

From recent discussions and studies about future hadron accelerator developments, two major advances are being considered [18]. There seem to be two kinds of machine emerging each having a distinctive physics reach and environment: the large linear electron-positron colliders (like the future Linear Collider [47]), and the next generation of hadron colliders (the possible SLHC, for example).

The SLHC is a continuing quest for increasing luminosity: an increase by an order of magnitude of the luminosity at the LHC. Considering the difficulties that had to be overcome, and the time and effort expended in the development of the radiation hard electronics for the present design luminosity, this will be a challenge which will require a renewed major R&D effort.

On a longer time scale, there is also a continuing quest for higher energies. The dynamic range required in electromagnetic (EM) calorimetry at the LHC is just about at the limit that a front-end amplifier device can accommodate in linear regime [18]. All the readout schemes for a large dynamic range (approaching 10^5) require multiple gain ranges (or multiranging) prior to analog-to-digital conversion at the speed of interest at the LHC. To achieve this dynamic range, an input stage with sufficiently low noise, where the noise of a single input transistor dominates, is required. Anyhow, the noise value for the best bipolar junction transistors and advanced CMOS devices corresponds to an equivalent series noise resistance of ~15 ohms or input equivalent series noise $e_n \approx 0.5nV/(Hz)^{1/2}$ (the concept of input equivalent noise will be explained in chapter 2). Even if the intrinsic device noise could be reduced below this value (by increasing the device width and/or reducing the electron transit time), lower values are difficult to realize in practice due to additional resistances, e.g., in the base or in the metalization in monolithic circuits. If the preamplifier has a bandwidth of about 10MHz and a minimum gain of 10, to overcome the noise of subsequent stages, the output noise voltage would be around 30 μV r.m.s. The maximum signal at the preamplifier output is likely to be even less than 3 volts, particularly as the trend to lower operating voltages continues. This limits the dynamic range of a linear front end stage to about 10^5 or 16-17 bits (an analysis with respect to the current gives the same result). This happens to be just sufficient for calorimetry at the LHC.

A very large hadron collider ("VLHC") will require a different approach to the dynamic range problem than the present designs for the LHC since the energies will increase. Therefore non-linear front-end electronics should be considered.

Some RD projects have already started [47] for the future International Linear Collider (ILC) [46], since its time scale is shorter (about 10 years). The electromagnetic calorimeter [45] of the Linear Collider is a barrel with two end-caps made of sandwich silicon-tungsten structure. It is composed of 40 piled up layers of reading. The basic element for each layer is a diode with 1cm² area. The first constraint is a great number of channels of measurement. There are 34 Millions channels which represent 3400m² of silicon. Secondly, a great dynamic range is needed, about 15 bits, with accuracy on the data equal to 8 bits. Another important point is the very low consumption required; just few mW by channel. And finally the system is relatively slow comparing to LHC. There is one train every 200ms and each one represents 3000 bunch-crossings with 300ns bunch-crossing period.

A new solid state photodetector may have impact on the design of electronics for calorimeters, and also for RICH detectors. It is the silicon photomultiplier (SiPMT), and it is also known as solid state photomultiplier (SSPM), Geiger APD or Multi Pixel Photon Counter (MPPC). The SiPMT is a silicon avalanche photodetector with Geiger mode operation. It is a combination of microcell semiconductor structure with integrated quenching mechanism and common electrode structure. There are some RD efforts to study the possibility of a tile scintillator and WLS fiber readout with a SiPMT for the ILC Hadron Tile Calorimeter [47]. The gain of the device is very high (10^5 to 10^7), can be operated under high magnetic fields and has an outstanding single photon counting capability. For the moment main limitation are crosstalk, dark rate and dynamic range, which is approximately half of the number of microcells of the device. Design of electronics for such a detector will have to pay much more attention to pulse shaping and dynamic range than to noise performance.

1.2.3.3 Trends in electronics for pixel detectors

Concerning pixel detectors for tracking and vertexing [17], it may be that technical limits in the new detectors should now be considered in the earliest stages of design of new machines. One of the major issues here is the problem of cooling and its influence on material and hence tracking precision. As the push towards smaller pixels continues, the power consumption density (for the same time

precision) increases. This is because the input capacitance is dominated by pixel-to-pixel capacitance and the total pixel-to-pixel capacitance per unit area increases with granularity. Increasing the bunch crossing frequency would lead to a further increase in power density.

The future e^-p^+ machines will provide events which are essentially clean with relatively low multiplicity and with event rates in the range of kHz. For these applications it may still be possible to use projective detectors or pixel-type detectors where every pixel is read out. Charge Coupled Devices (CCD) and Monolithic Active Pixel Detectors (MAPS) sensors seem the most likely candidates here. Both detectors provide the very highest spatial resolution since the amount of material, which reduces the resolution, is minimized by integrating the sensor and the FE electronics in the same chip, but the readout tends to be relatively slow. MAPS sensors based on standard CMOS technologies are being studied ([49] and [51], for instance). The epitaxial layer is thin, of order 10 μm, and the sensor bias voltage is limited, so charge collection proceeds primarily by diffusion. However, these structures allow very small pixel sizes of order 10 μm, so the small capacitance yields noise levels adequate to detect the small signal charge from minimum ionizing particles with good efficiency, although the typical signal to noise ratio of 10 does not provide much margin. It has to be pointed out that there are some alternative architectures based on triple well that implement a full charge sensitive preamplifier in pixel to overcome this problem, also proposed [50] for a possible SuperB factory. The signal charge is very sensitive to minority carrier lifetime, as charge collection proceeds by diffusion and cannot be accelerated by application of bias voltages sufficient to form high fields throughout the sensitive region. This limits radiation resistance, although it appears to be adequate for the ILC [36]. DEPFETS, sensor devices with built-in amplification, are also considered for ILC [53] and are used in other areas [54].

For the hadron machines the pattern recognition capability of pixel detectors is likely to still be the dominant requirement. The very tiny charge collection from standard MAPS detectors makes achieving good pattern recognition extremely difficult.

Developments of monolithic pixels in SOI (silicon on insulator) technology are also starting. SOI detector wafers are formed by bonding together a top wafer with low resistivity and a bottom wafer with high resistivity, using a silicon oxide bond. A buried oxide is formed between the wafers. After bonding, the top wafer is thinned to just a few microns using one of several different techniques. Later, vias are etched through the buried oxide to implant diodes in the bottom wafer and CMOS circuitry is built on the top wafer. SOI integrated detectors have several advantages over MAPS. One big advantage is that both NMOS and PMOS transistors can be easily accommodated in the design. The devices inherently can have larger detector signals since the thickness of the depleted detector substrate can be controlled. Finally, since the substrate can be fully depleted, less charge spreading and higher speed is possible compared to MAPS. Early detector work was done in a 3 micron SOI technology [55]. Recent work has been done in the OKI 0,15 micron SOI process [56].

A very interesting technology utilizes multi-tier structures to integrate a fully depleted sensor layer with multiple layers of electronics [57]. These structures are often referred as ‘‘3D’’. However, the term 3D is already used for a novel detector structure, so multi-tier is more appropriate. In multi-tier fabrication the wafers could be of different technologies but there are significant advantages if the wafers are all made in an SOI process. The SOI process allows the wafer to be easily thinned to the buried oxide layer, resulting in active circuit layers that are less than 10 microns thick. Furthermore, the via formation in SOI is easier than in CMOS processes.

There are some developments based on multichip module (MCM) technology [58]. The BTeV [58] pixel detector module is based on a design relying on a hybrid approach. With this approach, the readout chip and the sensor array are developed separately and the detector is constructed by flip-chip mating the two together. This approach offers flexibility in the development process, the choice of fabrication technologies, and the choice of sensor material. The pixel multichip module prototype is composed of three layers. The high density interconnects (HDI) form the bottom layer. The back of the readout IC is in electrical and thermal contact with a ground plane on the top layer of the HDI, whereas the other side of the readout IC is flip-chip bonded to the silicon pixel sensor. The clock,

control, and power pad interfaces of the read out chip extend beyond the edge of the sensor and are wire bonded to the HDI. The HDI then extends to one end of the module where a set of wire bond pads interface the HDI to the data acquisition system.

In some detectors front end electronics has been operated in cryogenic conditions to reduce noise. Cryogenic operation of the readout electronics has the advantage that a better transconductance to drain current ratio is obtained even if the transistor thresholds are increased [63]. This may lead to the possibility of reducing the problem of power consumption density. In any case cryogenically cooled Si detectors, with or without defect engineering [63], might be used in future experiments.

1.2.4 The effect of parameter variability

Matching two components, such as two resistors, two capacitances, two transistors, etc., is one of the most important features. In practice components are never exactly identical. Because of tolerances of production processes (photolithography, etching, etc) the characteristics of two matched transistors are slightly different. In general, the lager the devices, the less a role of differences play.

Usually these small differences do not influence parameters such as the gain bandwidth (GBW) or linearity of an amplifier. Other characteristics, such offset (the random component of the offset, of course) or Common Mode Reject Ratio (CMRR) of differential stages are fully determined by the matching properties of the technology. Other characteristics like Power Supply Reject Ratio (PSRR) of differential amplifiers may depend on matching too.

Usually the foundry provided statistical information of the tolerances in their processes (see [64] for example). Several factors cause the parameters of an integrated circuit to show random variations. One of these factors is the randomness of the edge definition when regions are defined to form resistors, capacitors or active devices. In addition random variations across the wafer in the diffusion of impurities can be a significant factor. These processes usually give rise to a Gaussian distribution of the parameters. It is possible, then, to calculate the distribution (basically the dispersion or standard deviation) of a given circuit characteristic, like the offset or the CMRR, using the dispersion of the components or processes given by the foundry. This methodology is presented, for example, in [65], [66], [67] or [79]. The foundry also provides models for the common CAD tools used in integrated circuit design that include statistical information: worst case parameters or even Monte Carlo models.

The parameter dispersion of the offset, for example, could be a limitation for the resolution of a front end electronic system. Therefore, it is important to estimate the impact of parameter dispersion at an early stage of a design. It might happen that a technology has to be discarded as an implementation option if its parameter tolerances are too high.

There are several different design levels where parameter dispersion can be considered in order to be minimized:

- System design. For example, one of the most classical solutions to avoid offset is to concentrate the amplification on the first stage of a system and the AC couple its output to next stages. Other techniques such as auto-zero or DC common feedback loops are frequently used.
- Circuit design. It is possible to optimize circuit design to minimize the effect of parameter dispersion ([79], [66] or [67]). For example, if a given characteristic of a circuit is determined by the ratio of two components of the same type, it is less sensitive to fluctuations of the parameters of the fabrication process than if it is given by the absolute value of a component.
- Layout design. There several layout techniques [68] such as using common centroid components, using interleaving array of components adding dummy components or minimizing distances between critical components to avoid the effect of process gradients across die (distance effect).

1.2.4.1 Statistical considerations on circuit analysis and simulation.

Monte Carlo analysis allows the investigation of both process spread and device mismatch. For Monte Carlo simulations purpose, SPICE-parameters are assumed to have a statistical distribution based on the process statistic or measured device matching statistic. A typical Monte Carlo run generates several multivariate random samples of the parameter vector and performs the desired circuit analysis for each sample. Afterwards, the distribution of performance variables can be analyzed by means of descriptive statistics (mean, standard deviation, correlation, higher order moments etc.) as well as by means of graphical statistical tools (histograms, approximate distribution function, scatter plots...). Statistical sensitivity analysis can be performed by correlating device parameters (input variables) with a specific circuit performance (output variables).

There are several advantages of Monte Carlo Analysis compared to a worst case analysis:

- Yield estimation. Since the Monte Carlo analysis imitates the statistical process spread a direct estimation of the yield is obtained using the distribution of the output performance. This helps designers to center their design.
- Correlation. The problem with standard worst case analysis is that worst cases are assumed to lie on corners of the parameter range and therefore can be very pessimistic in terms of probability. Moreover, correlations between device parameters are not included. In Monte Carlo models the most important statistical correlations between device parameters can be taken into account. The final figure of the process spread is therefore much more realistic as the result of a worst case corner analysis.
- Mismatch. Monte Carlo models enable the realistic simulation of device mismatch, where the local variations of device parameters are taken into account. Device mismatch can have considerable impact on specific analog designs (e.g., current-mirrors, offset-voltage of op-amps etc). Mismatch models that are geometry-dependent, enable the optimal sizing of circuit devices based on Monte Carlo simulation results.

There are two different kinds of statistical variation of fabrication parameters:

1. Process variations describe the lot-lot variations, e.g. device parameters on the circuit of the same simulation run will have the same random shift. The statistical modeling of process variations uses the uniform distributions. Process variations are modeled by process variables whose absolute limits correspond to the controlled Manufacturer Acceptance Parameters (MAP) and are reflected in the process parameter document [73].
2. Matching variations describe the local parameter variations of devices on the same circuit in close distance to each other; therefore, it does not model global parameter variations cause by non-uniformities across the wafer (parameter gradients across wafer). Device parameters of the same simulation run and of the same device type will have a different random shift. The manufacturer matching parameters result from matching parameter extraction based on matching measurements for all types of devices [73].

For instance, the Cadence Spectre simulator has a tool to perform Monte Carlo simulations. The implemented tool allows for both combined simulation of process and device mismatch as well as single process and single device mismatch simulations [71].

1.2.4.1.1 Considerations on process variations

Since process variations affects the whole die, it is fully equivalent to consider a device composed by several sub-devices (multiplier parameter M >1), either as a single device or as the composition of several elementary devices. This is not the case for matching variations because gradients will affect large devices whereas will not affect, at first order, composite devices if they are designed using common centroid techniques.

Monte Carlo models for process parameter variations often include important correlations between devices parameters which can introduce significant modifications in results, some of them are listed below:

- Correlation of oxide thickness between all MOS transistors: parameter deltgox.
- Correlation of treshold voltage between all NMOS (parameter delvton) and all PMOS (parameter delvtop) transistors.
- Correlation of effective length between MOS transistors and width of poly resistors: parameter dell.
- Correlation of effective width between MOS transistors and width of diffusion resistors: parameter dew.
- Correlation between bipolar transistor parameters through variation of gummel number.
- Correlation of bipolar junction capacitances between all bipolar transistors: parameters ratiocje, ratiocjs, ratiocjc.
- Correlation of n-well resistance and h_{FE} of CMOS vertical bipolar transistors: parameter gummelpa=log (ratiorw).

Process variations are measured through test structures included on different wafers.

1.2.4.1.2 Considerations on matching variations

Mismatch is the lack of equality in time-independent device parameters caused by random variations in physical quantities. The causes of mismatch can be divided into local and global variations corresponding to the correlation distance of mismatch causing phenomena. The matching parameter of most foundry processes parameters describe the short distance matching: the matching of two identically designed elements located close to each other. Matching variations are measured through test structures included in the same wafer.

Final matching parameters provided by manufacturer are determined by fitting a suitable mismatch model to the measured data (currents or voltages) for each device. A compact model is chosen to keep parameter extraction simple. For example a simplified drain current model (square law model) for MOS transistors in saturation region is taken. Some weakly correlated model parameters are extracted from single transistors of different sizes. The relative differences of the drain currents of transistor pairs are measured at different operating points and varying device sizes. The variance of these measurements is fitted by a drain current mismatch model with least-squares Gauss-Newton-Marquardt methods.

For all other devices, the mismatch parameters are extracted in a similar way.

Problems occur with the Gummel-Poon model for Bipolar Transistors. The saturation current IS shows a strong correlation with most of the model parameters. So only a very small set of "not so strongly" correlated parameters can be found for mismatch parameter extraction.

With regard to simulation we have to make some assumptions on the properties of mismatch generating processes:

- The total mismatch of a parameter is caused by many separate events of the mismatch process.
- Contributions to the mismatch of a parameter can be summed.
- The sum of many independently distributed stochastic variables will tend towards a Gaussian distribution.

As a consequence the values of the parameter are normally distributed with zero means.

As said above mismatch can be divided in:

a) Local Variations. Local parameter variations affect, at most, one single device such a transistor. Some examples of local variations are trapped charges in the gate oxide layer,

oxide granularity or random dimensional variations. For local variations, we assume a correlation distance much smaller than the transistor sizes, thus local variations are not a function of the distance between two devices.

b) Global parameter variations affecting all transistors in a given region are caused by non-uniformities across the wafer. Non-uniformities are related to process distributions e.g. produced by plasma etching and deposition rate variations. Some examples for global variations would be the distributions of gate oxide thickness or sheet resistance. Considering a constant gradient over the wafer in a physical parameter P, the effective parameter of a device results from averaging over its active device area. Best is splitting large area devices in a common centroid layout and to minimize distance between the small devices.

The mismatch between the parameter P of two devices is $\Delta P = P_1 - P_2$, usually the foundry provide the standard deviation of ΔP which is

$$\sigma_{\Delta P}^2 = \sigma_{P1}^2 + \sigma_{P2}^2 - 2\cdot\mathrm{cov}\left(P_1, P_2\right) \qquad (1.1)$$

As said above the matching parameter of most foundry processes parameters describe the short distance matching (local variations) which are independent. Then, considering P_1 and P_2 uncorrelated and of equal variance,

$$\sigma_{\Delta P}^2 = 2\sigma_P^2 \qquad (1.2)$$

The effect of systematic mismatch, produced by deterministic variations, causes a non-zero mean (an offset) in the observed parameter-distributions. Systematic mismatch is generally caused by layout or environmental differences, as for example voltage drop differences in varying device connections or stress gradients caused by packaging. Systematic mismatch can be avoided by appropriate layout techniques. This is very important, since systematic mismatch can exceed the stochastic mismatch considerably.

Marcel Pelgrom [69] presented an area dependence model for the mismatch relative variance of a parameter P:

$$\frac{\sigma^2\left(P_1 - P_2\right)}{\mu_P} = \frac{\sigma^2\left(\Delta P\right)}{\mu_P} = \frac{MP^2}{A_P} \qquad (1.3)$$

where "*MP*" is a device parameter provided by the manufacturer, "A_P" the area of the device and "μ_P" the mean value of parameter P. This relation describes the mismatch variance of many electrical and technological parameters of device pairs. It is the mathematical description of the observation that a large device area is more likely to average the local parameter variations to their zero mean value than a smaller one - a motivation for the design rule to maximize size. According to [69], expression (1.3) is valid for the current gain parameter β, a parameter that scales with device are. On the contrary the variance of the threshold voltage V_{th}, which is a parameter that does not scale with device area, is directly (not relative) proportional to the inverse of the area of the device:

$$\sigma^2\left(V_{th1} - V_{th2}\right) = \sigma^2\left(\Delta V_{th}\right) = \frac{MP^2}{A_P} \qquad (1.4)$$

Ulrich Grünebaum [70] showed that this rule only holds up to a specific size in device area. For larger devices, mismatch becomes even worse, as you arrive at the global parameter variations within one device. To avoid this effect the technique of splitting the large device into an interleaved layout style can be used. Nevertheless, the efficiency of this compensation technique is limited by the non-uniformity of the parameter gradients across the wafer.

This technique and any other combination or division of a single device in several smaller components must be analyzed using stochastic procedures. There two usual ways of combining devices:

a) Addition of device parameters

The device parameters P_i of n elementary devices are added to obtain a parameter P of a compound device. Examples are: resistance of resistors in series or conductances or transconductances in parallel. Let us take two matched parameters P_1 and P_2 of two compound devices. P_1 and P_2 parameters equal to the sum of n elementary equal device parameter, then

$$\begin{aligned} P_1 &= \sum_{i=1}^{n} P_1^i \\ P_2 &= \sum_{i=1}^{n} P_2^i \\ \Delta P &= \sum_{i=1}^{n} P_1^i - \sum_{i=1}^{n} P_2^i = \sum_{i=1}^{n} \left(P_1^i - P_2^i \right) = \sum_{i=1}^{n} \left(\Delta P^i \right) \end{aligned} \tag{1.5}$$

Assuming independent (local) variations for all devices and equal standard deviation $\sigma_{\Delta P^1} = \sigma_{\Delta P^2} = \ldots = \sigma_{\Delta P^i} = \ldots = \sigma_{\Delta P^n}$,

$$\sigma_{\Delta P}^2 = \sum_{i=1}^{n} \sigma_{\Delta P^i}^2 = n\,\sigma_{\Delta P^i}^2 \tag{1.6}$$

From (1.6) and using the Pelgrom's Law, for a parameter that scales with device area:

$$\sigma_{\Delta P}^2 = n\,\sigma_{\Delta Pi}^2 = n \frac{MP^2}{A_{P^i}} \mu_{P^i}^2 = \frac{MP^2}{n \cdot A_{P^i}} n^2 \mu_{P^i}^2 = \frac{MP^2}{A_P} \mu_P^2 \tag{1.7}$$

where "A_{Pi}" is the area of the elementary device and "μ_{Pi}" the mean value of parameter P of the elementary device. According to (1.7) it is equivalent, for a parameter that scales with device area, to consider the compound device either as a composition of n smaller devices of area A_{Pi} and mean parameter value μ_{Pi} using (1.6) to calculate the standard deviation of ΔP or as a single device of area $A_P = n\,A_{Pi}$ and mean parameter value $\mu_P = n\,\mu_{Pi}$.

It is also interesting to note that taking the relative value of the standard deviation defined in (1.6) we obtain

$$\frac{\sigma_{\Delta P}^2}{\mu_P^2} = \frac{\sigma_{\Delta Pi}^2}{n \mu_{P_i}^2} \tag{1.8}$$

which indicates that, since the local parameter variations tend to average, the compound device has smaller relative standard deviation as long as it is only affected by local variations, i.e. an alternative formulation of Pelgrom's Law, provided that the parameter P scales with device area.

b) Addition of inverted device parameters

The inverse of a device parameter P_i of n elementary devices are added to obtain the inverse of parameter of a compound device. Examples are: resistance of resistors in parallel or conductances in series. Let us take two matched parameters P_1 and P_2 of two compound devices: the inverse of P_1 and P_2 parameters equal to the sum of the inverse of n elementary equal device parameter, then

$$\begin{aligned} \frac{1}{P_1} &= \sum_{i=1}^{n} \frac{1}{P_1^i} \\ \frac{1}{P_2} &= \sum_{i=1}^{n} \frac{1}{P_2^i} \\ \Delta P &= P_1 - P_2 = \frac{1}{\sum_{i=1}^{n} \frac{1}{P_1^i}} - \frac{1}{\sum_{i=1}^{n} \frac{1}{P_2^i}} \end{aligned} \tag{1.9}$$

Expression (1.9) is complex. Instead of solving it we consider the inverse of parameter P,

$$P = \frac{1}{B} \qquad P^i = \frac{1}{B^i} \tag{1.10}$$

If we replace P in expression (1.9) by the expression (1.10) we are in the previous case (addition of parameters), therefore

$$\sigma^2_{\Delta B} = n\,\sigma^2_{\Delta B_i} \tag{1.11}$$

According to Theory of error propagation,

$$\sigma^2_{\Delta P} = \left(\frac{\partial P}{\partial B}\right)^2 \sigma^2_{\Delta B} = \left(-\frac{1}{B^2}\right)^2 \sigma^2_{\Delta B} \tag{1.12}$$

As B represents μ_B,

$$\begin{aligned} \frac{\sigma^2_{\Delta P}}{\mu^2_P} &= \frac{\sigma^2_{\Delta B}}{\mu^2_B} \\ \frac{\sigma^2_{\Delta P_i}}{\mu^2_{P_i}} &= \frac{\sigma^2_{\Delta B_i}}{\mu^2_{B_i}} \end{aligned} \tag{1.13}$$

For n equal devices $\mu_P = \frac{\mu_{P_i}}{n}$ and $\mu_B = n\mu_{B_i}$ and using (1.11) and (1.13),

$$\sigma^2_{\Delta P} = \frac{n\,\sigma^2_{\Delta B_i}}{n^2\mu^2_{B_i}}\left(\frac{\mu_{P_i}}{n}\right)^2 = \frac{1}{n^3}\frac{\sigma^2_{\Delta P_i}}{\mu^2_{P_i}}\mu^2_{P_i} = \frac{1}{n^3}\sigma^2_{\Delta P_i} \tag{1.14}$$

Using Pelgrom's law for a parameter P that scales with device area,

$$\sigma^2_{\Delta P} = \frac{1}{n^3}\frac{MP^2}{A_{P_i}}\mu^2_{P_i} = \frac{MP^2}{nA_{P_i}}\frac{\mu_{P_i}}{n^2} = \frac{MP^2}{A_P}\mu_P \tag{1.15}$$

where "A_{Pi}" is the area of the elementary device and "μ_{Pi}" the mean value of parameter P of the elementary device and "A_P" is the area of the compound device and "μ_p" the mean value of parameter P in the compound device. According to (1.15) it is equivalent, for a parameter that scales with device area, to consider the compound device either as a composition of n smaller devices of area A_{Pi} and mean parameter value μ_{Pi} using (1.14) to find the standard deviation of P or as a single device of area $A_P = n\,A_{Pi}$ and mean parameter value $\mu_P = \mu_{Pi}/n$.

1.2.5 The design cycle

Following the introduction of the organisation of Multi-Wafer-Projects (MWPs) at the beginning of the eighties, the development of ASICs in the high-energy physics community deeply impacted the way HEP electronics instrumentation is conceived. Now prototyping of HEP chips follows the schedule of MWPs.

Typically an ASIC for HEP instrumentation needs several iterations (usually between 2 and 5) to be accepted for production. Although, in some case some cells or even almost completes design are re-used. Production quantities range from a few tens to millions for chips used in several experiments. Nevertheless typical, values are thousands or tens of thousands.

Neglecting the time needed for design and test, each chip iteration in MWPs takes between 3 and 4 months and has to be scheduled according to the available dates (between 1 and 8 runs per year depending on the technology). Thus, first design iterations may take about a year if design is completely new and has to be fully characterized whereas latest ones may take only the production time plus a few weeks of test. It is important also to take into account that actually most chips for

HEP should be qualified for radiation, and this means that a test in a proper irradiation facility has to be scheduled.

1.3 Work organization

This thesis is organized a follows:

1.3.1 Chapter 2: Detector resolution and electronic noise

In chapter 2 the factors that determine the resolution of a detector are analyzed. The methods to analyze the electronic noise are summarized. A lot of attention is paid on the description of time variant systems. The concepts presented on this chapter will be extensively employed in subsequent sections.

1.3.2 Chapter 3: SPD signal processing

In chapter 3 the signal generation in the SPD of the LHCb calorimeter and the resulting requirements for the front end electronics are outlined. These requirements are described following the term definition given in this introduction. Those general requirements and specifications of all LHCb electronics system that have an impact on this design are summarized. Finally, an architecture for the front end is proposed, taking into account these requirements, the choice of a technology, the ASIC contents and partitioning, the packaging and the power consumption.

1.3.3 Chapter 4: Custom design of blocs

In chapter 4 the circuit design of each block of the chip is presented. Calculations are compared with computer simulations for all the relevant parameters. The design iterations of the IC are summarized. The IC floorplan and some relevant details of the layout are discussed.

1.3.4 Chapter 5: Analysis of the resolution of the ASD

The factors that will determine the resolution of the ASD are analyzed. First of all the intrinsic noise of the circuit is computed, both through hand calculations and simulations. Then the offset is also analyzed as it may determine “available” resolution of the system. Finally, the PSRR of the sensitive analogue input blocks is evaluated. Monte Carlo simulations are compared with hand calculations.

1.3.5 Chapter 6: Experimental results

Experimental results of the individual blocks and of the full system are reported in chapter 5. These results include test measurements at home laboratory and measurements in test beam facilities at CERN (Geneva) and irradiation facilities at GANIL (Caen).

1.3.6 Chapter 7: Conclusions

Conclusions about the performances of the architecture and of the implementation are presented in chapter 7. Possible future lines of development of the presented system are discussed also.

2 Resolution and noise of the front end electronics

Nearly all the detectors[g] have the ability not only to indicate by an output pulse the passage of an ionizing particle, but also to allow the determination of its energy from the amount of charge produced in the pulse. The energy deposited by ionizing particles varies from event to event and its statistics is typically described by the Landau-Varilov distribution, except for very thin detectors [74].

Even if the deposited energy is fixed the signal of the detectors has statiscal fluctuations. A detector response to a monoenergetic radiation has a certain linewidth and follows a probability distribution, which is called *response function*. The ***energy resolution (R)*** of a detector is defined as the full width at half maximum (FWHM) divided by the location of the peak centroid (H_0) of the response function [8]:

$$R = \frac{FWHM}{H_0} \qquad (2.1)$$

It should be clear that the smaller the figure for the energy resolution, the better the detector will be able to distinguish between two radiations whose energies lie near each other.

There are a number of potential sources of fluctuation in the response of a given detector that cause fluctuations of the response to a monoenergetic radiation. These include drift of the operating characteristics of the detector during the course of the measurements, sources of random noise within the detector and instrumentation system, and statistical noise arising from the discrete nature of the signal itself (noise in the signal). The third source is in some sense the most important because it represents an irreducible minimum amount of fluctuation that will always be present in the detector signal no matter how perfect the remainder of the system is made. In a wide category of detector applications, the statistical noise represents the dominant source of fluctuation in the signal and thus sets an important limit on detector performance.

The statistical noise arises from the fact that the charge Q generated within the detector by a quantum radiation is not a continuous variable but instead represents a discrete number of charge carriers and this number fluctuates from event to event. For example, in an ion chamber the charge carriers are the ion pairs produced by the passage of the charged particle through the chamber, whereas in a scintillation counter they are the number of electrons at the anode which are obtained by multiplication of the electrons (called also photoelectrons) collected from the photocathode of the photomultiplier tube [9]. A scintillator counter is composed by a scintillator, a light guide and a photon detector, usually a photomultiplier. The photons produced by an ionizing radiation in the scintillator are transmitted to the photon detector where they are converted to electrons and multiplied. Therefore, the fluctuations of two statistical processes, the ionization in the scintillator and the multiplication in the photomultiplier, determine the statistics of the charge that is measured at the output of the scintillator counter. In all cases, gas chamber or scintillator counter, the number of carriers is discrete and subject to random fluctuation from event to event even though the same amount of energy is deposited in the detector.

An estimate can be made of the amount of inherent fluctuation by assuming that the formation of each charge carrier is Poisson process. Under this assumption, if a total number N of charge carriers is

[g] The term detector has two different meanings. On the one hand, it is an elementary device to detect the particle radiation; for instance a gas chamber, a scintillator counter or a silicon sensor. On the other hand, it stands for the complex apparatus of a particle or nuclear physics experiment, a complex system involving many elementary detectors. Here we are using the term in his first sense.

generated on the average, one would expect a standard deviation of $\sqrt{N}$ to characterize the inherent statistical fluctuations in that number. If this were the only source of fluctuation in the signal, the response function should have a Gaussian shape, because *N* is typically a large number. The standard deviation σ of the Gaussian determines the FWHM of this response function through the relation $FWHM=2.35\cdot\sigma$.

The response of most detectors is approximately linear, so that the average pulse amplitude $H_0=KN$, where *K* is a proportionality constant. The standard deviation σ of the peak in the pulse height spectrum is $\sigma = K\sqrt{N}$ and its FWHM is $2,35K\sqrt{N}$. We then would calculate a limiting resolution *R* due only to statistical fluctuations in the number of charge carriers as

$$R\big|_{Poisson\ limit} \equiv \frac{\sigma}{H_0} = \frac{K\sqrt{N}}{KN} = \frac{1}{\sqrt{N}} \qquad (2.2)$$

This is the usual definition of resolution in particle physic experiments; in nuclear and medical field the FWHM is preferred,

$$R\big|_{Poisson\ limit} \equiv \frac{FWHM}{H_0} = \frac{2,35K\sqrt{N}}{KN} = \frac{2,35}{\sqrt{N}} \qquad (2.3)$$

Note that this limiting value of R depends only on the number of charge carriers *N*, and the resolution (*R* will decrease) as *N* is increased. The great popularity of semiconductor detectors stems from the fact that a very large number of charge carriers are generated in these devices per unit length lost by incident radiation. Furthermore, the assumption of Poisson statistics is not correct for such detectors.

It is observed that the resolution of many detectors is actually smaller than the calculated from Poisson statistics. The theory underlying Poissonian statistics implies that it should hold only if a very small part of the deposited energy went on average into carrier production, and this is not the case for semiconductors detectors where the energy deposited to produce a hole-electron pair is only three times the band gap energy. Remaining energy is taken up by the semiconductor lattice, statistical fluctuations of the fraction of energy taken by the lattice produces the linewidth[h]. The fact that a significant fraction of the deposited energy goes to carrier production means statistically that ionization events are not independent so that Poisson statistics is not applicable. A similar phenomenon occurs in gas detectors. The ***Fano factor (F)*** [75] has been introduced in an attempt to quantify the departure of the observed statistical fluctuations in the number of charge carriers from pure Poisson statistics and is defined as

$$F \equiv \frac{observed\ \text{variance in}\ N}{Poisson\ predicted\ (=N)} \qquad (2.4)$$

Because the variance is given by σ^2, the equivalent expression to (2.3) is now

$$R\big|_{Statistical\ limit} \equiv \frac{K\sqrt{N}\sqrt{F}}{KN} = \sqrt{\frac{F}{N}} \qquad (2.5)$$

Theories predicting the value of the Fano factor have not been particularly successful, and indeed experimental determinations of *F* have shown considerable variation. However, both for silicon and germanium the currently accepted values are around 0.1, In the case of proportional detectors and gas chambers, there has been a wide range of values of *F* suggested for various gases, but a number have *F* around 0.17.

[h] If all of the energy lost by ionizing radiation in a semiconductor were spent breaking covalent bonds in the detector's sensitive volume, no fluctuations would occur in the number of electron-hole pairs produced by ionizing radiation of a given energy.

We found for scintillation counters that theory and experiment agreed reasonably well without allowing for any Fano factor reduction (that is F=1), but this could possibly be the result of a Fano factor actually les than unity balanced out by some line broadening due to scintillator imperfections. Indeed, if the fluctuations of the electron multiplication in the photomultiplier or other photo-detectors such as avalanche photodiodes (APDs) are taken into account, at least two statiscal processes are convoluted: the ionization in the scintillator and the multiplication in the photo-detector. Then, the variance of the overall process can be larger than the one given by a Poisson process. The amplification process introduces a widening of the spread in the distribution ([9], [76]). The "widening" factor is called ***Excess Noise Factor (ENF)*** and is larger than unit. Typically for photomultipliers is between 1.2 and 2. Thus for a scintillator counter, the relationship between the mean (*H0*) and sigma on the spectra does not follow a Poisson distribution. Taking into account the photon detection efficiency (*PDE*)[i] of the photodetector, the resolution is function of the number of photoelectrons reaching the multiplication chain and of the ENF,

$$R\big|_{Statistical\ \lim it} \equiv \frac{\sigma}{H_0} = \frac{K\sqrt{N}\sqrt{ENF}}{KNQE} = \sqrt{\frac{ENF}{N_{phe}}} \qquad (2.6)$$

In addition to the fluctuations in ionization, a number of external factors can affect the overall resolution of a detector. This include the effects from the associated electronics such as noise, drifts, etc. To understand the way of these factors are combined, the theory of propagation of errors can be used. To simplify the algebra two variables are used, the extension to more variables is obvious. Consider a random variable U which is function of other random variables X and Y: $U = f(X,Y)$. The square root of the variances of the respective distributions are σ_U, σ_X and σ_Y. We would like then to calculate the standard deviation σ_U as a function of σ_X and σ_Y. The variance σ_U^2 can be defined as:

$$\sigma_U^2 = E\left[\left(U-\overline{U}\right)^2\right] \qquad (2.7)$$

To first order, the mean $\overline{U}$ may be approximated by $\overline{U} = f\left(\overline{X},\overline{Y}\right)$. This can be shown by expanding $f(X,Y)$ about $\left(\overline{X},\overline{Y}\right)$. Now, to express the deviation of U in terms of the deviation of X and Y, let us expand $\left(U-\overline{U}\right)$ to first order:

$$\left(U-\overline{U}\right) \simeq \left(X-\overline{X}\right)\frac{\partial f}{\partial x}\bigg|_{\overline{X}} + \left(Y-\overline{Y}\right)\frac{\partial f}{\partial y}\bigg|_{\overline{Y}} \qquad (2.8)$$

where the partial derivatives are evaluated at the mean values. Squaring (2.8) and substituting in (2.7) then yields

$$E\left[\left(U-\overline{U}\right)^2\right] \simeq E\left[\left(X-\overline{X}\right)^2\left(\frac{\partial f}{\partial x}\right)^2 + \left(Y-\overline{Y}\right)^2\left(\frac{\partial f}{\partial y}\right)^2 + 2\left(X-\overline{X}\right)\left(Y-\overline{Y}\right)\frac{\partial f}{\partial x}\frac{\partial f}{\partial y}\right] \qquad (2.9)$$

Now taking the expectation value of each separate term and making use of the definition of the variance and the covariance, we find

$$\sigma_U^2 \simeq \left(\frac{\partial f}{\partial x}\right)^2 \sigma_X^2 + \left(\frac{\partial f}{\partial y}\right)^2 \sigma_Y^2 + 2\,\mathrm{cov}(X,Y)\frac{\partial f}{\partial x}\frac{\partial f}{\partial y} \qquad (2.10)$$

[i] PDE is the ratio between the number of photons arriving to the photo-detector and the number of photoelectrons generated. It includes several factors such as the probability that an incident photon generates a carrier, i.e. the quantum efficiency (QE), the collection efficiency (CE) in photmotultipliers or geometrical factors such as the fill factor on silicon photodetectors. The QE depends on the wavelength of the incident light.

In our case the random variable corresponding to the detector resolution (E_{DET}) is added to the other fluctuations like noise (E_{NOISE}), jitter (E_{JITTER}) in synchronous control signals or drifts (E_{DRIFT}): $E_T = E_{DET} + E_{NOISE} + E_{DRIFT} + E_{JITTER} + ...$ Using this and taking into account that all the sources of fluctuations are in general independent:

$$\sigma_{E_T}^2 = \sigma_{E_{DET}}^2 + \sigma_{E_{NOISE}}^2 + \sigma_{E_{DRIFT}}^2 + \sigma_{E_{JITTER}}^2 + ... \qquad (2.11)$$

The Central Limit Theorem [77] and of the Probability Theory states that the sum of *n* independent random variables all having the same probability density function, and hence equal averages μ_X and equal variances σ_X^2, follows a normal distribution for large *n*, with an average $n\mu_X$ and a variance $n\sigma_X^2$, if σ_X^2 exists. In a more general formulation of the theorem the assumption of identical distributions can be substantially weakened. For that reason most fluctuating quantities such noise and the other terms in (2.11), which are combination of lot of individual processes, follow a normal distribution, even if individual processes are characterized by distributions of different shape. Therefore the relation $FWHM=2.35\sigma$ of the Gaussian distribution is valid in general and we can write:

$$FWHM_{E_T}^2 = FWHM_{E_{DET}}^2 + FWHM_{E_{NOISE}}^2 + FWHM_{E_{DRIFT}}^2 + FWHM_{E_{JITTER}}^2 + \ldots \quad (2.12)$$

Next subsections review the basic methods for noise analysis, the sources of electronics noise and the specific noise characteristics of the preamplifiers for detectors. Finally some considerations on drifts, pickups and environmental noise are summarized.

2.1 Noise Description

Noise is a random signal and therefore cannot be analyzed by common methods of circuit theory. Noise, like any random signal, can be described in different domains: amplitude, time, frequency. We will use the term definition given in [79]. Noise will be considered as a stationary and ergodic stochastic process [81] unless it is specified. For ergodic process temporal averages are the same as probabilistic averages and moments (like variance). Ergodicity implies stationarity, but stationarity does not imply ergodicity.

The assumption of stationarity fails when the output response of a time varying network to either stationary or non-stationary random input signal is considered (see section 11.7 in [82]), analysis of such systems will be considered in sections 2.3 and 2.6.5.

The *mean-square value*, or intensity, of signal *x(t)* is the average of the squares of the instantaneous values of the signal,

$$\Psi_x^2 \doteq \lim_{T\to\infty} \frac{1}{T}\int_0^T x^2(t)\,dt \qquad (2.13)$$

If only a small number of values of a random signal *x(t)* are considered, that is, if T is not very long, then different calculations of Ψ_x^2 yield different results. Signal *x(t)* is a particular sample function of the stochastic process.

The mean-square value can be separated into a time-invariant part and a time varying part. The time-invariant o static part is the square of the *signal averag*e or *mean value*,

$$\mu_x \doteq \lim_{T\to\infty} \frac{1}{T}\int_0^T x(t)\,dt \qquad (2.14)$$

The time-varying or dynamic part of the mean-square value is the *signal variance*, which is defined as the mean-square of *x(t)* about is mean value,

$$\sigma_x^2 \doteq \lim_{T\to\infty}\frac{1}{T}\int_0^T \left[x(t)-\mu_x\right]^2 dt \qquad (2.15)$$

It follows that

$$\psi_x^2 = \mu_x^2 + \sigma_X^2 \qquad (2.16)$$

It is also possible to define a time autocorrelation function for a particular sample function as,

$$R_x(\tau) = \lim_{T\to\infty}\frac{1}{T}\int_0^T x(t)x(t+\tau)dt \qquad (2.17)$$

It is readily seen that for $\tau=0$, the autocorrelation function is equal to the mean-square value of the process.

The power dissipated by a random voltage on a resistor is proportional to the mean-square voltage. Hence, the signal intensity is also termed *signal power*. Its units are volts squared (V^2), but if a *1* Ω load is implicitly assumed, the watt unit (*W*) can be used instead. The mean value for electronic noise (except for quantization noise) is zero. Therefore, the noise variance equals the noise power. The standard deviation then equals the root-mean-square voltage.

Rather different signals can convey the same power. Large amplitude during a short time, for example, can yield the same power as smaller amplitude during a longer time. The amplitude distribution of a random signal is described by the *probability density function* (PDF), *p(x)* defined as

$$p(x) \doteq \lim_{\Delta x\to 0}\frac{\Pr ob\left[x < x(t) < x+\Delta x\right]}{\Delta x} = \lim_{\Delta x\to 0}\frac{1}{\Delta x}\left[\lim_{T\to\infty}\frac{T_x}{T}\right] \qquad (2.18)$$

where T_x is the amount of time in which *x(t)* falls inside the amplitude interval from *x* to $x+\Delta x$. Therefore, the PDF gives the probability that the signal amplitude at any arbitrary moment lies inside a given amplitude range.

Very often, electronic noise has a Gaussian, or normal, probability density function because it results from a large number of random, independent and similar events (Central Limit Theorem). This means that is PDF is bell-shaped with zero mean value:

$$p(x) = \frac{1}{\sigma_X\sqrt{2\pi}}e^{-\frac{(x-\mu_X)^2}{2\sigma_X^2}} = \frac{1}{\sigma_X\sqrt{2\pi}}e^{-\frac{x^2}{2\sigma_X^2}} \qquad (2.19)$$

The PDF does not take into account the time when the different amplitudes of random signal appear. Therefore, very different amplitude sequences (or waveforms) can lead to the same Gaussian distribution. In order to better characterize a random signal, one must consider the distribution of its power in different frequency bands. The *power spectral densit*y (PSD) of a random signal *x(t)* is

$$G_{xx}(f) \doteq \lim_{\Delta f\to 0}\frac{\Psi_x^2(f,\Delta f)}{\Delta f} = \lim_{\Delta f\to 0}\frac{1}{\Delta f}\left[\lim_{T\to\infty}\frac{1}{T}\int_0^T x^2(t,f,\Delta f)\,dt\right] \qquad (2.20)$$

where $\Psi_x^2(f,\Delta f)$ is the signal power in the frequency band form *f* to $f+\Delta f$, and $x(t,f,\Delta f)$ is that part of *x(t)* contributing to power in the frequency band from *f* to $f+\Delta f$. A random signal having the same power density at all frequencies in a given frequency band is said to have a *white spectrum* in that band. The power of a signal can be obtained by integrating its PSD over the entire frequency range.

The PSD does not completely specify a signal either because signals with different phase can have the same spectrum. However, signal phase is not considered in noise analysis. Gaussian noise is completely described by its variance and power spectral density.

The Wiener-Khintchine theorem ([83] or [84]) provides an important relationship between the autocorrelation function and the PSD of a random process. For a stationary random process the PSD is the Fourier transform of the autocorrelation function

$$G_{xx}(\omega) = \int_{-\infty}^{\infty} R_x(\tau) e^{-j\omega\tau} d\tau = F\{R_x(\tau)\} \qquad (2.21)$$

For non-stationary processes both the PSD and the autocorrelation function (and time averages) depend on the absolute time [84], thus Wiener-Khintchine relationship becomes,

$$G_{xx}(\omega, t) = F\{R_x(t, \tau)\} \qquad (2.22)$$

A detailed analysis of the probability structure of non-stationary process can be found on [82] and [81], and some relevant examples, for instance the Wiener-Levy process (random walk), are analyzed in [84].

2.2 Noise Sources

The main sources of this section are Chapter 11 of [79] and of [66], and [77].

2.2.1 Thermal Noise

The most common noise sources in electronic circuits, and in any medium that dissipates energy, are the random fluctuations at the atomic and molecular level because of the thermal energy in the medium. Random charge movements yield instantaneous differences in voltage between any two points in every conductor, regardless of the material, even in the absence of any connection, or coupling, from the conductor to any power supply. The PDF of thermal noise is Gaussian, because it is results of many independent, similar events.

Thermal noise in conductors was first measured by J. N. Johnson [85] and theoretically analyzed by H. Nyquist [86] in 1927-28. Hence, its other names are Johnson noise or Nyquist noise. Using thermodynamics and statistical mechanics [86], Nyquist determined that when two conductors are connected by means of a non-dissipative transmission line, the average power transferred by each conductor is

$$N_t = kTB \qquad (2.23)$$

where $k=1.38 \times 10\text{-}23$ J/K is Boltzmann's constant, T is the absolute temperature for the conductor and B is the noise bandwidth which is related to the bandwidth of the system (the range of frequencies that are significant in the PSD of the noise signal depend on the frequency response of the system, see section 2.3). Thermal noise is white. A larger bandwidth implies larger noise, but equation (2.23) is a simplification of a more general expression of statiscal mechanics and this simplification is not valid above few THz [86].

Expression (2.23) is by definition equal to the *available noise power* from a resistive source (a conductor). In terms of circuit theory, the *available noise power* is the power that can be delivered to a resistive load R_L equal in value to the source resistance R_S. Therefore, if in Figure 2-1a the load is noiseless and $R_S=R_L$ then

$$N_t = \frac{E_{no}^2}{R_L} = \frac{\left(E_t/2\right)^2}{R_s} = kTB$$

and thus,

$$\sigma^2 \doteq \psi^2 \doteq E_t^2 = 4kTBR \qquad (2.24)$$

where $R=R_S$ is the real part of the conductors impedance (the conductor can have stray capacitance and inductance). E_t^2 is the *thermal noise power*[j] and E_t is the *thermal noise voltage*, both measured in root mean square (r.m.s) units. Analogously, the thermal noise from a resistive current source can be modeled as a current source (Norton equivalent), Figure 2-1b, in which case

$$I_t^2 = \frac{4kTB}{R} \qquad (2.25)$$

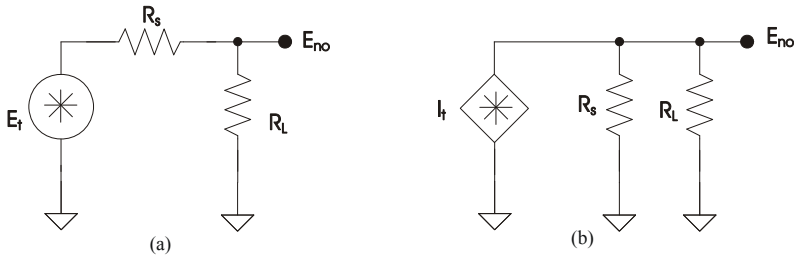

Figure 2-1. Circuit for determining (a) the thermal noise voltage or (B) the thermal noise current from a conductor with resistance RS. Figure taken from [79].

The power spectral density for thermal noise is

$$S_t \doteq \frac{E_t^2}{B} = 4kTR \qquad (2.26)$$

and its unit is volts squared divided by hertz $\left(\mathrm{V}^2/\mathrm{Hz}\right)$. The square root of S_t is usually termed *noise voltage density* and its unit is volts divided by the square root of hertz $\left(\mathrm{V}/\sqrt{\mathrm{Hz}}\right)$. We will denote it e_t, so that $S_t \equiv e_t^2$.

The thermal noise voltage for any impedance Z can be calculated by substituting *Re[Z]* for *R* ([86]) in (2.24) and taking the square root.

2.2.2 Shot Noise

Shot noise is always associated with a direct current flow and is present in diodes, MOS transistors, and bipolar transistors. Electric currents are made of individual carriers. When there is a current across a potential barrier, the passage of each carrier across the junction is modeled as a random event. The number of charge carriers crossing the barrier during each unit of time is random because each carrier is independent ([77], [84]). These random current fluctuations constitute the shot noise current, whose r.m.s value is

$$I_{sh} = \sqrt{2qI_{dc}B} \qquad (2.27)$$

where $q=1.602\times10^{-19}$ *C* is the electron charge, I_{dc} is the average current and B is the noise bandwidth. The total current will therefore be

$$i(t) = I_{dc} + i_{sh}(t) \qquad (2.28)$$

where $i_{sh}(t)$ is the random shot noise, for which there is no analytical expression, but whose r.m.s value is I_{sh}.

The power spectral density for shot noise is

[j] Note that thermal noise power E_t^2 is precisely speaking a square voltage and not a power (its units are V^2 and not *W),* nevertheless it is usually referred as noise power because is propotional ($1/R$) to the power. Similar consideration is valid for noise square current I_t^2.

$$S_{sh} \doteq \frac{I_{sh}^2}{B} = 2qI_{dc} \qquad (2.29)$$

whose unit is amperes squared divided by hertz $\left(A^2/Hz\right)$. Hence, shot noise is white, although, at very high frequency charge movements are correlated because of collisions and PSD decreases. Equation (2.29) is valid until frequency becomes comparable to $1/\tau$, where τ is the carrier transit time through the depletion region. For most practical electronic devices τ is extremely small and (2.29) is accurate well in the gigahertz region.

Conductors do not have shot noise because there are no potential barriers in them and electrons movements are correlated. The PDF of shot noise is Gaussian, because it is results of many independent, similar events.

2.2.3 Flicker or *1/f* noise

When there is a current through either ordinary resistors or semiconductor junctions, the noise generate is larger than the thermal noise predicted for conductors or the shot noise predicted for semiconductor junctions. This is found in all active devices, as well as in some discrete passive elements such as carbon resistors. The mechanisms contributing the additional noise are unknown (although are supposed to be caused by traps associated with contamination and crystal defects) but their properties have drawn much attention: its PDF is usually Gaussian and its PSD is inversely proportional to the frequency (often it is called *low frequency noise*) according to

$$S_f(f) = i_f^2(f) = K_f \frac{I_{dc}^a}{f^b} \qquad \left[A^2/Hz\right] \qquad (2.30)$$

where I_{dc} is the direct current flowing through the noisy device, K_f is a characteristic constant of a particular device, exponent a is a constant in the range 0.5 to 2 and exponent b is constant about unity. Flicker noise only exists in association with a direct current. Thus, in the case of carbon resistors, no flicker noise is present until a direct current is passed through the resistor. The constant K_f not only varies by orders of magnitude from one device type to the next, but it can also vary widely for different transistors or integrated circuits from the same process wafer. This is due to the dependence of flicker noise on contamination and crystal imperfections. Thus, the typical value of K_f is determined from measurements.

This noise is also termed *excess noise*, because it is observed to add to thermal or shot noise, *flicker noise* in vacuum tubes, *contact noise* in carbon composition resistors, and *semiconductor noise*. The frequency dependence of S_f means that this noise is not white, and has led to the term *pink noise*.

The mean-square current of the low frequency noise depends not only on the bandwidth, like thermal and shot noise, but also on the frequency. For $b=1$ and a bandwidth from f_L to f_H,

$$I_t^2(f) \equiv \int_{f_L}^{f_H} i_f^2(f)df = K_f I_{dc}^a \int_{f_L}^{f_H} \frac{1}{f^1}df = K_f I_{dc}^a \ln\left(\frac{f_H}{f_L}\right) \qquad (2.31)$$

which means that there is the same noise power in each frequency decade. A PSD inversely proportional to the frequency seems to suggest “infinite” noise at dc. This is not the case, “zero” frequency does not exist: any electronic equipment is turned on (and off) at some moment. For illustration, in 30 years the noise current increases only three times compared with the 0.1 Hz to 1 Hz band. Furthermore, (2.30) indicates that the PSD increases when the frequency decreases, but noise depend on the bandwidth considered, and at low frequencies the bandwidth is very narrow (to consider years in time means a very small increase in bandwidth).

The real problem with *1/f* noise is that it starts to be noticeable at frequencies well inside the bandwidth of many instrumentation signals, sometimes even at 1kHz. Then, at low frequencies *1/f* noise dominates over other noise sources.

2.2.4 Burst Noise (Popcorn Noise)

This is another type of low-frequency noise found in some integrated circuits and discrete transistors. The source of this noise is not fully understood, although it has been shown to be related to the presence of heavy-metal ion contamination. Gold-dope device show very high levels of burst noise.

Burst noise is so named because an oscilloscope trace of this type of noise shows bursts of noise on a number (two or more) of discrete levels. Thus, the PDF of burst noise is not Gaussian; it presents a number (two or more) of peaks corresponding to the discrete levels. The repetition rate of the noise pulses is usually in the audio frequency range and produces a popping sound when played through a loudspeaker. This has led to the name popcorn noise for this phenomenon.

The PSD of burst noise can be shown to be of the form

$$S_b(f) = i_b^2(f) = K_b \frac{I_{dc}^c}{1+\left(\frac{f}{f_c}\right)^2} \qquad \left[A^2/Hz\right] \qquad (2.32)$$

where K_b is a constant for a particular device, I_{dc} is the direct current flowing through the device, exponent c is a constant in the range 0.5 to 2 and f_c is the particular frequency for a given process. Burst noise processes often occur with multiple time constants, and this gives rise to several bumps in the spectrum (several f_c). Nowadays, devices are rarely affected by burst noise.

2.2.5 Avalanche noise

This is a form of noise produced by Zener or avalanche breakdown in a pn junction. In avalanche breakdown, holes and electrons in the depletion region of reverse-biased pn junction acquire sufficient energy to create hole-electron pairs by colliding with silicon atoms. This process is cumulative, resulting in the production of a random series of large noise pikes. The noise is always associated with direct current flow, and the noise is much greater than the shot noise. This is because single carrier can start avalanching process that results in the production of a current burst containing many carriers moving together. The total noise is the sum of a number of random burst of this type. The most common situation where avalanche noise is a problem occurs when Zener diodes are used in the circuit. The spectral density of the noise is approximately flat, but the amplitude distribution is generally non-Gaussian.

2.3 Response of Linear Systems to Random Inputs

If a deterministic signal *x(t)* is applied to the input of a (noiseless) linear time-invariant system whose response to a unit area impulse is *h(t)*, then the output is *y(t)*, such that *Y(f)=H(f)X(f)*, where variables in capital letters designate the respective transforms of time-domain signals. If the input signal is random instead, then the input-output relationship is established between the respective power spectral densities ([79] and [87]),

$$G_{yy}(f) = \left|H(f)\right|^2 G_{xx}(f) \qquad (2.33)$$

if $G_{xx}(f)$ is a power signal, *H(f)* is the power gain. Therefore, if a noise source with PSD $G_{xx}(f)$ is connected to this system, the output noise power (mean square) will be

$$\psi_y^2 \doteq \int_0^\infty G_{yy}(f)\,df = \int_0^\infty |H(f)|^2 G_{xx}(f)\,df \qquad (2.34)$$

In general the square voltage or current gains *G(f)* are used instead of the power gain *H(f)*. Remember that indeed thermal noise power is a square voltage and shot noise power is a square current. Thus if a voltage noise source with PSD $G_{xx}(f) = S_x(f) = e_x^2(f)$ is connected to a system with voltage gain *G(f)* the output square noise voltage is

$$\sigma^2 \doteq \psi_y^2 \doteq E_y^2 \doteq \int_0^\infty G_{yy}(f)\,df = \int_0^\infty |G(f)|^2 S_x(f)\,df = \int_0^\infty |G(f)|^2 e_x^2(f)\,df \qquad (2.35)$$

and if a voltage noise source with PSD $G_{xx}(f) = S_x(f) = i_x^2(f)$ is connected to a system with current gain *G(f)* the output square noise current is

$$\sigma^2 \doteq \psi_y^2 \doteq I_y^2 \doteq \int_0^\infty G_{yy}(f)\,df = \int_0^\infty |G(f)|^2 S_x(f)\,df = \int_0^\infty |G(f)|^2 i_x^2(f)\,df \qquad (2.36)$$

The *noise bandwidth (B)* of a system *H(f)* is the frequency span of a rectangular power gain curve yielding the same output power as the actual system. If the input is white noise, for the actual system we have,

$$\psi_y^2 \doteq G_{xx} \int_0^\infty |G(f)|^2\,df \qquad (2.37)$$

whereas for the system with rectangular power gain,

$$\psi_y^2 \doteq G_{xx} |G_0|^2 B \qquad (2.38)$$

From these two equations,

$$B = \frac{1}{|G_0|^2} \int_0^\infty |G(f)|^2\,df \qquad (2.39)$$

which means that the area under the actual power-gain curve equals that of a theoretical rectangular power-gain curve with width *B* and height of a convenient value $|G_0|^2$. For instance, the noise bandwidth of low pass filter with corner frequency f_c is $B = \frac{\pi}{2} f_c$.

Noise bandwidth cannot be defined for *1/f* noise (or burst noise) because its power spectral density depends on the frequency (it is not white noise), and it is not possible to take it outside the integral (2.34).

Analysis frequency domain is usually preferred in circuit analysis and in instrumentation fields due to the simplification in the analysis introduced by Fourier or Laplace transforms. Nevertheless, it is also possible to determine the response of a linear system to random inputs using time domain techniques. The procedure is analogous to the computation of the output of a deterministic system using the convolution method. As shown in section 8-3 in [83], the value of the mean square of the output is

$$\psi_y^2 = \int_0^\infty d\tau_1 \int_0^\infty R_x(\tau_2 - \tau_1) h(\tau_1) h(\tau_2)\,d\tau_2 \qquad (2.40)$$

For the particular case of white noise with $R_x(\tau) = \frac{N_o}{2}\delta(\tau)$, where $N_o/2$ is the two-sided spectral density of the white noise, (2.40) becomes

$$\psi_y^2 = \frac{N_o}{2} \int_0^\infty h^2(\tau)\,d\tau \qquad (2.41)$$

Indeed, the fundamental expression (2.33) for frequency domain analysis is derived using (2.40) and the Wiener-Khintchine theorem (2.21), (see [81], [82], [83] and [87]).

Only time invariant circuits have been considered so far. However, the discussion on noise description and analysis can be generalized for time variant circuits and non stationary random processes [82]. A more detailed discussion can be found in [82], [88], [89] and [90]; we will only present here some relevant concepts.

In [82] and [88] the time varying transfer function is defined as, with $\omega=2\pi f$,

$$H(j\omega,t)=e^{-j\omega t}\int_{-\infty}^{\infty}h(t_i,t)e^{-j2\pi ft_i}dt_i=e^{-j\omega t}F\{h(t_i,t)\} \qquad (2.42)$$

where $h(t_i,t)$ is the so called time variant impulse response or weighting function (in the original work [88] it was written as $W(\tau=t_i,t)$). As in the case of time invariant networks, the impulse response represents the output response at a time t of a given system to an impulse applied at $t= t_i$, $\delta(t- t_i)$. For time invariant circuits, however, only the difference $t- t_i=\tau$ is relevant, then the response to $\delta(t- t_i)$ is just $h(t- t_i)=h(\tau)$ for any τ, then the transfer function does not depend on t: $H(j\omega)$.

The Time Varying Transfer Function $H(j\omega,t)$ is a function of $j\omega$ involving t as a parameter. In [88] and [89] it is shown that $H(j\omega,t)$ represents a natural extension of the notion of the system function of a fixed network $H(j\omega)$, thus it possesses many of the fundamental properties of $H(j\omega)$ and can also be used in similar way to obtain steady-state as well the transient response of a variable network to any prescribed input, whether deterministic or random. For instance, response to deterministic signals can be obtained using the inverse Fourier transform (F^{-1}): $y(t)=F^{-1}\{H(j\omega,t)X(j\omega)\}$. The mean square of the output signal produced by an input Gaussian and stationary noise source is given by

$$\psi_y^2(t)\doteq\int_0^{\infty}G_{yy}(f,t)df=\int_0^{\infty}\left|H(j\omega,t)\right|^2G_{xx}(f)df \qquad (2.43)$$

Note that the mean square value of the output depends on time. Non-stationary random input signals can be also analyzed [82] using the concept of Bi-Frequency System Function which is the Fourier transform of $H(j\omega,t)e^{j\omega t}$, i.e. the double Fourier transform of $h(\tau,t)$.

In [90] it is shown that time varying filters may be characterized in a symmetrical manner in time and frequency variables by arranging system functions in dual pairs. These system functions include the Time Varying Transfer Function and the Bi-Frequency System Function.

It is important to point out that much of the random processes are non stationary when viewed on large enough time-scale. Nevertheless, it is often possible to force the process to be at least piecewise stationary for measurement and analysis purposes [82].

2.4 Noise Calculations: Input Equivalent Noise

Electronic circuits consisting of several components will include many noise sources. The overall noise must be calculated by considering that power from different sources adds together as seen in (2.10) for the combination $U=f(X,Y)$ of two random processes. Replacing the sensitivity by the gain or transfer function between a given noise source and a voltage or current in a node or branch defined as output:

$$S_o^2(f)\simeq\left|G_{S_{X_1}}(f)\right|^2S_{X_1}(f)+\left|G_{S_{X_2}}(f)\right|^2S_{X_2}(f)+2\operatorname{cov}\left(S_{X_1}(f),S_{X_2}(f)\right)\left|G_{S_{X_1}}(f)\right|\left|G_{S_{X_2}}(f)\right| \qquad (2.44)$$

Power Spectral Densities are used since the transfer function may depend on the frequency. To be strictly correct we should consider any correlation between different sources (covariance is not zero if sources are not fully independent). But the improvement in accuracy that would results is not usually worth the complexity in analysis and is often thwarted by the variation in value for noise sources that it is due to IC manufacturing processes.

According to expression (2.44), when analyzing circuits including noise sources, the principle of superposition is not valid for voltages or currents, but for powers, that is, for voltages and currents squared and for its PSD.

Therefore, when analyzing circuits with noise sources the following rules apply:

- Combine any series or parallel components into a single equivalent component and then calculate the noise contribution to the equivalent component.
- Obtain the transfer function for any noise source analyzing the circuit when a common (not random) voltage or current source occupies the same circuit position. Calculate the output noise power spectral density by multiplying the noise source PSD by the squared modulus of the amplitude of the respective transfer function.

2.4.1 Equivalent Input Noise Voltage and Current Generators: Series and Parallel Noise

Any real (means noisy) two-port network, such as single-ended amplifier, can be considered a noiseless network with a noise voltage source in series which each port, as in Figure 2-2. Each voltage source represents the noise voltage measured at the respective port with the other port left open circuit. An alternative equivalent circuit uses a noise voltage source e_n (also called *series noise*) and a noise current source i_n (also called *parallel noise*) at the input port, Figure 2-2c. The use of these two generators plus a complex correlation coefficient (not shown) completely characterizes the noise performance of the device [91]. In the next section a method to compute or measure e_n and i_n based on the effect of source impedance is described.

Although e_n and i_n are normally correlated to some degree since they arise in part from the same noise sources, the typical spread of e_n and i_n for a device normally overshadows the effect of the correlation coefficient. Therefore it is common practice to assume the correlation coefficient is equal to zero.

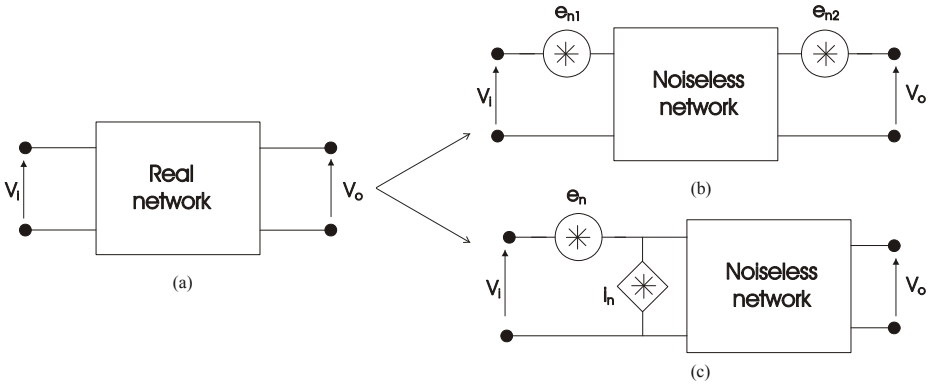

Figure 2-2. General noise models for a two-port network. Figure taken from [79].

2.4.2 Effect of source impedance

In Figure 2-3 there is a voltage signal with output Z_s connected to an amplifier whose input impedance is Z_i. The equivalent circuit for noise analysis is shown in Figure 2-3b. There is the thermal noise of Z_s (of Re[Z_s]), called e_t, and the amplifier input noise voltage, e_n, and current, i_n. This current source can be replaced by a voltage source $e_i^2 = i_2^i \left| Z_S \right|^2$ as shown in Figure 2-3c.

Any voltage source at the input of the preamplifier in Figure 2-3 will undergo an attenuation $A(f) = \dfrac{Z_I(f)}{Z_I(f) + Z_S(f)}$ followed by the amplification *G(f)* provided by the amplifier. From (2.33), the output noises PSD will be

$$e_{no}^2(f)=\left(e_t^2+e_n^2+i_n^2\left|Z_S(f)\right|^2\right)\left|A(f)\right|^2\left|G(f)\right|^2=\left(\left(e_t^2+e_n^2\right)\left|A(f)\right|^2+i_n^2\left|Z_S\parallel Z_I(f)\right|^2\right)\left|G(f)\right|^2 \quad (2.45)$$

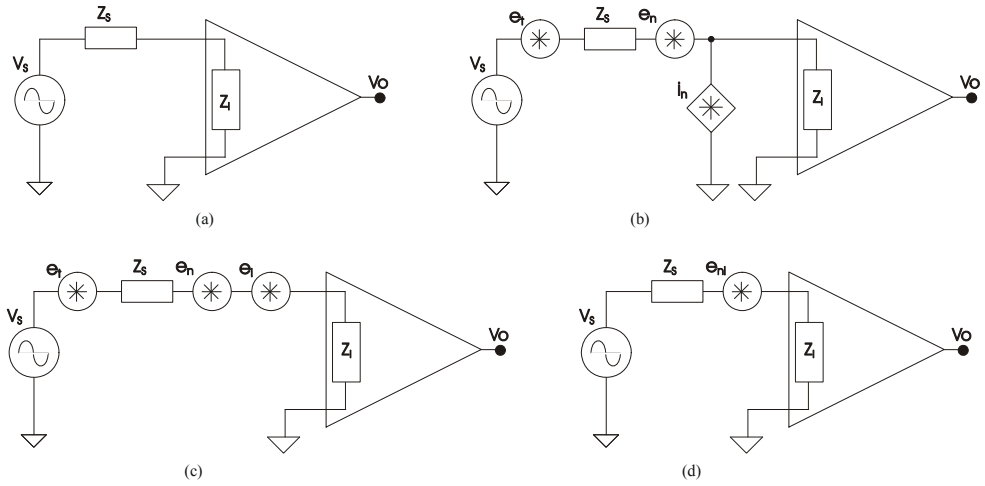

Figure 2-3. Single-ended amplifier equivalent noise models. Figure taken from [79].

The equivalent input noise PSD in Figure 2-3d is the quotient of the output noise PSD divided by the squared system gain ($A \times G$). Hence,

$$e_{ni}^2(f)\doteq\frac{e_{no}^2(f)}{\left|A(f)\right|^2\left|G(f)\right|^2}=e_t^2+e_n^2+i_n^2\left|Z_S(f)\right|^2 \quad (2.46)$$

Therefore, e_{ni} does not depend on the amplifier gain or its input impedance. Both parameters, however, are necessary to calculate the output noise. Equation (2.46) suggests a simple procedure to measure the different components of e_{ni}. If $Z_S=0$ (input short circuit), e_t will be zero too. Hence, the output noise will be only contributed by e_n. If $\mathrm{Re}[Z_S]$ is designed to be very large, e_t will increase as $\sqrt{\mathrm{Re}[Z_S]}$ but the contribution of i_n will increase as Z_S, so that it will predominate as depicted in Figure 2-4.

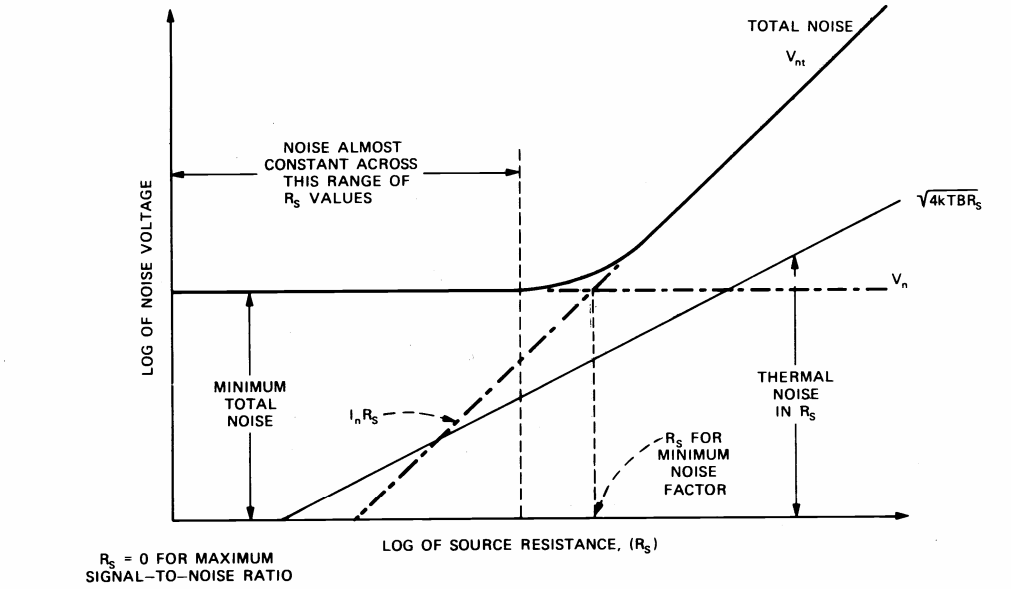

Figure 2-4. Total equivalent input noise voltage e_{ni} for a typical device and its components (e_t, e_i and i_n). Figure taken from [80].

The reasoning above also points out that, although e_n and i_n vary with frequency and depend on the amplifier's technology, for low-impedance signal sources, e_n will dominate the noise, whereas for high-impedances sources, i_n will yield the larger contribution. Therefore, since FET-input amplifiers have very small input currents, they are suitable for high impedance voltage sources. In any case, because of e_t, high impedance sources will be inherently noisy if they have a large resistive component.

2.4.3 Noise Factor (*F*) and Signal to Noise Ratio (*SNR*)

The noise factor (F) is a quantity that compares the noise performance of a device to that of an ideal (noiseless) device. It can be defined as

$$F \equiv \frac{Noise\ power\ output\ of\ actual\ device}{Noise\ power\ output\ of\ ideal\ device} \tag{2.47}$$

The noise power output of an ideal device is due to the thermal noise power of the source resistance. The standard temperature for measuring the source of noise power is 290 K. An equivalent definition of noise factor is the input signal-to-noise ratio (SNR_i) divided by the output signal-to-noise ratio (SNR_o),

$$F \equiv \frac{\mathrm{SNR_i}}{\mathrm{SNR_o}} \tag{2.48}$$

The equivalent input noise divided by the thermal noise from the signal source resistance is the noise factor,

$$F \doteq \frac{e_{ni}^2}{e_t^2} = 1 + \frac{e_{ni}^2 + i_n^2 \left|Z_S\right|^2}{e_t^2} \tag{2.49}$$

The noise figure NF is defined as $NF \doteq 10 \log F$. Ideally, $F=1$, that is, the amplifier does not contribute any noise. F does not depend on signal amplitude, or on amplifier load. For a purely reactive source $e_t^2 = 0$ and F would not have any meaning.

2.4.4 Optimal source resistance

When R_S=0 the source thermal noise and the noise factor tend to infinity, but also when R_S tends to infinity F will also tend to infinite. Therefore, there is an optimal value for R_S which makes F minimal. For a resistive signal source and to find the minimal F we set the derivative of (2.49) to zero to obtain

$$\frac{\partial F}{\partial R_S} = \frac{4kT\left(i_n^2 R_S^2 - e_n^2\right)}{\left(4kT R_S\right)^2} = 0$$

Thus the optimal source resistance is

$$R_{OP} = \frac{e_n}{i_n} \tag{2.50}$$

Therefore, the noise contributed by the amplifier is minimal when the source resistance is R_{OP}. Both, F and R_{OP} will depend on frequency if e_n and i_n are frequency dependent.

Nevertheless, minimizing F may not be the best design criterion. For example, if an amplifier has a very small i_n, selecting a very large R_S yields $F \approx 1$. However, from (2.46) it is obvious that the equivalent noise will be very large because of the thermal noise of R_S. We are interested in maximizing the signal-to-noise ratio (SNR),

$$\frac{S}{N} = \frac{v_s^2}{e_t^2 + e_n^2 + i_n^2 R_S^2} \qquad (2.51)$$

where v_s^2 is the power spectral density of the input signal. The optimal R_S can be obtained by setting the derivative of (2.51) to zero. However, this requires us to know the dependence between v_s and R_S. Usually, there are three cases [92]:

- The signal PSD is independent of R_S. This is the case of some inductive sensors where an increase in L_S (inductive part of the source impedance) implies an increase in v_s and in R_S. On that situation, the optimal SNR is for R_S =0.
- The signal PSD v_s^2 is proportional to R_S. On that case the SNR has a maximum at R_{OP}.
- The signal PSD v_s^2 is proportional to R_S^2. On that case the SNR is a monotonic function that increases with R_S. This is valid for sensors that can be modeled as current sources, for example.

The signal source, however, will have a given output impedance, not necessarily optimal according to (2.50) or any other criterion. *Noise matching* is transforming the impedance of the source to match the amplifier's optimal noise resistance. This is usually done by inserting a transformer between the signal source and the amplifier.

2.4.5 Noise of Cascaded Stages

The overall noise factor of series of *n* networks connected in cascade was shown by Friis ([93]) to be

$$F = F_1 + \frac{F_2 - 1}{H_1} + \frac{F_3 - 1}{H_1 H_2} + \ldots + \frac{F_n - 1}{H_1 H_2 \ldots H_n} \qquad (2.52)$$

where F_1 and H_1 are the noise factor and available power gain of the first stage, F_2, H_2 are those of the second stage.

Equation (2.52) clearly shows the important fact that with sufficient gain in the first stage of a system, the total noise factor (or *SNR*) is primarily determined by the noise factor F_1 (or *SNR*) of the first stage.

2.5 Fundamentals of Noise Analysis in Nuclear and Particle Physics

In Nuclear and Particle Physics instrumentation the time profile of the detector signal and the response of the pulse shaper are used in signal response calculations and in analyzing pile-up and ballistic deficit effects. Additionally, the time-domain approach offers an intuitive picture of the effect of shape on noise and facilitates handling the behavior of time-variant shapers and cases where circuit elements contributing to noise vary with time. Probably due to these reasons, a particular methodology for the noise analysis has been developed on that field, however, we will see that it is consistent and equivalent with the concepts presented in previous section.

We will summarize the formulation presented by Radeka in [95] and by Manfredi and Gatti in [94], other sources are [95], [96], [97] and [99]. Goulding present an alternative formulation, see [10], [98] and [100]; it is interesting to point out that this technique is able to deal with non-stationary noise sources [100].

Time varying networks are used often in Nuclear and Particle Physics instrumentation and, as it has been pointed out in section 2.3, the complexity of the noise analysis for time variant circuit is higher than for time invariant circuits. Indeed some authors claim that time variant shapers cannot be

dealt with in the frequency domain in any convenient and general way ([94], [100] and [101]). It is not clear at all what means such statement because it is not explained in detail and because there are general methods to analyze the response of time variant networks to random input signals, summarized in section 2.3. What is clear is that time domain techniques may have some advantages to define the effect of the shaping on the noise process, because the analysis of the circuit can not be performed in a direct and simple way in frequency domain as it is done for time invariant circuits, i.e. using the Fourier or Laplace transform of elementary circuit elements to avoid complex differential equations.

However, it is important to point out that in time domain approach there is not a suitable time domain model for Flicker noise (or any non-white noise), because ideal *1/f* noise is a weakly divergent process whose exact autocorrelation is impossible to express in a closed-form solution [101]. Nevertheless, it is possible to perform approximated analysis and simulations using a prefilter that colors white noise ([101] and [103]). Other important limitation of time domain is the lack of noise analysis in time domain for common circuit SPICE simulators where noise analysis is included on the form of noise spectral density calculations for linearized circuits. There are some attempts to incorporate capability of analyze noise in time domain in those simulators, a comprehensive discussion can be found in [101]. Other works try to extend classical formulation of noise in time domain to frequency domain in order to be able to use frequency analysis and simulation techniques, these works will be discussed later.

Subsequent discussion will start from Radeka's formulation [95], but different treatment will be given in some points, especially regarding time variant shaping.

The basis of a noise process can be represented as a sequence of randomly generated elementary impulses (Dirac function $\delta(t)$) that has a Poisson distribution in time [104]. At the output of the system, individual impulses may or may not be separated in time depending on the width of the impulse response of the read out system ($h(t)$) and on the rate n of occurrence of the impulses. When the impulse response of the device, with which we are looking on the noise signal, is much longer than $1/n$, the characteristics noise waveforms (those observed on an oscilloscope) are produced as a superposition of responses to individual impulses. This is illustrated in Figure 2-5, for an impulse response of relaxation type (RC=τ). For a signal measurement, we are interested in the measurement error due to the noise at the observation time t_0;i.e., when the signal is observed (the signal is not shown in the figure). The amplitude of noise at t_0 is the result of many randomly generated noise impulses. In Figure 2-5 all impulses are of the same polarity, but usually noise impulses are both polarities, thus the mean output value equals to zero.

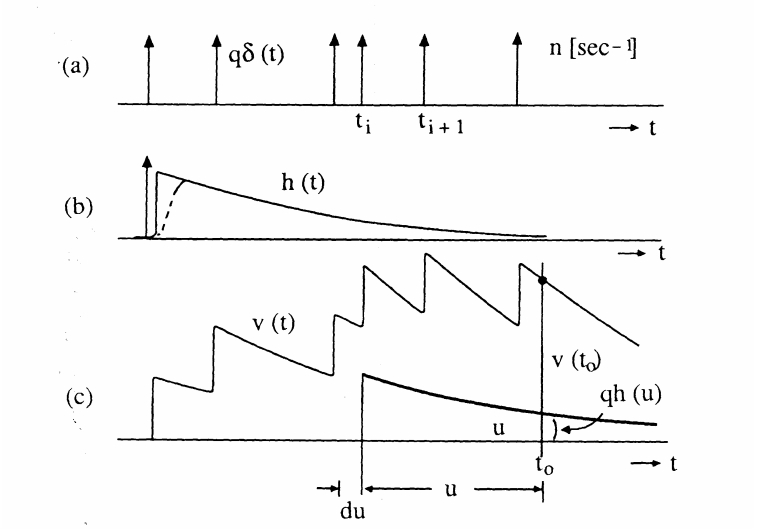

Figure 2-5. System output for a random sequence of impulses at the input. [95]

2.5.1 Noise Weighting function w(u)

According to the Figure 2-5, the contribution $v_i(t)$ to the output signal $v(t)$ at time t_0 of an impulse occurring at time t_i is $v_i(t_0) = qh(t-t_i)\big|_{t=t_0} = qh(u)$ with $u=t_0-t_i$. This is always true only for time invariant systems. Imagine a time variant system that, for example, resets a component at a given time, then the noise impulses occurring during the reset time, depending on the position of the switch and on the duration of the impulse response, the noise impulse might not have any influence in a present or future measurement.

We will recall now the definition of *Noise Weighting function* given in [95].*The Noise Weighting function $w(t_0,t_i)$ is defined to be able to describe both time invariant and time variant systems. It is defined as the output at the measuring time $t=t_0$ which results from a unit impulse $\delta(t-t_i)$ delivered by an input noise generator at a time $t=t_i$.*

For *time invariant systems* the response of the system does not depend on the time and it is $h(t- t_i)$ for a unit impulse $\delta(t- t_i)$ produced at any t_i. It follows then that the weighting function for a time invariant shaper is,

$$w(t_0,t_i) = h(t-t_i)\big|_{t=t_0} = h(u) \qquad (2.53)$$

The weighting function is usually represented as a function of the time of the unit impulse t_i, then it can be regarded as the mirror function in time of the impulse $h(t)$ (see Figure 2-6). Figure 2-6 shows that maximum of $h(t)$ is at T_m, the so called measurement time or peaking time because the maximum of the impulse response of the shaper is the typical time to measure the detector signal (assuming the signal impulse is produced a $t=0$). Therefore, T_m is a specific value of the measurement time variable t_0. The fundamental characteristic of fixed networks is that their impulsive response is dependent solely upon the so-called age variable, that is, the difference between the instant of observation (t_0) and the instant of application of the impulse (t_i). In the literature the Noise Weighting function is usually referred as a function of a single variable (the age variable) w(t) or w(u), we will use these convention also for time invariant shapers.

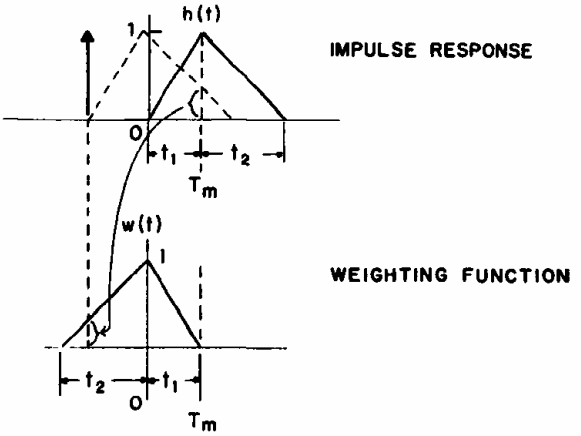

Figure 2-6. The weighting function $W(t)$ of a time invariant system is a mirror image in time of the impulse response with respect to the time of measurement T_m (a particular value of t_0). [95]

If a noise hit occurs at after the measurement time $t=t_i > t_0$ ($u<0$) and since $h(x)$ is causal ($h(x)=0$ *for* $x<0$) the contribution of this hit is zero. Figure 2-6 shows the definition of the Weighting function as the mirror of the impulse response of a time invariant system. If $h(t)$ is transformed according to $t=t_0-t_i$, i.e.: if it is shifted by t_0 and if it is mirrored, then the evaluation of the resulting function $w(t)$ at a time t gives the contribution at the measurement time t_0 of a noise impulse arriving at that time t. For the particular case $t_0=T_m$, shifting $h(t)$ by T_m, means that the maximum of $w(t)$ is at $t=0$: maximum contribution is given by noise impulses arriving at the same time as detector signal.

In the case of time variant shapers the situation is more complex because the impulse response changes with time. Figure 2-7 shows the noise weighting function for a time invariant processor with triangular impulse response of the form depicted in Figure 2-6. It also shows the weighting function for a possible time variant network where a prefilter with the same impulse response of the time invariant shaper is followed by a switch which is closed for $11 \leq t_0 \leq 20$.

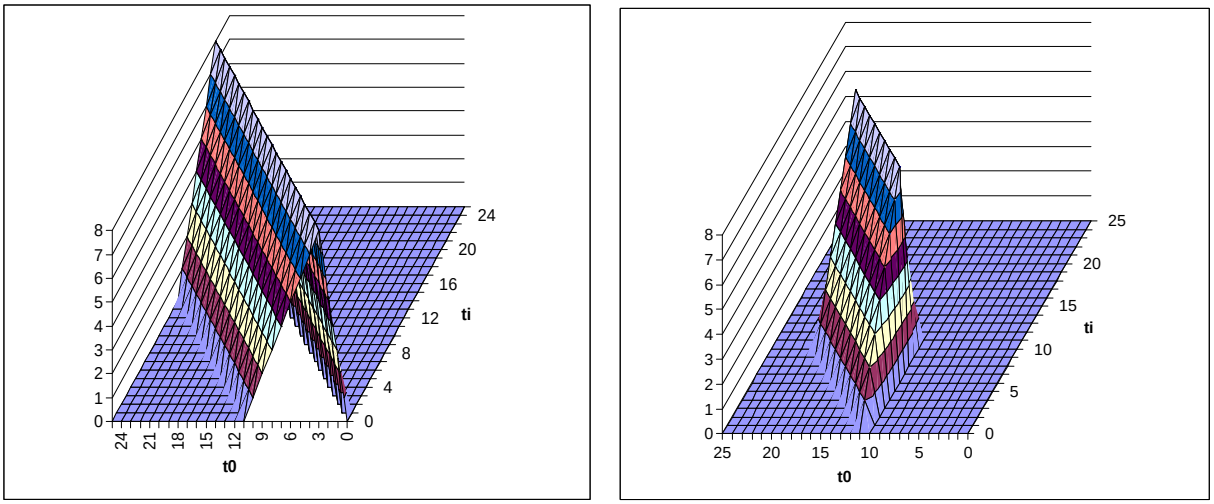

Figure 2-7. Noise weighting function for a time invariant (left) and a time variant shaper (right).

As far as we are aware there is no systematic approach to compute $w(t_0,t_i)$ in noise analysis of front end for particle detectors. The most common procedure is to use the definition of $w(t_0,t_i)$ and the knowledge of a particular processor to derive its expression for a particular measurement time, see [94]. An example of such procedure will be given in section 2.6.5.

Nevertheless, a connection can be established with theory of analysis of time variant systems, see section 2.3. What is not done in previous works on that field is to establish a relationship between the weighting function and the concept of the time variant impulse response or weighting function $h(t_i,t)$ [88]. According to [88], see section 2.3, the time variant impulse response represents the output response at a time t of a given system to an impulse applied at $t= t_i$, $\delta(t- t_i)$. Comparing to the definition of weighting function given above in this section, we can conclude that the noise weighting function of a time variant shaper corresponds to the time variant inmpulse response (2.42):

$$w(t_0,t_i) = h(t,t_i)\Big|_{t=t_0} \qquad (2.54)$$

Unfortunately, there is no simple way to derive neither the time variant impulse response nor the time variant transfer function [88]. Nevertheless, equation (2.54) provides an important relationship to proof that analysis of time variant systems can be carried out in the frequency domain, as we will see in next section. As said before, in section 2.6.5 a method to compute $w(t_0,t_i)$ for a fixed measurement time will be described.

2.5.2 Computation of the variance of the output noise

In this section we will try to generalize to time variant shapers the analysis given in [95], which is restricted to time invariant shapers due to the application of some relationships valid only for time invariant systems. A simple tool for calculation of the noise variance is Campbell's theorem, which states that the sum of mean square contributions of all preceding impulses with charge q equals the variance. The contribution at time t_0 of an impulse occurring at time t_i, is $v_i(t_0) = qw(t_0,t_i)$ with $u=t_0-t_i$. By using Campbell's theorem and subtracting the mean value, one obtains (for white noise),

$$\sigma^2(t_0) = \left\langle v^2(t_0) \right\rangle - \left\langle v(t_0) \right\rangle^2 = q^2 \sum_i w^2(t_0, t_i) \qquad (2.55)$$

For a very high rate of impulses, $\langle n \rangle \tau \gg 1$, we can use continuous variables and write for a contribution to the variance at t_0 from impulses generated in the time interval du is $q^2 w(t_0, t_i)^2 \langle n \rangle dt_i$ (mean number of impulses in dt_i is $<n>dt_i$). We add all the previous history and obtain,

$$\sigma^2(t_0) = \langle n \rangle q^2 \int_{-\infty}^{+\infty} w^2(t_0, t_i)\, dt_i \qquad (2.56)$$

If the random process is stationary (time invariant shaper) σ^2 is independent of the time t_0 of the measurement. Integration limits $(-\infty,\infty)$ signify that the integration has to be carried out for all nonzero values of the weighting function $w(t_0,t_i)$ independently of the origin of the time variable t_i.

The noise variance is determined by the noise process, the rate $<n>$ and the charge q of impulses and by the weighting function $w(t_0,t_i)$ (this is related to the noise bandwidth B in the representation of noise in frequency domain).

The result for the variance $\sigma^2(t_0)$ has been derived without any reference to noise description in the frequency domain in terms of the noise power spectral density. However, as said in section 2.1 noise is usually described using its PSD, therefore it is useful to find a way to use this description in the time domain representation.

The total "energy" of the system response is independent of whether the output is analyzed in terms of time or frequency so that we can write for a time invariant system:

$$\int_{-\infty}^{+\infty} w(t)^2\, dt = \frac{1}{2\pi} \int_{-\infty}^{+\infty} \left| W(\omega) \right|^2 d\omega \qquad (2.57)$$

where $W(\omega)$ is the Fourier transform of the weighting function. This equality follows from Parseval's theorem. In the same way for the time variant weighting function, for a given t_0 which can be taken as a parameter,

$$\int_{-\infty}^{+\infty} w^2(t_0, t_i)\, dt_i = \frac{1}{2\pi} \int_{-\infty}^{+\infty} \left| W(\omega, t_0) \right|^2 d\omega \qquad (2.58)$$

where $W(\omega,t_0)$ is the Fourier transform of the time variant weighting function with t_0 as a parameter.

Since $H(\omega)^2$ is an even function (and with $\omega=2\pi f$):

$$\int_{-\infty}^{+\infty} w^2(t_0, t_i)\, dt_i = 2 \int_0^{+\infty} \left| W(\omega, t_0) \right|^2 df \qquad (2.59)$$

Using (2.59) and (2.56), the noise variance is:

$$\sigma^2(t_0) = 2 \langle n \rangle q^2 \int_0^{+\infty} \left| W(\omega, t_0) \right|^2 df \qquad (2.60)$$

According to the relationship between weighting function and time variant impulse response (2.54) and the definition of time variant impulse response (2.42),

$$W(\omega, t_0) = F\{w(t_0, t_i)\} = F\{h(t_0, t_i)\} = \int_{-\infty}^{\infty} h(t_0, t_i) e^{-j2\pi f t_i} dt_i = H(j\omega, t_0) e^{j\omega t} \qquad (2.61)$$

Then we can also write,

$$\sigma^2(t_0) = 2 \langle n \rangle q^2 \int_0^{+\infty} \left| H(\omega, t_0) \right|^2 df \qquad (2.62)$$

Comparing (2.62) with (2.43) of section 2.3, it follows that this relation represents an integrated PSD at the output of the system, and that the PSD at the input is

$$G_{xx}(\omega) = 2 \langle n \rangle q^2 = G_0 = e_0^2 = i_0^2 \qquad (2.63)$$

Therefore we can express the variance of the noise at the output using the definition of the weighting function either in time domain

$$\sigma^2(t_0) = \frac{1}{2} G_0 \int_{-\infty}^{+\infty} w^2(t_0, t_i)\, dt_i \qquad (2.64)$$

or in frequency domain (2.43),

$$\sigma^2(t_0) = G_0 \int_0^{+\infty} \left| W(\omega, t_0) \right|^2 df \qquad (2.65)$$

Previous expressions are valid both for time variant and time invariant shapers, thus both are described by the weighting function, while their implementation will be quite different. For time invariant shapers equation (2.64) becomes

$$\sigma^2 = \frac{1}{2} G_0 \int_{-\infty}^{+\infty} w^2(t)\, dt = \frac{1}{2} G_0 \int_{-\infty}^{+\infty} h^2(t)\, dt \qquad (2.66)$$

We obtain the same result as the one in expression (2.41), derived for white noise using the autocorrelation function. Note that (2.66), as it was (2.41), is only valid for white noise.

It has been already pointed out by some authors ([114], [115] and [116]) that it is possible to use the Fourier transform of the weighting function to compute the variance of the output noise and that therefore, it is possible to include non white noise sources such *1/f* noise. However, some operations (such Fourier transforms or convolutions) are not fully justified or clearly defined for time variant circuits in those works. We will use the identity of the noise weighting function with the time variant impulse response to derive a general form of (2.65) (valid also for non-white noise), just recalling expression (2.43),

$$\sigma^2(t_0) = \int_0^{\infty} \left| W(\omega, t_0) \right|^2 G_{xx}(f) df \qquad (2.67)$$

So far we have modeled noise as a current generator in parallel with the detector, i.e. parallel noise. To fully determine the noise contribution by the amplifying device, we have to take into account that series noise acts on a different way. This will be studied in next section.

2.6 Noise in Front End Electronics for Detectors

Figure 2-8 shows a schematic representation of typical front end for detector readout, with the elements described in section 1.1: the detector modeled as a current source, the detector and stray capacitances C_D, the preamplifier, the shaper and the discriminator (or ADC). The preamplifier is composed by an ideal preamplifier (noiseless and with a resistive ideal input impedance R_I, that means infinite for voltage preamps and zero for charge and current preamplifiers), the series e_n and parallel i_n input noise sources and the input capacitance C_I of the preamp (which models the reactive frequency dependent part of the impedance of the preamp). Usually, a detector is a capacitive signal source and no load resistor R_S at the preamplifier input is used (except on the case of the photomultipliers), because it would increase the parallel noise.

Preamplifier impulse response is *p(t)* and its Fourier transform is *P(ω)*, shaper impulse response is *s(t)* and its Fourier transform is *S(ω)*. The impulse response of the overall system is *h(t)*, and can be obtained from the convolution of *p(t)* and s(t): $h(t) = p(t) \otimes s(t)$. The Fourier transform of the impulse response of the system is $H(\omega) = P(\omega) \cdot S(\omega)$. As said in section 1.1, usually the preamplifier is designed to be fast enough so that the transfer function of the complete system is given by the shaper, so that $H(\omega) = S(\omega)$. In the case of the ideal charge sensitive preamplifier it means that response to a δ current impulse is a step function voltage (named *u(t)*) at the output of the preamplifier. This will be assumed in following considerations.

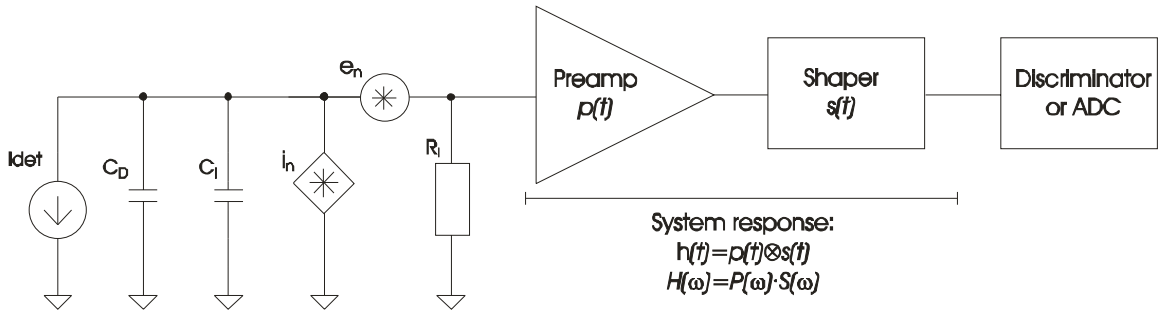

Figure 2-8. Typical front end of detector read out.

In this section we will review how the general concepts about noise exposed up to now can be applied to the most common configurations in detector electronics. First a definition of an input equivalent noise in terms of charge is presented. Then, the series and parallel noise input sources are studied, taking into account the effect of the impedances (C_I,C_D and any other impedance such bias resistors) at the preamplifier input. It will be outlined how noise can be reduced choosing the proper shaping. Finally, the characteristics of some implementations according to the active device used are summarized.

Impulse response of a preamplifier *p(t)* with constant gain *G* is defined with different input/output variables according the type of the preamplifier (and assuming bandwidth of preamplifier much higher than pulse bandwidth):

- Voltage sensitive: $p(t)=G\cdot V_O\cdot\delta(t)$ for an input voltage δ impulse.
- Current sensitive: $p(t)=G\cdot V_O\cdot\delta(t)$ for an input current δ impulse.
- Charge sensitive: $p(t)=G\cdot V_O\cdot\delta(t)$ for an input charge δ impulse. Since $i(t)=dq(t)/dt$, it can be also defined $p(t)=G\cdot V_O\cdot u(t)$ for a input current δ impulse.

The charge sensitive configuration is by far the most extended in detector electronics. For this reason most shapers are usually defined according to the response to a step voltage at its input (the charge sensitive preamplifier output to a detector current pulse) as explained in section 1.1.2. In the following considerations about shaping, we will take the system transfer function *h(t)* as the response to an input current δ impulse.

2.6.1 Equivalent Noise Charge (ENC)

In order to compare the electronic noise with the signals generated in detectors conveniently, the electronic resolution is generally expressed as the total equivalent noise charges (ENC). The equivalent noise charge ENC of a detector readout system is defined as the ratio of the total integrated r.m.s. noise at the output of the pulse shaper to the signal amplitude due to one electron charge *q* [105], i.e. the ENC equals to a signal that would produce the same output amplitude as the total integrated r.m.s. noise at the output. As the definition implies, the ENC depends on the characteristics of both the preamplifier and the shaper. Therefore, optimization of ENC will in general involve optimal designs of both the preamplifier and the shaper.

As stated before, one basic function of the pulse shaper is to improve the SNR of the readout system. It has been demonstrated that exists a shaper that optimizes the SNR. However, other factors such as counting rate requirement, pile-up rejection, etc, must be considered as well in choosing the most suitable shaper for a given application. These points are discussed in sections 2.6.3 to 2.6.6.

The optimization of the preamplifier is more constrained by the device or technology of the preamplifier and detector than the optimization of the shaper is. This is discussed in section 2.6.7 and 2.6.8.

2.6.2 Series and parallel noise

The parallel noise generator i_n is a current source at the preamplifier input, so the response for a δ impulse of this current source is by definition the impulse response of the system *h(t)* (in the case of charge sensitive preamplifier). Therefore the noise variance ($\sigma^2_{O_P}$) or noise square voltage ($E^2_{O_P}$) at the output of the shaper due to the parallel noise is, according to previous results (for white noise),

$$\sigma^2_{O_P} = E^2_{O_P} = \frac{1}{2} i_n^2 G^2 \int_{-\infty}^{+\infty} w(t)^2 \, dt \qquad (2.68)$$

where $w(t) = h(t_0 - t)$ for time invariant shapers and *G* is the constant preamplifier charge gain.

The equivalent noise charge due to the parallel noise ENC_P is obtained normalizing the noise variance at the output to the signal output for a δ impulse at the measurement time T_m,

$$ENC_P^2 = \frac{1}{2} i_n^2 \frac{\int_{-\infty}^{+\infty} w(t)^2 \, dt}{w(T_m)^2} \qquad (2.69)$$

The series noise e_n is an equivalent input voltage source, thus a voltage δ impulse in e_n should be translated to current in order to use *h(t)*. Using superposition and considering that the input impedance of the charge preamplifier is very low, the input current due to e_n is $i_{in}(t) = (C_D + C_I) \frac{de_n(t)}{dt}$, therefore response to a voltage δ impulse is,

$$i_{in}(t) \otimes h(t) = (C_D + C_I) \frac{d\delta(t)}{dt} \otimes h(t) = (C_D + C_I) \frac{dh(t)}{dt} = (C_D + C_I) h'(t) \qquad (2.70)$$

The noise variance ($\sigma^2_{O_S}$) or noise square voltage ($E^2_{O_S}$) at the output of the shaper due to the (white, not taking into account *1/f* noise for the moment) series noise is, according to (2.70) the response to a voltage δ impulse is the proportional to the derivative of the response to a current δ impulse and the same happens with the noise Weighting function,

$$\sigma^2_{O_S} = E^2_{O_S} = \frac{1}{2} e_n^2 (C_D + C_I)^2 G^2 \int_{-\infty}^{+\infty} w'(t)^2 \, dt \qquad (2.71)$$

The equivalent noise charge due to the series noise ENC_S is,

$$ENC_S^2 = \frac{1}{2} e_n^2 (C_D + C_I)^2 \frac{\int_{-\infty}^{+\infty} w'(t)^2 \, du}{w(T_m)^2} \qquad (2.72)$$

Total ENC is the sum of series and parallel noise,

$$ENC^2 = \frac{1}{2} i_n^2 \frac{\int_{-\infty}^{+\infty} w(t)^2 \, dt}{w(T_m)^2} + \frac{1}{2} e_n^2 (C_D + C_I)^2 \frac{\int_{-\infty}^{+\infty} w'(t)^2 \, dt}{w(T_m)^2} \qquad (2.73)$$

Series noise increases with preamplifier input capacitance or detector capacitances, whereas parallel noise is independent.

Expression (2.73) does not serve to analyze the effect of Flicker noise, which is present usually in the series noise generator. To do this the frequency domain approach should be taken.

Expression (2.73) is usually written in the following way,

$$ENC^2 = \frac{1}{2} e_n^2 (C_D + C_I)^2 \left[\int_{-\infty}^{+\infty} w_N'(t)^2 \, dt + \frac{1}{\tau_C^2} \int_{-\infty}^{+\infty} w_N(t)^2 \, dt \right] \qquad (2.74)$$

where $w_N(t) = \frac{w(t)}{w(T_m)}$ is the normalized Weighting function and τ_C is the noise corner time constant,

$$\tau_C = \sqrt{\frac{e_n^2}{i_n^2}}\left(C_D + C_I\right) \tag{2.75}$$

The noise corner time constant τ_C is the reciprocal of that particular angular frequency ω_C at which the contributions from series and parallel (white) noise at the preamplifier input (for the input equivalent noise voltage $e_{ni}^2 = e_n^2 + \frac{i_n^2}{\omega^2\left(C_D + C_I\right)^2}$) became equal.

2.6.3 Optimal shaping

Equation (2.74) raises the question: what is the optimum shape of the impulse response *h(t)* to minimize the equivalent noise charge? The optimum impulse response can be found by using the calculus of variations [97]. The solution is,

$$h_{opt}(t) = e^{-\frac{|t|}{\tau_C}} \tag{2.76}$$

and the corresponding optimal ENC is,

$$ENC_{OPT}^2 = \left(4e_n^2 i_n^2\right)\left(C_D + C_I\right) \tag{2.77}$$

The function (2.76) is known as the "cusp" or as the "matched filter". The matched filter concept is discussed in some detail in [94]; it is shown that the "cusp" can be derived both in a time domain approach [107] and in a frequency domain approach [108]. The "cusp" derivation in frequency follows the derivation of the optimum filter for communications systems where it is called "matched filter" [109]. This function implies an infinite delay (in practice only several times τ_C) between the event (induced current impulse) and the measurement time when the peak of the response is recorded. The tails of this function have a small effect on the measured noise. For example, if the system is constrained to a triangular impulse response, its optimum half-width is $\sqrt{3}\tau_C$, and the noise calculated from Equation (2.74) is only 8% higher than for the ideal filter.

We usually strive to reduce the parallel noise since it is a result of imperfections and not intrinsic as is the noise associated with the amplification. In the system design, it is best to make noise corner time constant τ_C much longer than the system response. Then the second term in Equation (2.74) becomes negligible. It can be shown that the optimum response for the series (amplifier) noise alone is a triangular function,

$$w_{Triang}(t) = \begin{cases} 1 - \frac{|t|}{T_m} & for\ |t| < T_m \\ 0 & for\ |t| > T_m \end{cases} \tag{2.78}$$

where T_m is the zero-to-peak time (and the FWHM) and it defines the measurement time with respect to the time of occurrence of the signal impulse. In order to compute the ENC for a triangular shaper the frequency approach is taken to calculate the effect of Flicker series noise ($e_n^2(f) = e_{n_0}^2 + \frac{e_{n_f}^2}{f}$) (see [94]),

$$ENC_{Triang}^2 = 2e_{n_0}^2\left(C_D + C_I\right)^2\frac{1}{T_m} + e_{n_f}^2\left(C_D + C_I\right)^2\frac{4\ln 2}{\pi} + \frac{2}{3}i_{n_0}^2 T_m \tag{2.79}$$

First term of (2.79) correspond to series white noise, second term to series *1/f* noise and third term to parallel (white) noise.

2.6.4 Common shaping functions

Although "cusp" function represents the optimal processor many other shapers or filters are used in detector readout. Cusp function varies rapidly around its maximum, which is the point where signal has to be measured in order to obtain the best SNR. Therefore, any imprecision in the timing of the system that has to sample and convert (or discriminate) the signal would degrade the resolution. In addition, as said before, many other criteria are taken into account to design the shaper: the pile-up rejection, the baseline stability, the counting rate, the complexity of implementation, etc. For that reason, according to the application, many shaping functions have been used: the CR-RC, the sinusoidal lobe, the triangular, the semi-Gaussian or the trapezoidal step functions. A summary can be found in [10], [94], [95], [96], [97] and [98].

However, one of the most popular shapers, for monolithic time-invariant systems, is the Semi-Gaussian (SG) or CR-$(RC)^n$ shaping (described in section 1.1.2). The ENC for a SG of arbitrary order *n* is give by [105],

$$ENC_{SG}^2 = \left(\frac{\left(C_D + C_I\right)^2 \beta\left(\frac{3}{2}, n-\frac{1}{2}\right) n}{q^2 4\pi T_m} + \frac{\left(C_D + C_I\right)^2}{q^2 2n} + \frac{\beta\left(\frac{1}{2}, n+\frac{1}{2}\right) T_m}{q^2 4\pi n} \right) \left(\frac{n!^2\, e^{2n}}{n^{2n}} \right) \qquad (2.80)$$

where $\beta(x,y)$ is the Beta-function and T_m is the peaking time or measuring time of the SG shaper which is related to the time constant RC as T_m=n·RC. First term of the left parenthesis (2.80) correspond to series white noise, second term to series *1/f* noise and third term to parallel (white) noise.

If a second differentiation is added to the SG shaper its step response, which was unipolar turns out to be bipolar (see section 1.1.2). This is done in high counting rate systems, to improve the rise time and to attenuate the baseline shift if AC coupling exists. Nevertheless, the ENC of the unipolar SG shaper is smaller than the ENC of its bipolar counterpart [95].

In some cases rise time variations in detector signals may become very significant and an important factor in the choice of a shaper may be its insensitivity to the ballistic deficit. This means that the step function of the shaper must exhibit a flat top over a time at least equal to the maximum detector signal rise time. Shapers producing a sharply peaked waveform (such as the cusp) are not acceptable. Some shapers, such as the triangular (or symmetrical triangle) or the cusp may be modified to produce a flat top at slight cost in the parallel noise (series noise is proportional to h'(t) and this is zero during the flat top). It can be shown [94] that ENC_P increases as,

$$\Delta ENC_P^2\Big|_{Flat\,Top\,Time=T_{FT}} = i_n^2 T_{FT} \qquad (2.81)$$

where T_{FT} is the duration of the flat top. The trapezoidal [110], the double correlated sampling [112], and many other ([113], [123] and [127]) flat topped shaping step functions have been proposed to obtain immunity against ballistic deficit. The gated integrator exhibits outstanding insensitivity to detector pulse rise time fluctuations, it is widely used in these implementation of flat topped step functions, which usually are time variant processors.

2.6.5 Time variant shapers

The filtering properties of a time-variant system are described by its weighting function *w(t)*. As said before, the weighting function describes the contribution that a noise impulse, occurring at time t,

makes at the measurement T_m. It is essentially a measure of the memory of noise impulses (or any other signals) occurring before the observation time T_m. In time variant systems the shaper step response is different from the weighting function.

Systems can be divided in two main categories [94]:

- Shaping before the gate (Figure 2-9a). The detector is followed by a linear amplifier-shaping system and by a gate opened for interesting events: the pulse *h(t)* is integrated by an area sensitive ADC and the ADC is reset just after the end of the gate window T_m. In the figure, the weighting function *w(t)* which has to be used for noise performance calculations and which is different from *h(t)* is shown. An analytical discussion of the calculation of *w(t)* for this kind of shapers can be found in [94].

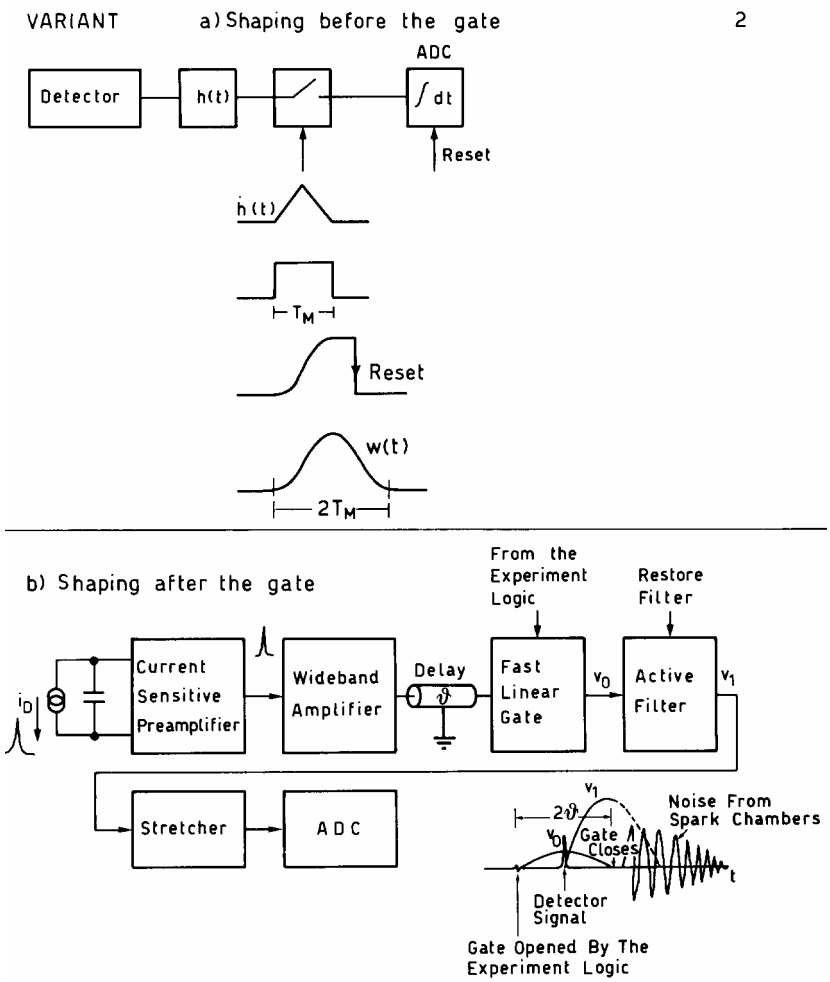

Figure 2-9. [94]. Time variant systems with shaping before the gate (a) and after the gate (b).

- Shaping after the gate (Figure 2-9b). The detector is followed by a fast current amplifier delivering at its output a narrow pulse similar to the $q\delta(t)$ input current pulse, a linear gate is opened for the interesting events (switch is closed when particles are detected) and with suitable delay, the fast pulse passes through the gate and excites the shaping network. The peak amplitude of the resulting signal is stretched and measured by a conventional ADC. The shaping network and the stretcher are reset to zero; the former as soon as the stretcher has stored the peak amplitude, the latter as soon as the ADC has sensed the stretched amplitude.

Figure 2-9b shows, for a particular processor, the pulse excited by the delayed δ pulse and truncated by the reset operation. The figure also shows a doublet noise pulse transformed into a δ by the splitting done by the opening of the gate. It is also shown that, by virtue of the appropriate timing,

the response induced by this noise pulse does not affect the measurement of the signal, because it has zero amplitude at the instant of peak measurement of the useful signal. If this is not done, the uncompensated part of the doublet will impair the SNR, in another words a discontinuity in *w(t)* means a infinite derivative *w'(t)*. If the effect of split doublet is avoided in the way shown, the root-mean square noise at the measurement instant can be calculated with the same procedure adopted for the time domain analysis of time-invariant shapers. This is a consequence of the fact that all the shaping is concentrated after the switch.

Figure 2-10 shows a typical time variant filter with shaping before the gate. Time variant part of the processor is a gated integrator. The switch conduction is synchronised with the detector-signal arrival and the switch remains conductive for $\tau_R \geq \tau_p$, where τ_p is the duration of the impulse response of the preshaper and *p(t)* its impulse response.

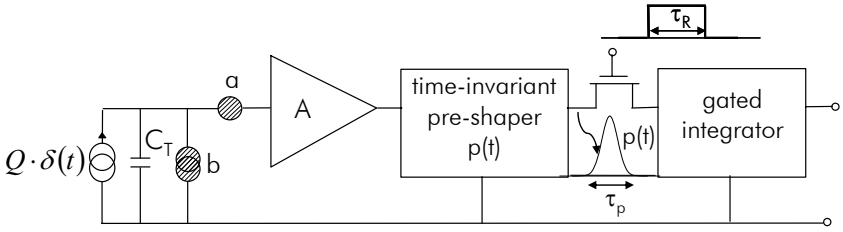

Figure 2-10.Typical time variant filter with shaping before the gate [111].

A detector signal of charge Q occurring at $t=t_1$ will produce at the pre-shaper output the signal $\frac{qA}{C_T} p(t-t_1)u(t-t_1)$ that is integrated over the time interval $[t_1,\ t_1+\tau_R]$. The contribution of the unit pulses describing series and parallel noises generator to the r.m.s noise at the measuring instant depends on their relationship with the signal. As signals arriving to the gate have a finite width τ_p, all the δ-pulses delivered by the parallel and series noise generator in the time interval $[t_1-\tau_p,\ t_1+\tau_R]$ contribute to the noise at the measuring instant $t_0=t_i+\tau_R$.

Figure 2-11 shows the numerical computation of an example the two-dimensional noise weighting function $w(t_0,t_i)$ corresponding to a prefilter with approximately Gaussian impulse response *p(t)*. The integration gate is $11 \leq t_0 \leq 20$. The particularized noise weighting function at the end of the integration time ($t_0=20$) is also shown.

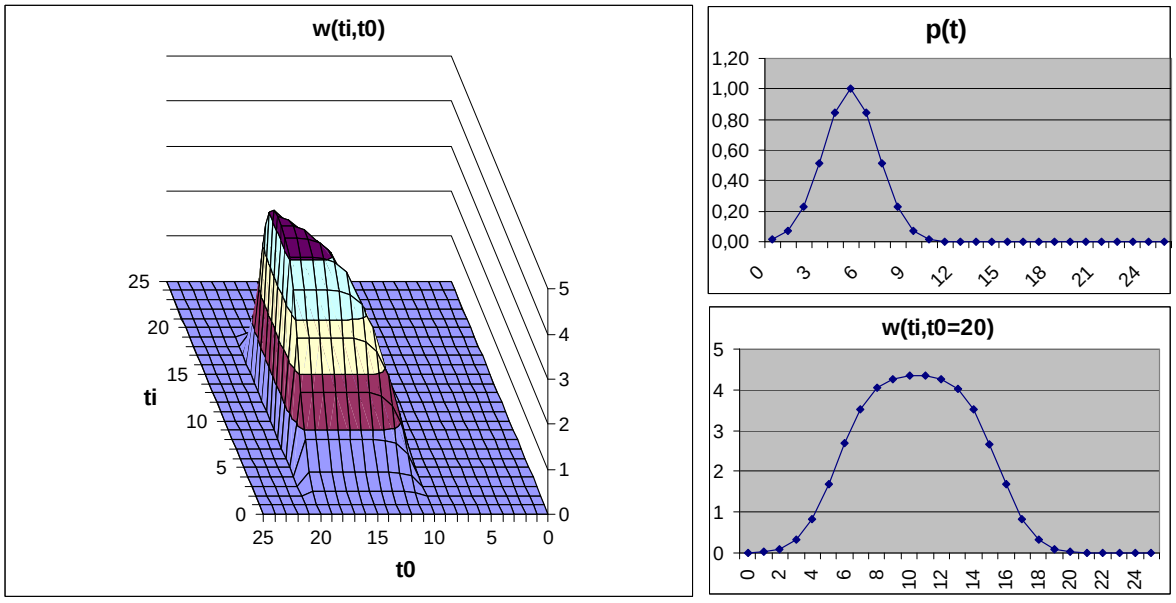

Figure 2-11. Two dimensional weighting function $w(t_0,t_i)$ (left), prefilter impulse response *p(t)* (right top) and particularized noise weighting function at $t_0=20$ (right bottom).

A common method to compute analytically the noise weighting function for a particular measurement time is depicted in Figure 2-12 ([111], [94]). The noise weighting function [$w(t_0,t_i)$] is the contribution at the measuring time t_0 to the noise at the measuring time instant given by a δ-pulse delivered by the parallel noise generator at a time t_i: ($t_i \in [t_1-\tau_p,\ t_1+\tau_R]$). The noise weighting function $w(t_0,t_i)$ is given by the area of the shaded region of the signal induced at the pre-shaper output by a δ-pulse of the parallel noise generator. In fact the portion of this signal entering the gate is integrated and stored in the integrator therefore contributing to the noise at $t_0=t_i+\tau_R$.

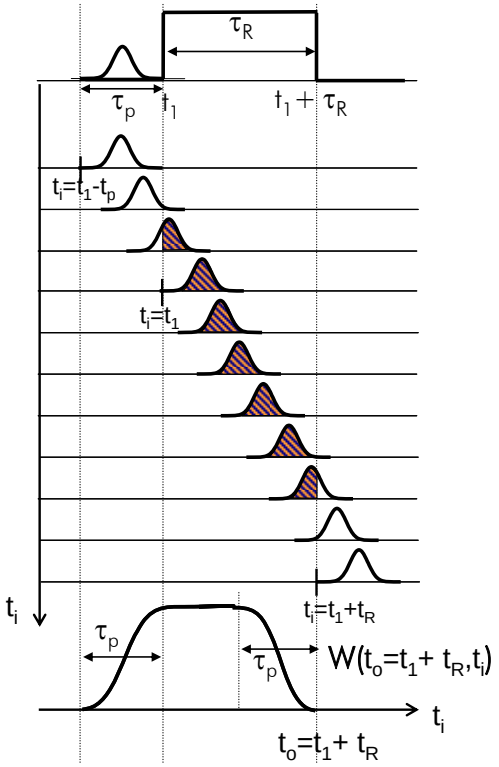

Figure 2-12. Weighting function of a gated integrator with prefilter [111].

The analytical expression of $w(t_0,t_i)$ can be computed by parts:

1. If the current impulse is produced after the end of the integration ($t_i>t_1+\tau_R$) or ends before the start of the integration ($t_i+\tau_P<t_1$) the contribution is null: $w(t_0,t_i)=0$.
2. If the current impulse is produced at a t_i before the start of the integration t_1 ($t_i<t_1$) but part of the tail of pulse is inside the integration window ($t_i+\tau_P>t_1$):

$$w\left(t_0=t_1+\tau_R,t_i\right)=\int_{t_1-t_i}^{\tau_p}p\left(x\right)dx \qquad t_1-\tau_p<t_i<t_1 \qquad (2.82)$$

3. If the current impulse arrives after start of integration ($t_i>t_1$) and ends before the end of the integration ($t_i+\tau_P<t_1+\tau_R$) the full area of the impulse response is the contribution to the weighting function:

$$w\left(t_0=t_1+\tau_R,t_i\right)=\frac{A}{C_T}\int_0^{\tau_p}p\left(x\right)dx \qquad t_1<t_i<t_1+\tau_R-\tau_p \qquad (2.83)$$

4. If the current impulse arrives after start of integration ($t_i>t_1$) and ends after the end of the integration ($t_i+\tau_P> t_1+\tau_R$), only the initial part of the pulse is integrated and contributes to the noise response at $t_0=t_i+\tau_R$:

$$w\left(t_0=t_1+\tau_R,t_i\right)=\frac{A}{C_T}\int_0^{t_1+\tau_R-t_i}p\left(x\right)dx \qquad t_1+\tau_R-\tau_p<t_i<t_1+\tau_R \quad (2.84)$$

Correlated Dual Sampling (CDS) methods are quite popular nowadays not only in strip and pixel detectors for Particle Physics, but also on CMOS cameras for imaging and on switched capacitor design in general. On [112] the noise of the double correlated sampling is studied as a time-variant filter using direct calculations of noise dispersion starting from noise spectrum density by means of the autocorrelation functions. In [117] the analysis is extended to multiple correlated systems. In [114] sampling methods, as correlated samplers, are also analyzed and noise expression for the gated integrator is also obtained as a limit in this case. An interesting method to perform noise analysis of time variant shapers in circuit simulators is also proposed. Concerning CDS noise analysis there are some important references in imaging and switched capacitor fields: [118], [119], [120] and [121].

2.6.6 Effect of measurement time T_m

If the ENC for the Triangular (2.79) and the Semi-Gaussian (2.80) shapers are analyzed, and assuming a charge sensitive preamplifier, some statements can be made:

- Parallel noise (white) is proportional to the square root of the measurement time: $ENC_P \propto \sqrt{T_m}$
- Series white noise is inversely proportional to the square root of the measurement time: $ENC_S \propto \frac{1}{\sqrt{T_m}}$
- Series *1/f* noise is independent from the measurement time. Usually, is quite independent of the shaper step response also [94].

These considerations can be extended to any shaper with finite step response ([94], [95], [10]). The general connection between the exponent α for an equivalent input voltage noise generator with power law spectrum $|f|^{\alpha}$ and the corresponding ENC is [95],

$$ENC(\alpha)^2 \propto T_m^{-(1+\alpha)} \qquad (2.85)$$

Although input parallel noise generator is white, it is integrated on the input capacitance and becomes $1/f^2$ in voltage or charge.

As is clear from Figure 2-13, an optimum measurement time T_{mOPT} where ENC is minimum must exists. Since, *1/f* has no influence on the T_{mOPT} the time domain approach can be useful to analyze T_{mOPT} for different shapers. Once T_{mOPT} it is found, it is possible to compare the ENC for the T_{mOPT}, i.e. $ENC_{TmOPT,}$ of different shapers.

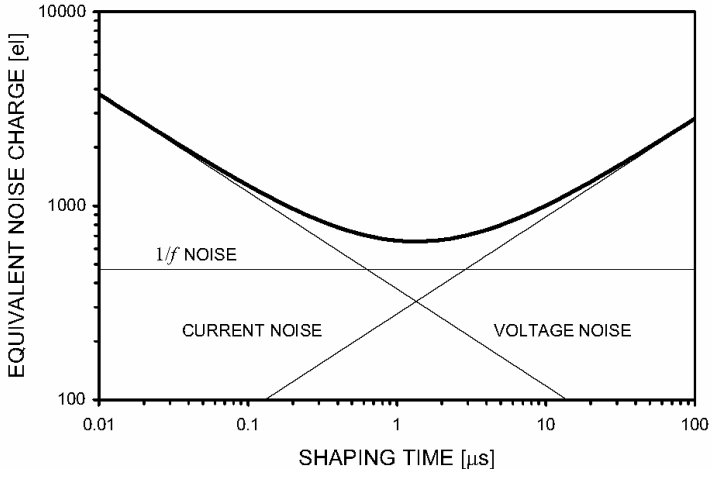

Figure 2-13. Generalized noise behavior of a system as the measurement or shaping time T_m is varied. Logarithmic scales are assumed.

According to [95] the integral of the system response squared is simply a measure of the width of the response and the integral of (2.73) corresponding for parallel noise can be written as

$$\int_{-\infty}^{\infty} w(t)^2 dt = a_{F2} T_m \qquad (2.86)$$

where T_m is proportional to the length of the weighting function (or the length of the impulse response for time invariant shapers) and a_{F2} is its form factor. Also, the integral of (2.73) corresponding for series noise can be written as,

$$\int_{-\infty}^{\infty} w'(t)^2 dt = \frac{a_{F1}}{T_m} \qquad (2.87)$$

where a_{F1} is the form factor of derivative of the weighting function. Substituting (2.86) and (2.87), in the normalized expression of the ENC (2.74),

$$ENC^2 = \frac{1}{2} e_n^2 \left(C_D + C_I\right)^2 \left[\frac{a_{F1}}{T_m} + \frac{1}{\tau_C} a_{F2} T_m\right] \qquad (2.88)$$

The optimal measurement time (or peaking time of the shaper) is the one that makes $\frac{\partial ENC^2}{\partial T_m} = 0$,

$$T_{mOPT} = \tau_C \sqrt{\frac{a_{F1}}{a_{F2}}} = \sqrt{\frac{e_n^2}{i_n^2}} \left(C_D + C_I\right) \sqrt{\frac{a_{F1}}{a_{F2}}} \qquad (2.89)$$

The optimal peaking time is proportional to the noise corner time constant τ_C times a constant, which depends of the form factor of the shaper.

Table 2-1 summarizes the optimal peaking time T_{mOPT} and its corresponding ENC_{TmOPT} of several common shapers.

Shaper	T_{mOPT}	ENC_{TmOPT} /ENC_{CUSP}
Cusp	∞	1
Triangular	$\sqrt{3}\tau_C$	1.07
DL-RC		1.1
Trapezoidal	$\sqrt{3}\tau_C$	$1.07\left[1+0.43\frac{T_{FT}}{\tau_C}\right]$
Semi-Gaussian 4th order (CR-$(RC)^4$)	$\sqrt{\frac{n^2}{2n-1}}\tau_C \approx 1,5\tau_C$	1.16
CR-RC	τ_C	1.36
Bipolar SG ($(CR)^2$-$(RC)^4$)	$\approx 0.74\tau_C$	1.38
Bipolar: $(CR)^2$-RC		1.41

Table 2-1. Optimal T_m and ENC for this T_m, relative to the optimal ENC, the ENC of the cusp function, of several common shapers. Flicker noise is not considered. Sources are [8], [94] and [105].

Although, minimizing the ENC is an important criteria to choose the peaking time of the shaper and the shaper itself (both are related as it has been shown), there are other points that need to be taken into account. It was already discussed the effect of shaping on pile-up and on ballistic deficit immunity. Crosstalk could be another point that could be considered. Crosstalk is usually related to capacitive coupling between signals, thus cross-talk signals have zero net area. Cancellation of induction and crosstalk signals requires a round-topped or, better, a flat topped shaper step response function of suitable duration (superposition of 2 impulses of equal area but with opposite polarities

yields a zero response at the measurement time provided that the shaper has a flat response time long enough and that measurement time is after crosstalk signal).

The phenomena that sets a lower limit to the peaking time, namely ballistic error, induction or crosstalk, combined with the pile-up effect which conversely sets an upper limitation to the processing, may lead to incompatible requirements.

If a compromise is found, the type of device or the technology used to implement the preamplifier have to be taken into account since they fix an optimal peaking time and this T_{mOPT} depends on the noise corner time constant τ_C which at his turn depends on the input series and parallel noise, and these parameters are quite different for bipolar junction transistor, JFETs or MOSFETS.

2.6.7 Noise sources in preamplifiers

Figure 2-14 shows an example [94] of ENC as a function of measurement time for three types of active devices and a fixed value of C_D=*30 pF* and detector leakage current I_D=*10* nA. Although absolute values have changed since this figure was generated, using theoretical expressions which are function of technological parameters that have evolved; some conclusions on the optimal range of operation of the different devices are still valid. The bipolar transistor has an optimum ENC at a value of a few tens of nanoseconds. The ENC for a junction field-effect transistor (JFET) would be a continuously decreasing function of T_m if the noise from the detector leakage current and bias resistors were not present: both contribute to parallel noise whereas JFET has negligible intrinsic parallel noise. A 10 nA detector leakage current shifts the value of T_{mOPT} to the 1μs range.

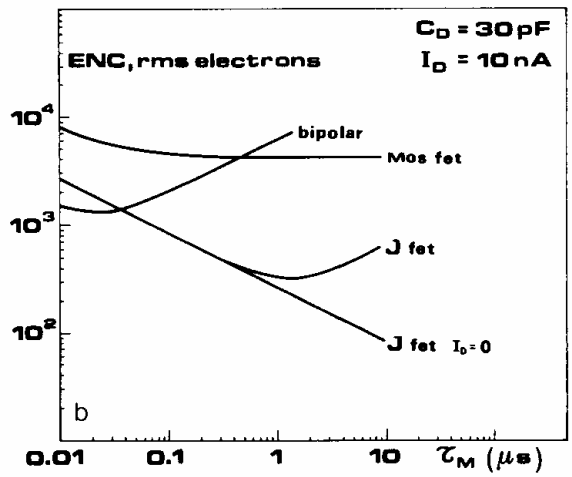

Figure 2-14. Example of ENC as a function of measurement time T_m or τ_M for three types of active devices and a fixed value of C_D=30pF and detector leakage current I_D=10 nA. [94].

The MOS transistor has an initial drop of the ENC as a function of T_m, which reflects the behavior of the white component in the spectral power density of the series noise, followed by a settling to the value determined by the *1/f* noise component. The ENC in Figure 2-14 was calculated in 1985 [94], as it will be explained later results for modern deep sub-micron CMOS technologies show that MOSFET can be nowadays the optimal solution in a wide range of peaking times.

In the system design, if a noise corner time constant much longer than the peaking time is achieved, i.e. parallel noise is made negligible, and then the total ENC (2.74) would approximately the ENC due to the series noise

$$ENC^2 \approx ENC_S^2 = \frac{1}{2} e_n^2 \left(C_D + C_I\right)^2 \int_{-\infty}^{+\infty} W_N'\left(t\right)^2 dt = \frac{1}{2} e_n^2 \left(C_D + C_I\right)^2 \frac{a_{F1}}{T_m} \qquad (2.90)$$

ENC^2 due to the series noise is a monotonic decreasing function with the T_m parameter and increases with the square of the sum of detector and input capacitances.

A detailed description of noise sources in different devices can be found in [77] and in [66]. The methods presented in section 2.4 should be used to determine the parallel and series input equivalent noise generators. As seen in section 2.4.5, when several amplification stages are cascaded the first one determines the SNR of the system provided that its gain is high enough. This should be the case in the preamplifier design: the first stage of a low-noise preamplifier should be carefully designed to optimize SNR and should have enough gain so that noise contributions of subsequent stages are negligible. Therefore, following considerations apply on the first stage of the preamplifier.

Some qualitative considerations will be made about noise sources for parallel, white series and flicker series noise sources of a preamplifier capacitively coupled to the detector:

- ***Parallel noise sources***. They are related to the shot noise on the leakage current of some detectors, on the gate current of field effect transistors and on the base current of bipolar transistors. As pointed out, gate current in JFETs can be almost negligible compared to detector leakage current.

  Conversely, shot noise in base current of bipolar transistors can be significant, for this reason the optimal peaking time of bipolar transistors is 1 or 2 orders of magnitude smaller than for field effect transistors: the noise corner time constant τ_C is inversely proportional to the parallel noise. In order to consider the bipolar transistor a competitor of a field effect transistor where parallel noise is negligible, the value of the peaking time T_m must be adequately short to make the parallel noise associated with the base current of the bipolar transistor acceptable.

- ***Series white noise sources.*** In JFETs, MOSFETS and GaAs field effect transistors it is related to the thermal noise in the channel[k]. Sometimes detectors and input field-effect transistors are operated at very low temperatures (using cryogenic systems) to achieve very low noise performance. The thermal noise in resistors and dielectrics is reduced according to equations. The thermally generated leakage currents are reduced, and so is their shot noise (this affects the parallel noise). The maximum reduction in the thermal (series) noise of field-effect transistors is about 30% at temperatures in the range of 120-160 K.

  In bipolar transistors series noise has two main contributions: a first one related to shot noise of the collector current and a second one due to the thermal noise in the base spreading resistance. In large discrete devices the base spreading resistance is usually less than 30 Ω, whereas in small devices in monolithic technology it can be as high as 200 Ω, and in those cases the base resistance can increase series noise significantly. However, bipolar transistors for modern HF technologies have a base spreading resistance quite low, and are used often when short shaping times are required.

  The thermal noise current PSD on the channel of the field effect transistors or the shot noise PSD on the collector current of bipolar transistors (BJTs) is converted to a input equivalent noise voltage dividing this PSD by the squared module of the transconductance of the device. Therefore, the higher the gain of a device the smaller the input series noise of this device for the same PSD on its channel or collector current. In [95] it is shown that the transconductance of transistor is proportional to the transition frequency or gain bandwidth product f_T (frequency at which the transconductance decreases to $1/\sqrt{2}$). It can be shown [94] that input series generator can be described with a single expression for either bipolar (not taking into account the effect of the base spreading resistance in this case) or field effect transistors,

$$e_n^2 = 2kT\frac{\aleph}{g_m} \qquad (2.91)$$

[k] This is true for a MOS biased at strong inversion. In weak inversion region, the dominant source of noise becomes shot noise.

where $\aleph$ is a constant that depends on type of device and g_m is transconductance. It can be also shown that the g_m/C_I represents the gain bandwidth product of the device $\omega_T = 2\pi f_T$ ([66], [94]). Equation (2.90) can be, therefore, written

$$ENC_S^2 = 2kT\frac{\aleph}{\omega_T}\frac{\left(C_D + C_I\right)^2}{C_I}\frac{a_{F1}}{T_m} = 2kT\frac{\aleph}{\omega_T}\frac{a_{F1}}{T_m}\left[\sqrt{\frac{C_D}{C_I}} + \sqrt{\frac{C_I}{C_D}}\right]^2 C_D \quad (2.92)$$

The gain bandwidth product increases with the bias current, collector current for BJTs[1] or drain current for FETs (more precisely with the overdrive), and as the inverse of the critical device dimension across which carries are in transit ([66]). For BJTs this dimension is the base width and it is a vertical dimension determined by diffusion or implants and can typically be made much smaller the dimension for FETs, the channel length of a FET, which depends on surface geometry and photolithographic processes. Thus BJTs generally have higher f_T than FETs made with comparable processing. However, due to short channel effects for submicron MOS transistors devices f_T is proportional to L^{-1} rather than L^{-2}. For these reasons scaling down in MOS technologies increases the f_T and reduces the equivalent input series noise.

Thus, the theoretical limit of the series noise of a device is related to its transition frequency, although other factors like the effect of base spreading resistance for bipolar transistor will make the series noise exceed this theoretical limit. Microwave transistors with f_T as high as 90 GHz (GaAs MESFETS, for example) would appear to be very attractive, however they are usually limited by other factors such as flicker noise.

- ***Series 1/f noise sources.*** Silicon MOS field-effect transistors and gallium arsenide metal-semiconductor field-effect transistors (GaAs MESFETs) are known to have a relatively high *1/f* noise compared to JFETs and bipolar transistors. This *1/f* noise appears as fluctuations in charge in the gate channel interface, which modulate the conducting channel. The noise that modulates the conducting channel appears as an equivalent voltage generator in series with the gate.
- ***Noise in feedback network.*** Many preamplifiers are implemented in closed loop configuration, therefore noise generated by the feedback network should be considered. It may include capacitors, resistors (that contributes to parallel noise generator), switches (for reset the feedback capacitances of a charge sensitive loop) and even active linear components. For capacitors, it has to be pointed out that thermal fluctuations in dielectrics generate a noise the magnitude of which is quantitatively related to the parameters describing dielectric losses. It can be shown [95] that the dissipative dielectric acts as a source of *1/f* noise in parallel with the detector at the preamplifier input.

New trends in the front-end design ([13] and [40]) have appeared as a consequence of the advancement in CMOS processes known as device scaling. The device scaling has considerably reduced the gate length, entering the submicron and deep submicron regions, by virtue of which devices with gate length down to 60 nm are nowadays available. Perhaps even more importantly, it acted also in the sense of reducing the thickness of the gate oxide to a few nanometers. The reduction in the gate oxide thickness t_{ox} to the few nanometer region has produced a considerable reduction of *1/f*-noise in the submicron CMOS families. The *1/f*-noise has attained acceptably low values in the P-MOSFET, although in terms of absolute improvement the effect on the N-MOSFET has been quantitatively more evident. A thinner gate oxide and a shrinking in the gate length have also upgraded the behavior of the high frequency noise (frequency independent or white) at reasonably small standing currents, i.e. the f_T increases with the device scaling down. Although a JFET still has a better noise behavior at very long peaking times, it is outperformed by a submicron channel MOSFET at short or medium peaking times. This is shown in Figure 2-15, where a P-channel MOSFET, which belongs to a process of 0.35 μm minimum gate length and 7.2 nm gate oxide thickness, and a N-

[1] For bipolars the f_T as function of collector current has maximum, it declines at high currents. It is due to an increase of the base transit time in forward direction, which is the theoretical upper limit for $1/2\pi$ f_T, caused by a high level injection and Kirk effect at high currents.

channel JFET, that belongs to a JFET-CMOS process which has a gate length of 1.2 μm, are compared.

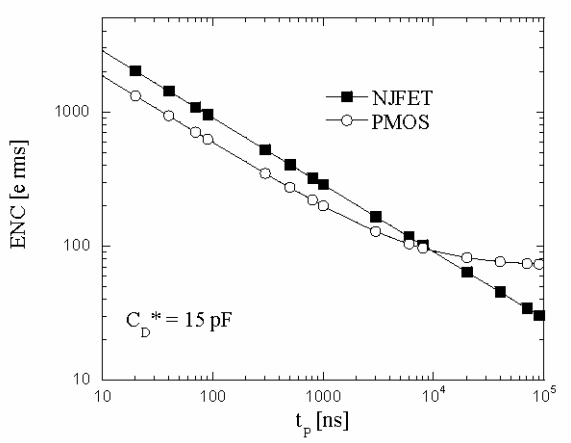

Figure 2-15. Contributions to ENC of NJFET and PMOS transistors, as a function of the peaking time t_p. Figure taken from [13].

The JFET has been set to operate at a current (500 μA) which is twice as much that of the MOSFET (250 μA) to partially offset the difference in channel lengths. In spite of this, the series noise voltage spectrum of high-frequency (white) noise in the N-JFET is about $2nV/(Hz)^{1/2}$, against the $1.3nV/(Hz)^{1/2}$ of the P-MOS. In [41] a 0.25μm CMOS technology with gate oxide thickness equal to 5.5 nm is studied, obtaining also a series white noise voltage spectrum close to $1.3nV/(Hz)^{1/2}$ for a drain currant of 500 μA. All these results are obtained at room temperature.

In mixed-signal detector readout systems, power dissipation constraints set an upper limit on the drain current in the preamplifier input device. In most cases, this means that the device is operating close to the weak inversion region [38]. The noise performance of two 0.13μm CMOS processes, from IBM and ST, has been studied in [38]. The analysis of the experimental results shows that the behaviour of the white noise term is consistent with equations valid in weak inversion, independently of the fabrication process, with some limitations concerning NMOS devices with a channel length close to the minimum allowed by the technology. As expected from past experience on previous CMOS generations, *1/f* noise is dependent on the fabrication technology and it is very difficult to derive a general law correctly describing the behaviour of this noise term. At a drain current of 1 mA and 10 kHz the *1/f* noise contribution appears to be larger in NMOS than in PMOS by about a factor of 10 for devices with the minimum channel length while a lower difference appears for longer channels. The study has been extended to 90 nm CMOS ST technology [39], the *1/f* noise coefficient K_f is larger for devices with channel length close to the minimum allowed by the technology and is lower in the 90 nm process with respect to 130 nm process. Moreover, it is independent of the drain current in the NMOS while in PMOS it increases with the overdrive voltage.

As was said before, the noise PSD for the input equivalent series generator depends on the transconductance of the device, which at turns depends on the bias current. Bias current could be limited by power dissipation, especially in modern HEP collider experiments where a lot of channels are needed in small areas. In Figure 2-16 ([60]) it is shown an interesting comparison of the performances of several charge preamplifiers, very useful to illustrate this fact and the implications of the technology scaling down.

CSP	Schmitt *et al* (1987) [19]	Binkley *et al* (1992) [20]	Paulus *et al.* (1996) [21]	Binkley *et al.* (2000) [22]	**5-mW CSP**	**1-mW CSP**
e_n	0.9 nV/Hz$^{1/2}$	1.6 nV/Hz$^{1/2}$	1.1 nV/Hz$^{1/2}$	0.65 nV/Hz$^{1/2}$	**0.57 nV/Hz$^{1/2}$**	**0.83 nV/Hz$^{1/2}$**
Current	20 mA	5 mA	10 mA	2 mA	**3 mA**	**600 µA**
Technology	Discrete MOS FET	2 µm	2 µm	0.8 µm	**0.18 µm**	**0.18 µm**
Time Resolution (FWHM)	0.9 ns	9.2 ns	1.57 ns	1.15 ns	**1.56 ns**	**2.49 ns**
Rise time (0 pF)	5 ns	22 ns	7 ns	6 ns	**7 ns**	**9 ns**
Power	300 mW	25 mW	50 mW	10 mW	**5 mW**	**1 mW**

Figure 2-16. Input equivalent series voltage for several CSP (for Positron Emission Tomography (PET) imaging. References in this figure correspond to references in the original paper of the figure [60]. Last columns correspond to performance of circuits presented by the authors (2004).

The question which naturally arises in the presence of a BiCMOS technology is whether some particular low-noise situations may benefit from the availability of the bipolar transistor. In order to consider the bipolar transistor a competitor of a MOSFET, the value of the peaking time T_m must be adequately short to make the parallel noise associated with the base current of the bipolar transistor acceptable. The theoretical value of the relevant voltage noise spectral density, calculated as $2kT/g_m$, where g_m = 10 mS at the collector current of 250 µA, would be about 0.9 nV/(Hz)$^{1/2}$ (see [13]). To outperform the MOSFET from the standpoint of high frequency noise, however, the bipolar transistor should feature a base spreading resistance of less than 50 Ω, a value which is not so easily achieved in a bipolar transistor part of a monolithic process. As a conclusion, the bipolar transistor might be a competitor of the short channel MOSFET provided that the two following conditions are met:

- The value of T_m is in the 10 nanoseconds region or shorter.
- The base spreading resistance of the bipolar transistor can be accurately controlled.

In detectors not capacitively coupled with preamplifier, such as photomultipliers that have a small load resistance, parallel noise introduced by the amplifier is less important (see 2.4.2), therefore, range of applications of bipolar technologies in those cases is much wider. However this configuration is not optimal for detectors providing very weak signals, because the load resistor introduces a significant source of parallel noise.

CMOS processes featuring a SiGe bipolar transistor are appearing on the scene also. Attention must be paid to the value of the base spreading resistance and to the *1/f* noise in the base and collector current. In a charge measuring system a parallel noise component with a *1/f* spectral density appears at the output of the charge-sensitive loop as a $(1/f)^3$ component after being integrated on the feedback capacitance. This spectral density would yield a divergent ENC contribution with a unipolar shaping. This means that the use of SiGe transistor as a front-element requires an accurate control of the amount of the *1/f* component in the base current noise and suitable attention in the design of the signal processor. In [122] the possibility to use heterojunction bipolar transistors (HBTs) based on SiGe technology for the front end of SLHC trackers is studied. The HBTs characterised by much higher cut-off frequencies and lower base spread resistances. In [122] it is shown that the operation principle, and so the physics of noise phenomena, in HBTs are the same as in BJTs. A combination of large detector capacitance, short shaping time, and low power consumption constraints might favour the use of HBTs because of its higher f_T (between 30 and 40 GHz for I_C=100 µA [122]). However, SiGe transistors suffer from radiation damage in a similar way as conventional bipolar junction transistors and performance of these devices after irradiation with particle fluences up to $1 \cdot 10^{15}$cm^2, as foreseen for the silicon strip detectors in the super-LHC environment, still has to be evaluated.

Some developments have been made also in GaAs MESFETS. In [61] a cryogenic charge-sensitive preamplifier with very low noise and large dynamic range was developed and fabricated using a GaAs MESFET process is presented. Output signals reaching 10 V and a white series noise level of 0.2nV/(Hz)$^{1/2}$ have been verified at 77 K. The GaAs has an optimum behaviour at cryogenic temperature, where the *1/f* descends.

2.6.8 Capacitive matching between detector and preamplifier

It has just shown that the series and parallel noise depend on technology and design of the preamplifier, but its impact on the SNR or ENC of the system depends at the end also on the shaper characteristics, on the shaping time and on the detector and, in the case of series noise, on the detector and preamplifier input capacitances as it has been shown in (2.74) and in (2.92). According to (2.92), the ENC due to series noise attain a minimum when C_I is made equal to C_D, that is, when the preamplifier is capacitively matched to the source: the detector. The value of such minimum is,

$$ENC_{S_{CM}}^2 = 8kT\frac{\aleph}{\omega_T}\frac{a_{F1}}{T_m}C_D \qquad (2.93)$$

The capacitive matching condition corresponds to the best transfer of the energy available at the source capacitance (detector) to the load capacitance (preamplifier). This condition is also valid for the flicker series noise.

In the case of the bipolar transistor the base spreading resistance also contributes to the serial noise. This contribution and the non-negligible parallel noise causes that the value of C_I for optimal ENC in bipolar transistors differs from the capacitive matching condition [94].

In the case of MOSFET transistors, ω_T depends on the overdrive which depends on dimensions of the transistor if it is operated at fixed current. Dimensions of the transistor also determine the input capacitance, therefore, optimization of (2.92) also involve ω_T. On fixed current operation it can be shown that the optimal preamplifier input capacitance is C_I =1/3 C_D [105]. If the MOSFET is operated at fixed current density (overdrive independent of transistor dimensions) ω_T is independent of dimensions and capacitive matching C_I=C_D holds, same result applies for JFET front ends. For MOFETS the minimal channel length is chosen to achieve the maximum ω_T and the optimization is done on the channel width.

Large values of W/I_D ratio eventually leads to weak inversion operation. In this case g_m is independent of W so any increase of W degrades the ENC. Therefore, the capacitive matching might not be the driving condition to minimize the ENC and to choose the dimensions of the input transistor ([105], [111]).

Moreover, in fixed current operation different optimal values of C_I are obtained for series noise and for *1/f* noise. The optimal value for the dominant noise source must be chosen ([105], [62] and [106]). For fixed current density operation, optimal value of C_I is the same for series noise and for *1/f* noise.

Matching of high capacitance detectors without an impractical increase in the device size, noise (magnetic losses in the core) and power dissipation can be achieved with a transformer. This solution can not be adopted in experiments that make use of strong magnetic fields.

However, it is also possible to achieve a capacitive matching (or optimal C_I in the case of bipolars and MOSFETs) by controlling the capacitance of input device of the preamplifier:

- For technologies employing field effect devices it is possible to control the input capacitance of the input transistors though a proper scaling of its width and its length. Of course, to adjust these parameters other factors like gain, bandwidth or power dissipation have to be considered, as said before.
- In bipolar transistors, within the range of values of the collector current where the gain-bandwidth is independent of this current and with a negligible junction capacitance, so that C_I can be determined by the diffusion term alone, transconductance and input capacitance are, within a good approximation, linear functions of the collector current. Therefore, to achieve capacitive matching there are two parameters available: the number of device that can be connected in parallel and the collector current. Parallelizing bipolar transistors also decreases the total base spreading resistance and its corresponding term in series noise.

It is important to optimize the design of the preamplifier to achieve an optimal SNR, taking into account the noise sources for a given technology, the capacitive matching condition (or optimal capacitance for BJTs and MOSFETs) and other factors like power dissipation or linearity. This is done systematically in [105], [62], [106] and [126] for CMOS technologies, in [42] and [43] for bipolar transistors and in [44] for DMILL technologies. DMILL is a technology which realises devices of four different types, NPN bipolar transistors, P-channel JFETs, N and P-channel MOSFETs on separate insulating layers, thereby removing any compatibility problem.

After this discussion one may ask: "Which is the smallest ENC achievable with a preamplifier?" The preamplifier should be optimized but at the end, depends mainly on the shaping time T_m and on the detector capacitance C_D. For example, in [95] an ENC of the order of 10 r.m.s. electrons is reported for Silicon (Si) X-Ray detectors with $C_D \approx 1$pF and T_m=100 ms operated at 120K, and for Charge Coupled Devices (CCDs) and Si drift chambers with $C_D \approx 0.1$pF and T_m=1-10 μs. However, fast detectors (gas drift detector or Si strip detectors) with $C_D \approx 10$pF and T_m=10-100 ns have an ENC of thousands of r.m.s electrons. Large calorimeters with $C_D \approx 1$μF and T_m=1-10 μs, have a high ENC of 10^5 r.m.s. electrons.

There many works where systems with ENC of few electrons at room temperature are being studied [124]. Pixel radiation detectors made on epitaxial silicon carbide have very small leakage currents (order of fAs), and in terms of equivalent noise charge, the contribution of most of the pixels is lower than 1 electron root mean square (r.m.s) up to peaking times of tens of s of pulse shaping. These pixel detectors are ready for applications in ultimate-resolution X-ray spectroscopic imaging at room temperature when a suitable ultra low noise front-end electronics, presently not available, will be developed.

New systems like the monolithic active pixel sensors (MAPS) are pixel detectors with the sensor (a reverse biased diode) and the preamplifier integrated on the same substrate and for this reason detector capacitances are extremely low. Typical collection times are on the order of about 100 ns. Results of ENC of about 10 r.m.s electrons are reported [49]. With monolithic solutions the capacitances can be as low as few tens of fF, and it is possible to achieve ENC of less than 10 electrons, even with shaping times in the μs range.

Charge sensing elements for charged particle detection with a first amplification stage built into the device were proposed in order to increase SNR. The signal amplification is achieved through modulation of the current conveyed via the transistor by a voltage variation on the inner node capacitance. For example the DEPFET [52] or the photoFET [49] address very low noise operation manifested in ENC of about 5 r.m.s electrons for a shaping time of 10 μs and at room temperature. Furthermore, in [125] it is theoretically and experimentally shown the capability to reduce the readout noise of an optical and X-ray photon detector based on the semiconductor DEPFET device below a level of only $0.3e^-$ ENC. The readout method used is called "Repetitive Non Destructive Readout" (RNDR) and was realised by placing two single DEPFET-devices next to each other and by coupling their charge storing region by an additional gate.

2.7 Timing measurements

In timing measurements the slope-to-noise ratio must be optimized, rather than the signal-to-noise ratio alone, so the rise time t_r of the pulse is important. The "jitter" σ_t of the timing distribution

$$\sigma_t = \frac{\sigma_n}{\left(dS/dt\right)_{S_T}} \approx \frac{t_r}{S/N} \qquad (2.94)$$

where σ_n is the r.m.s noise and the derivative of the signal dS/dt is evaluated at the trigger level S_T. To increase dS/dt without incurring excessive noise the amplifier bandwidth should match the rise-time of the detector signal. The 10 to 90% rise time of an amplifier with bandwidth f_U is t_r=0.35/ f_U (first

order low pass filter response). For example, an oscilloscope with 350 MHz bandwidth has a 1 nanosecond rise time. When amplifiers are cascaded, which is invariably necessary, the individual rise times add in quadrature[m].

Increasing signal-to-noise ratio improves time resolution, so minimizing the total capacitance at the input is also important. At high signal-to-noise ratios the time jitter can be much smaller than the rise time. The optimum weighting function for time measurements is obtained as the convolution of the cusp filter with the derivative of the input current pulse. The timing distribution may shift with signal level ("walk"), but this can be corrected by various means, either in hardware or software. For a more detailed revision on timing measurements see [59] or [111].

2.8 Other possible sources for degradation of resolution

The previous discussion analyzed random noise sources inherent to the sensor and front-end electronics. In practical systems other phenomena often limit the obtainable detection threshold or energy resolution:

- Interference or pickup noise. Interference sources couple into an electric circuit by one of four means: a current through an impedance, termed conductive coupling, an electric field, termed capacitive coupling, a magnetic field, termed inductive coupling, or an electromagnetic field at high frequencies. The techniques to provide a safe and stable common ground for a system to avoid conductive coupling and ensure a stable common reference signal, are are called grounding. Shielding minimizes capacitive and inductive interference by reducing, respectively, the mutual capacitance and inductance between the interference source and the victim circuit. Other techniques like decoupling are also important to control interference.
- Drifts. Variation of components with time or temperature is called drift. For example, random noise whose frequency is below 0.1Hz or sometimes 0.01Hz is termed drift. Some techniques as differential design are important to reduce the sensitivity of the system to time or temperature drifts.
- Environmental noise or pseudonoise. It is a random fluctuation in electronic circuits that is not inherent to the electronic behavior of the components themselves (noise). It is produced by environmental factors such as temperature, humidity or vibration. Temperature changes affect not only semiconductors, but also conductors because of thermoelectric effects.

It is far from the scope of this document to review these sources of potential problems because they are very dependent not only of a given circuit or a subsystem but on the complete environment., [79] or [80] are good sources of documentation. Nevertheless, as a general comment, differential design is recommended to deal with interferences, drifts and any error source coupled as a common mode signal.

In a modern HEP experiment there are about 10 different subsystems with thousands of different cards and crates, therefore it is very important to take into account grounding and shielding. For instance, the LHCb experiment has a common defined policy which is documented in [130] and [131].

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[m] This is not always true. This results derives from the central limit theorem, which applies well to the sort of lowpass-filtering effects found in I/O drivers, scope probes, BNCs, and other simple one-pole linear systems. Technically, the central-limit theorem says that for large values of N, a cascade of N lowpass filters tends to produce a Gaussian frequency response with a step-response rise time that grows in proportion to □N. For this result to hold true, the theorem requires that the impulse response of each individual filter have a finite mean, a finite variance, and a monotonic step response. In the frequency domain, these conditions imply that near dc, the transfer response of the filter must be flat with a finite curvature. Curiously, both the skin effect and dielectric-loss mechanisms violate the flatness conditions; therefore, the central-limit theorem does not apply to lossy transmission lines. See: "*Rise time of lossy transmission lines*" H. Johnson, EDN, 10/2/2003

3 SPD signal processing

In this chapter we will discuss the requirements of the front system presented in this document. It is specifically designed for the calorimeter system of the LHCb experiment, to provide a fast input to the trigger system. First, the LHCb experiment and the subdetectors of the calorimeter system will be briefly described. Secondly, after analyzing the signal characteristics and other constraints of the experiment, basic requirements for the readout electronics will be derived. Finally the proposed solution to fulfill those requirements will be presented.

3.1 The LHCb experiment

The Large Hadron Collider (LHC) at CERN, Geneva, will collide protons at a centre-of-mass energy of 14 TeV with a frequency of 40MHz. The accelerator will be housed in the 27 km tunnel that has been built for the LEP collider. LHC is scheduled to start data taking in summer 2008. The clear objective is to get the luminosity to $10^{33}cm^{-2}s^{-1}$ during 2008 operation. Then the luminosity will be increased to $10^{34}cm^{-2}s^{-1}$, its nominal one, in the next few years. The total cross-section at LHC energy is conservatively assumed to be ≈100 mb and the $b\bar{b}$ total cross section to be ≈500μb. Furthermore b and $\bar{b}$ pairs production are correlated. They are predominantly produced in the same forward or backward cone, so that a forward spectrometer like LHCb (Figure 3-1, see [1], [2], [3]) will have an acceptance similar to the one of a central detector like ATLAS or CMS to capture both produced b-hadrons.

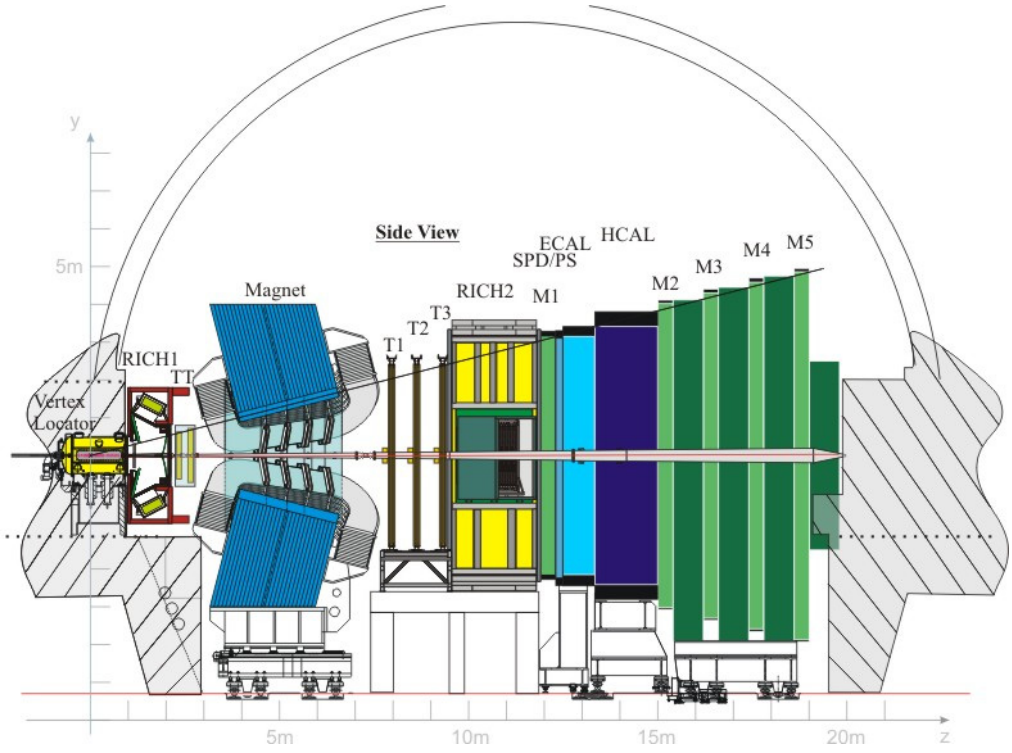

Figure 3-1. Layout of the LHCb spectrometer.

LHCb will run at a reduced luminosity of $2\times10^{32}\text{cm}^{-2}\text{s}^{-1}$, obtained by controlling the focus of the beam at the LHCb interaction point. This has been chosen to optimize the number of single interactions per crossing to produce clean events and also to facilitate the triggering and reconstruction. This permits also to make radiation damage in the forward region more manageable. LHCb is a single arm spectrometer. It consists of a silicon vertex detector (VELO) which includes a pile-up system surrounding a beam pipe, a magnet and a tracking system, two RICH counters, a calorimeter system and a muon detector. All detector subsystems, except for RICH1, are split into two halves that can be separated horizontally for maintenance and access to the beam pipe.

3.1.1 The VELO

The vertex locator (VELO) is installed inside the vacuum tank at the interaction region. It is made of series of 21 detector stations placed along the beam line covering a distance of about 1 m. It represents 0.23 m^2 of silicon, read-out in 170 Kchannels. Each station consists of two pairs of half-circular Si microstrip detectors; one with sensors with strips at constant radius (r-sensors) and one with sensors with quasi radial strips (φ-sensors). The sensors are made from 220μm thin silicon. The strip pitch and length varies as a function of the radial position of the detectors during LHC beam injection, they can be retracted to a distance of 3 cm from the beam line and hence the sensors are placed in Roman pots. They are separated from the LHC vacuum by a 250 μm thick Al foil.

In addition to the 21 VELO stations there are two *r*-disks upstream of the interaction point, which make up the Pile-Up System. It is used in the first level trigger for identifying multiple interaction events and for measuring the luminosity and track multiplicity.

The VELO provides a resolution on the primary vertex of about 8 μm in (*x,y*) and 44 μm in *z*.

3.1.2 The tracking system

In addition to the VELO, the LHCb tracking system consists of one tracking station before the magnet (TT) and three tracking stations behind the magnet (T1–T3). It is used to measure angles and momenta and provides a momentum resolution of $\frac{\delta p}{p} \simeq 0.37\,\%$. For example the mass resolution is about 14 MeV for $B_s \rightarrow D_s K$ decays. The track finding efficiency is ≈94 % for tracks with hits in all tracking stations (for p> 10 GeV/c).

To achieve a precision on momentum measurements of better than half a percent for momenta up to 200 GeV/*c*, the LHC dipole provides integrated field of 4 Tm. The warm magnet has an aluminium conductor and is centred at $z\approx5$m. Its weight is 1600 tons and its power consumption is 4.2 MW. Magnetic field has been introduced between the VELO and the magnet, *i.e.* in the region of RICH1 and TT, for Level-1 trigger improvement. The magnetic field will be regularly reversed to reduce experimental systematic errors in CP violation measurements.

Each tracking station consists of 4 layers. The outer layers (1 and 4) have vertical readout strips (*x*–layers) to measure the track coordinates in the bending plane. The inner layers (2 and 3) are rotated by a stereo angle of +5º and -5º respectively. The first station is the Trigger Tracker. It consists of four planes of silicon microstrip detectors with a pitch of 198 μm. Strips have lengths of up to 33 cm with a thickness of 500 μm. They amount to a total surface of approximately 8.3 m^2 of silicon and to 180k readout channels. The four layers are arranged in two pairs, with a gap of 30 cm between second and third detection layers.

The three remaining stations are placed behind the magnet with equal spacing. Each station consists of an Inner Tracker (IT) [8] close to the beam pipe and an Outer tracker (OT) [9] surrounding the IT. The IT uses silicon microstrip detectors with a pitch of 198 μm. Strips have lengths of up to 11–22 cm with a thickness of 320–410 μm depending on the location. They amount to a total surface of

approximately 4.2 $m^2$of silicon and to 130k readout channels. The OT is made of 5 mm × 4.7 m straw tubes, with a fast drift gas, allowing signal collection in less than 50 ns. It consists of about 50k readout channels.

3.1.3 The RICH

Two Ring Imaging Cherenkov detectors (RICH1&2) are used for charged hadron identification. They are made with three radiators: Aerogel and C_4F_{10} for RICH1, sited upstream of the magnet, which has an angular coverage 25–300 mrad and CF_4 for RICH2 which has an angular coverage 15-120 mrad. They provide greater than 3 $\sigma\pi/K$ separation over the momentum interval 3 $<p<$ 80 GeV/c. The photodetectors used are 1024-pixel Hybrid Photodiodes (HPD) developed by LHCb.

3.1.4 The calorimeter system

The calorimeter system ([134]) consists of 4 subdetectors. A Scintillating Pad Detector (SPD) to distinguish charged particles from photons is followed by a 15 mm lead wall (2.5 X_0) and a Preshower (PS) made with the same technology. The detector elements are 15 mm thick scintillator pads. A groove in the scintillator holds the helicoidal WLS fiber which collects the scintillation light. The light from both WLS fiber ends is sent by long clear fibers to 64-anode photomultipliers tubes that are located above or below the detector. Just after is the Electromagnetic Calorimeter (ECAL) based on the Pb/scintillator Shashlik type (25 X_0,1.1 λ_I), followed by the Hadronic Calorimeter (HCAL) based on the iron/scintillator tile type (5.6 λ_I). SPD, PS and ECAL are made of 6016 channels while HCAL has 1488 channels.

They provide electron, photon and hadron (including π^0) identification and play a central role in the Level-0 trigger. Their readout is performed every 25 ns. The efficiency to identify an electron is expected to be $\varepsilon(e \to e) = 95\%$ for a misidentification rate $\varepsilon(\pi \to e) = 0.7\%$. In a test beam, an energy resolution of $\frac{\sigma E}{E} = \frac{8.3\%}{\sqrt{E}} \oplus 1.5\%$ for the ECAL and $\frac{\sigma E}{E} = \frac{75\%}{\sqrt{E}} \oplus 15\%$ for the HCAL has been measured.

3.1.5 The muon system

The muon system consists of 5 stations of 1380 Multi Wire Proportional Chambers (MWPC). M1 in front of the calorimeter system and M2–M5 behind it, interleaved with iron shielding plates. M1 is used mainly to improve the momentum resolution in the first level trigger. It consists of two layers of MWPC, while the other four stations are made from four layers. This represents a total surface of approximately 435 m^2, readout in 26k channels and a hadron absorber thickness of 20 λ_I. The system provides efficient muon identification, typically 94% for a pion misidentification rate below 1%. Highest p_T muons are selected and used for Level-0 trigger.

3.1.6 The trigger system

The LHCb trigger is dedicated to select *b* decays of interest. It is subdivided in two trigger levels, called Level-0 and HLT. The aim of Level-0 is to reduce the LHC beam crossing rate of 40 MHz which contains about 10 MHz of crossings with visible *pp* interactions at the LHCb luminosity, to a rate of about 1 MHz at which in principle all sub-systems could be used for deriving a trigger decision. It preselects the "highest p_T" (>1–2 GeV/c) muon tracks and highest E_T calorimeter clusters (e, γ, π^0 and hadrons) which information is collected by the Level-0 Decision Unit (L0DU) to select

events. With simple arithmetic, L0DU combines all signatures into one decision per crossing. Events can be rejected based on global event variables such as the total transverse energy deposited in HCAL, the charged track multiplicities, or the number of interactions as reconstructed by the Pile-Up system. To be fast it is implemented on hardware.

The HLT algorithms will be implemented on a commodity processor farm, which is shared between HLT and offline reconstruction algorithms. The HLT algorithm sstart with a pre-trigger which aims at confirming the Level-0 decision with better resolution, followed by selection algorithms dedicated to either select specific final states, or generic cuts to enrich the *b*-content of about 200 Hz. The efficiency achieved by the Level-0 trigger varies between 30% and 60% depending on the final states, whereas the HLT efficiency will reach nearly 100%.

3.2 SPD signal

3.2.1 SPD signal conversions: from beam to charge

The four LHCb calorimeter systems are shown in Figure 3-2. They provide high energy hadrons, electron and photon candidates for the first level trigger (called L0 trigger) of the experiment.

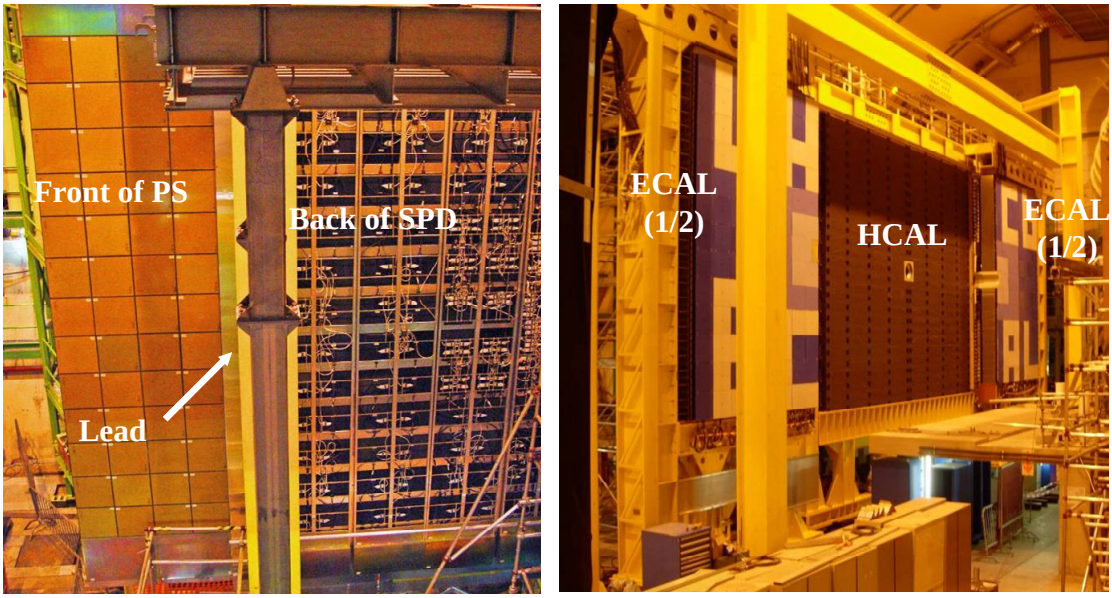

Figure 3-2. View of the calorimeter system. Left: PS and SPD. Right: ECAL (open) and HCAL before PS/SPD installation.

The SPD is designed to distinguish charged particles from neutral particles for the LHCb first level trigger. It is a binary output detector. SPD and PS are two sub-detectors in front of ECAL separated by a 1.5 cm thick layer of lead. They consist in a layer of plastic scintillator (Bicron BC-408) tiles with a Kurarai Y11 WLS (wavelength shifting) rolled fiber to collect the light emitted by the scintillator when a charged particle goes through it. The 5952 cells are distributed in three different sizes in order to obtain better granularity near the beam and more uniform occupancies. As in ECAL, there are three zones in SPD/PS: the outer with $12\times12\text{cm}^2$ tiles, the middle with $6\times6\text{cm}^2$ tiles and the inner with $4\times4\text{cm}^2$ tiles. Charged particles will produce, whereas photons will not, ionization on the scintillator. This ionization generates a light pulse that is collected by the WLS fiber that is twisted inside the scintillator cell. The light is transmitted through a clear fiber to the SPD readout system.

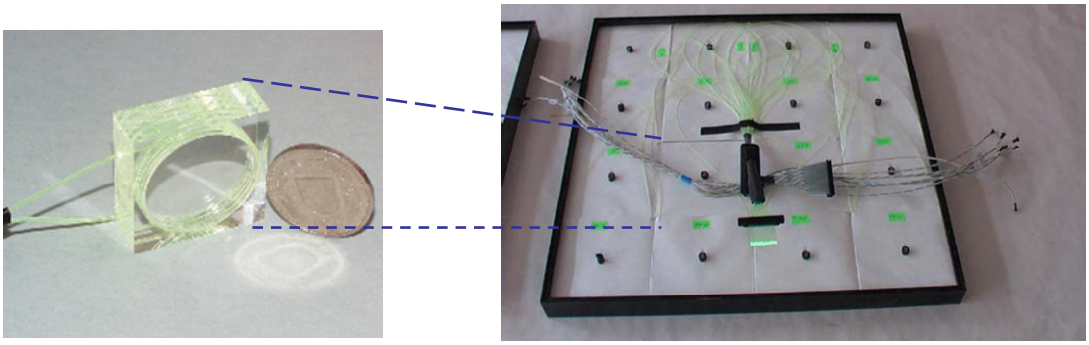

Figure 3-3. Scintillator cell (left) of the PS/SPD system and module with 16 cells (right).

An overview of SPD readout system is shown in Figure 3-4. The signal of the scintillator pads is processed in a Very Front End (VFE) unit, which includes a photomultiplier (PMT) to convert the light pulse into charge, the electronics to perform the discrimination between electron and photon signals, a bunch crossing clock receiver, a control unit and a LVDS serialiser to send the information to the PS/SPD Front End boards (FEBs). For economical reasons a multianode MaPMT is chosen as photodetector, the Hamamatsu R7600-M64 [135].

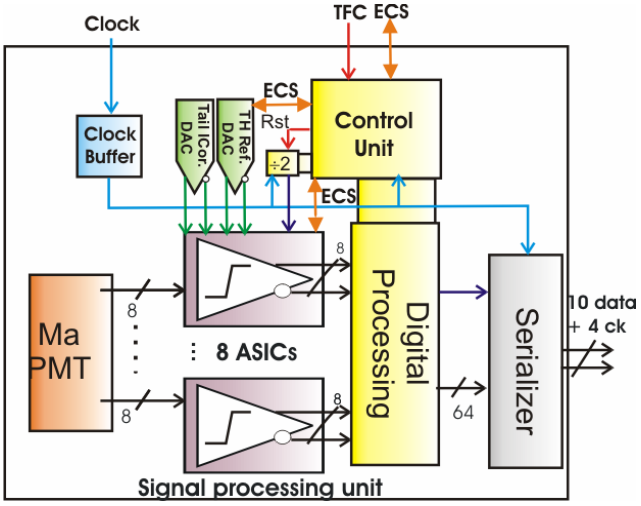

Figure 3-4. SPD readout system.

Each VFE unit is implemented through three boards: one containing the PMT, a second one with the analog signal processing circuitry and a third one with the control unit, the serialiser and the connectics. It is decided to install the analogue processing unit in the PMT base board to improve the SNR and to be able to simplify the interconnections and the PS FE boards by transmitting digital multiplexed information. There are two external (no on-chip) DAC with I2C interface to set some analogue references for the signal processing part. The control unit, the digital processing and clock divider to obtain the 20 MHz clock that controls the ASICs operation are implemented through a re-programmable FPGA, the ProAsic Plus Actel APA300. Triple Voting Registers (TVRs) are used to minimize possible SEU errors. The digital processing consists on mapping the PMT channel to a given serialiser channel to match the PS and SPD detector cell and to inject arbitrary patterns to test the detector data flow.

The Hamamatsu R7600-M64 presents non-negligible gain non-uniformities among its 64 channels. Typical gain uniformity (relative difference of gain between channel with highest gain and channel with lowest gain) is around 2 but some PMTs could reach a factor 3. The light generation and collection system also presents some non-uniformities. The SPD read out system must be able to deal with this problem.

Ideally only charged particles would generate a signal. The signal corresponding to the typical energy deposited by a charged particle with minimal ionization power (it depends on the particle

momentum [74]) is termed Minimum Ionizing Particle (MIP) signal. However, high energy photons can create an electron through secondary processes such as Compton Effect or pair production. These phenomena produce a photon energy spectra with a maximum at 0 but with a small tail for high energies (see Figure 3-5, where 1 MIP corresponds to about 2.85 MeV of deposited energy in scintillator), this provokes misidentification of photons taken for electrons as measured in a tagged photon test beam at CERN SPS ([136] and [137]). Applying a cut between 0.4 and 0.7 MIP is a good compromise to reject the photons with minimum losses for the trigger.

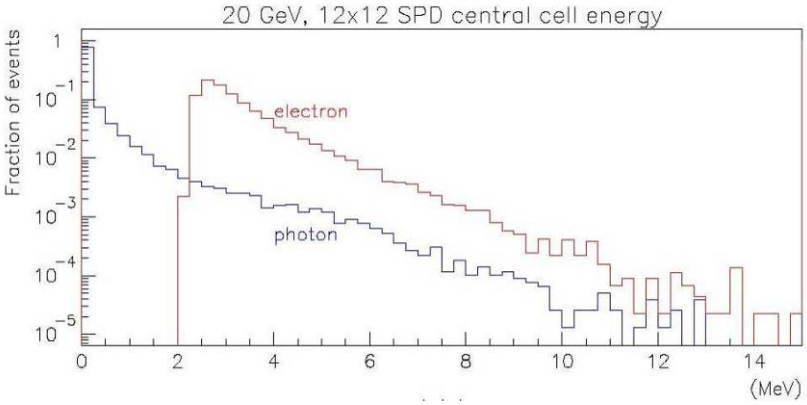

Figure 3-5. Deposited energy distribution at a central SPD cell.

When a photon is emitted in the scintillator it has a certain probability to be lost in a reflection or reabsorbed in the scintillator before it reaches the WLS fiber. Once it is captured by the fiber it is reemitted in a random solid angle. The Y11fiber consists of a scintillator core, and a double cladding. Depending on its emission angle the photon will have a certain incident angle in the cladding surfaces, and it may be lost if this is less than the limit angle. It could also be reabsorbed before it reaches the PMT. About 10000 photons are emitted per deposited MeV by a charged particle in the scintillator; but only around 100 of them arrive to the PMT, which has a 10 % quantum efficiency for the wavelength of the WLS light. So finally we expect about 10 photoelectrons (phe) per MeV.

3.2.2 Waveform shape

Low photo-statistics (about 25 phe per MIP) and the response of the WLS fiber, which has a decay time τ of around 12 ns, produce an irregularly shaped PMT outing signal as shown in Figure 3-6.

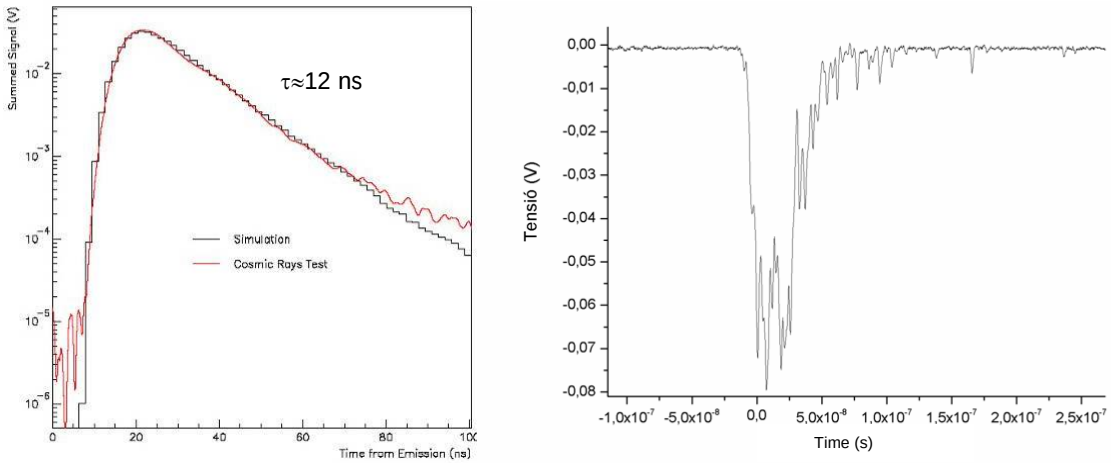

Figure 3-6. MIP signal shape: (left) average and (right) a typical single event.

The main factors contributing to the signal shape have been analyzed, simulated and compared with Cosmic Rays MIP signals [138]:

- Scintillator decay time. It has a 2.1 nanoseconds decay exponential.
- Time of propagation inside the scintillator. The time distribution is slightly different for the three sizes of tiles.
- WLS Fiber decay time. Exponential with about 10 nanoseconds time constant. This dominates the decay shape of the total time distribution.
- Time of propagation inside the fiber until it arrives to the PMT.
- PMT response. The FWHM of a photoelectron pulse for the R7600 is 1.8 ns.
- PMT load circuit: input impedance of readout system. Not considered for the moment.

The "slow" decay time means also that the signal spreads over more than the 25 nanoseconds which is the clock period of LHC machine. As seen in Figure 3-7 about the 80% of the signal is in the first period, with slight dependence on the pad size. This means that the read-out electronics must deal with a spill-over problem: the potential tail of a high amplitude event (> 2MIPs) could cross the threshold and provoke a fake trigger in the next clock period. Also, if a photon signal receives contributions of tails of a large electron signal, pile-up could provoke fake triggers.

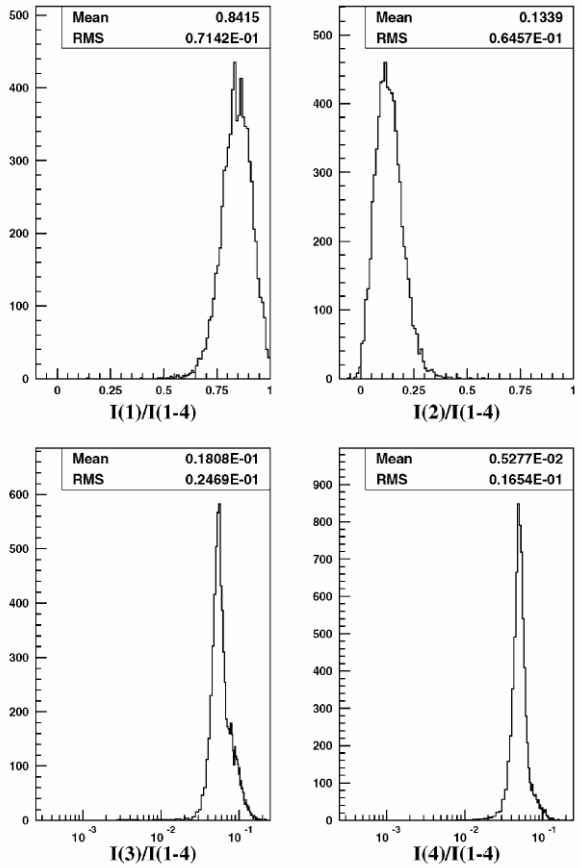

Figure 3-7. Normalized integral of the (cosmic ray) signal in four integration windows for a 4×4cm^2 pad: I(1) stands for the first 25 nanoseconds (where the collected charge is around 84.%), I(2) from 25 to 50 ns (13%), I(3) from 50 to 75 ns (1.8%) and finally, I(4) from 75 to 100 ns (0.5%).

3.2.3 Detector occupancy and its consequences

The occupancy is defined as the percentage of bunch crossings (not real interactions) where a particle hit (particle detection) is detected on a detector channel. The occupancy of the SPD cells depends on its position: occupancy is higher for the inner cells than for the outer ones. The average occupancy and the maximum occupancy of SPD at the nominal luminosity ($2\times10^{32}cm^{-2}s^{-1}$), and assuming about 0.37 events per bunch crossing, are 1% and 10% respectively, which is the highest maximum occupancy in the LHCb experiment [139] together with PS detector. For this reason it has been required that the front end electronics of the calorimeter detectors is capable to read out and process consecutive events. In many cases front end electronics for detectors with lower occupancy is designed introducing some "dead time" after a hit is produced, avoiding on that way the effects of pile-up (just rejecting any possible hit produced within the dead time) and having more flexibility in the shaping time constants (to optimize resolution, for example). This strategy can not be adopted in the SPD front end electronics: it has to process analog signals at the 40MHz bunch crossing rate.

Another consequence of the high luminosity of the LHCb experiment is the potential ageing problems of its detectors. In the case of SPD it affects the MaPMTs because the dynodes where electron multiplication is produced contain a Cs layer that is continuously depleted and then do not contribute to secondary electrons emission. As studied in [140] this effect implies not only gain degradation of 20 to 80 % (depending on the occupancy of the cell) but also an increase of the gain asymmetry within the channels of a PMT for 1 LHCb year if the PMT is operated at an average anodic current of 3μA. It has been tested [141] that gain and gain uniformity degradation is tolerable (below 5% per 1 LHCb year) if the PMT is operated at an average anodic current of 300 nA. Thus, MaPMT gain must be adjusted according to this limit.

To compute the PMT gain to avoid ageing it is necessary to estimate the average incident light for each channel, which at his turn depends on the mean energy deposit on each cell. The mean current $\overline{I}$ on each anode of the MaPMTs can be obtained through the following relation:

$$\overline{I} = \overline{F_e}\,\overline{E}\,\overline{Q} \qquad (3.1)$$

where:

- $\overline{F_e}$ (Event/second) is the average event frequency.
- $\overline{E}$ (MeV/Event) is the mean energy deposit at the corresponding scintillator cell (taking into account the occupancy of the cell) in scintillator tile per event.
- $\overline{Q}$ (Coulomb/MeV) is the average charge on the corresponding MaPMT anode per unit of energy deposit.

The bunch crossing rate at the LHCb interaction point is 40.08 MHz with 2622 out of 3564 bunches having real collisions (74 %). The fraction of interactions per bunch crossing at nominal luminosity is about 50%; therefore the average event frequency is 14.75 MHz. The mean energy deposit depends on the cell occupancy, for the cell with highest occupancy we obtain the maximal mean energy deposit, which is 0.44 MeV/Event. Imposing that the maximal average anodic current should be 300nA, a maximal charge for MeV is obtained: 46 fC/MeV. Since 1 MIP is 2.85 MeV, the maximal charge for MeV should be 132 fC/MIP.

As consequence of the ageing problem of the PMTs the gain of the PMT is limited according to the occupancy of its channel with higher gain. For the worst case, the gain of PMT should be tuned to have 132fC/MIP and the front en electronics should be capable to process the resulting signal.

Because of this relatively small charge (at least compared to other PMT based detectors such as ordinary calorimeters), it would be advantageous to mount the electronics on the PMT as shown in Figure 3-4 to minimize any ill effects such as pickup noise, loss or pulse distortion due to a long cable.

3.3 Requirements for signal analogue processing

In the SPD the collection time of the detector (25 ns for the 84% of the signal and 50 ns for the 97%) is higher than the maximum allowable measuring time: 25 ns (the LHC bunch crossing period) because no dead time is allowed. To maximize the resolution, and hence the charge collection, the measurement time T_m must be the maximum possible: 25 ns.

The low photo-statistics also cause an irregularly shaped signal, this is equivalent to say that the collection time of the detector has severe fluctuations, in addition to be comparable to the measurement time; therefore, the front end electronics must minimize the effects of the ballistic deficit.

3.3.1 Noise

The aim of the read out electronics is not only to distinguish between the pedestal and the MIP signal: it is important also to minimize the number of fake triggers due to the photon energy deposition. Therefore, the energy resolution in the threshold zone must be considered.

The cut between charged and neutral particles is around, 0.5 MIP. The inherent resolution related to photo-statistics for a scintillator counter is given by (2.6). An ENF of about 1.3 has been computed for single anode version of the same photomultiplier ([142], [143]). Although there are some variations, even between photomultipliers of the same model, we will assume ENF=1.2 (a real low value for a PMT), the most demanding value for the electronics. With H_0= 0.5 MIP and with N=25 phe/MIP is,

$$R \equiv \left.\frac{\sigma_{phe}}{H_0}\right|_{H_0=1MIP} = \sqrt{\frac{ENF}{0.5\, N_{phe/MIP}}} = 30\,\% \qquad (3.2)$$

A σ=0.15 MIP r.m.s is obtained for the best photo-statistics. The noise of the read out electronics ($\sigma_{Electronics}$) adds in square to the fluctuations of the signal related to the photostatischs ($\sigma_{Poisson}$,). It is required that $10\,\sigma^2_{Electronics} \le \sigma^2_{Poisson}$ to preserve the resolution given by photo-statistics. Then, $\sigma_{Electronics}$<0.05 MIP r.m.s.

As said above 1 MIP corresponds to 132fC in the worst case (PMT ageing limitation) If the gain non-uniformity is taken into account (up to factor 3 is accepted[n]) some channels of the PMTs of the hottest cells could have a MIP signal of 44fC/MIP.

Moreover, only the 80% of the signal is the first 25ns, the time available for the analogue processing; i.e. only 35 fC/MIP are available for the discrimination in the worst case.

Therefore, the required maximal noise of the electronics can be specified in terms of ENC $\sigma_{Electronics}$<2 fC MIP r.m.s or 12500 r.m.s electrons. Although PMTs, could provide very high gain (up to 10^7), the gain limitation due to ageing imposes to operate the PMT at gains of about $3\cdot10^4$ and, hence, quasi-low noise requirements for the read-out electronics.

3.3.2 Spill over correction

Correction of the spill over effect should be performed. As the output is binary, i.e. there is no amplitude or charge information after the discrimination, the spill over correction must be done before the signal is digitized (compared with threshold in the discriminator), that is to say in the analogue domain.

[n] Taking into account both MaPMT and detector non-uniformities.

Since the signal shape may change according to the scintillator size, to the distance from the WLS fiber to the PMT (the clear fiber length) or to the input impedance of the read out electronics (basically the load resistor at the PMT anode) the spill over correction must be programmable.

3.3.3 Reliescence against ballistic deficit

As said before, signal presents severe fluctuations. These fluctuations are seen by the signal processing electronics as a distribution in rise times at the output of a charge preamplifier. Rise time fluctuations manifest themselves as "ballistic deficit" when convolved with the transfer function of a pulse shaping network [8]. The extent to which the ballistic deficit influences the resolution and line shape obtainable from a spectroscopy system depends upon the tolerance of a given pulse shaping network to fluctuations in the input rise time and to the relative ratio fluctuation/peaking time. It is intuitive in fact, that the lower the rate of curvature at the peak of the step response of a pulse shaping network, the higher the immunity to the ballistic deficit [128].

It can be demonstrated that several pulse shaping networks are very tolerant to ballistic deficit [128]; therefore, in principle the problem can be minimized by using electronic techniques. However, the solutions applicable to reduce the ballistic deficit cannot be exploited in all of their potential, due to other conflicting needs. For example, often a practical solution for the mitigation of ballistic deficit is simply to choose a long(er) peaking time (where "long" is compared to the rise time at the output of the charge preamplifier and to its spread). It is also known that a long peaking time is usually associated with signals with an increased area and this implies degradation in electronic resolution due to parallel noise contributions [10].

A shaper with a step function response exhibiting a flat top for a time greater than the maximum detector signal rise time will result in zero deficit [113]. This is not possible in this application as the measurement time is limited to 25 ns, but again we found a reason to maximize it. The gated integrator shaper comes close to achieve this result and it was developed specifically to reduce ballistic deficit effects [110]. Therefore, gated integrator will be considered for the analogue processing.

The main drawback of flat top shaper is the increase of noise, proportional to the duration of the flat top as seen in 2.6.6. For charge sensitive amplifiers only parallel noise increases, but for voltage sensitive preamplifiers both series and parallel nois increase. It is very important to study the effect of the shapinf time on the noise and design the electronics considering this.

3.3.4 Dynamic range

Although the SPD is a binary output system there are several reasons to define its dynamic range:

- Good energy resolution is required around the threshold area.
- Must deal with gain non-uniformities (up to factor 3).
- A signal range of about 10 MIPs is required to perform the correction of the spill-over corresponding to the tails of large energy depositions. As shown in Figure 3-5 the probability of energy depositions larger than 10 MIPs is very small.
- Effect of the offset of the electronics.

Therefore, the analogue signal range must be 132 fC·80%·10 MIP ≈ 1pC. The internal analogue dynamic range is about 500 (9 bits) and the output should be a binary signal.

3.3.5 Baseline stability and offset

The high occupancy of the detector prevents the use of AC coupled elements in the signal path or DC feedback circuits due to the resulting severe baseline shifts.

Baseline restoration to compensate the shift is also really complicated because no dead time is allowed during bunch trains, thus, classic auto-zero or correlated sampling systems can not be applied, and the peaking time or measurement time is equal to the bunch crossing period, then no bipolar shaping is possible.

The read out should use, then, DC couple with the detector and between its blocks. Thus, a lot of care must be taken with the offset of the front end part of the electronics. Instead of designing a complicated offset cancellation circuit (as said before there is no dead time during bunch train), the solution adopted will relay on a careful design of the blocks to minimize their offset and on achieving dynamic range high enough to compensate it.

Another consequence of the offset, and of the MaPMT non-uniformities, is that each channel of the electronics must be able to set a different threshold.

3.3.6 Linearity

Since the MaPMT linearity error specification is 5%, the requirement for the electronics linearity error is <5%. Calibration could be applied to deal with linearity errors but the goal is to avoid it.

3.4 Global requirements to assure compatibility

The LHCb collaboration has defined a set of common requirements for the electronics sub-systems through the LHCb electronics coordinator. The purpose of the front-end electronics coordination activity is to define and specify a common architecture of the front-end electronics implementation in the different sub-detectors of LHCb such that they can work together as a homogenous system. The implementation of the front-end electronics of each sub-detector must conform to the defined architecture in such a way that the behavior of each front-end system can be predicted from the general architecture definition. The requirements for the L0 electronics, which includes the analogue front end electronics for detector readout, are defined in [144].

The L0 electronics is in general located very close to the detector, either inside the sub-detector itself or on its periphery. Electronics located inside a sub-detector can only be accessed for service or repair during the long shutdown periods of the LHC machine once per year (may in exceptional cases be accessed to perform specific repairs). Electronics located outside the detector can be accessed on a regular basis for simple repairs and service. The SPD analogue front end (included in the VFE unit) electronics is located in the upper and in the lower sides of scintillator wall, as shown in Figure 3-8. The SPD Control Board (CB) is located in the Frond end crates, on a platform over the ECAL.

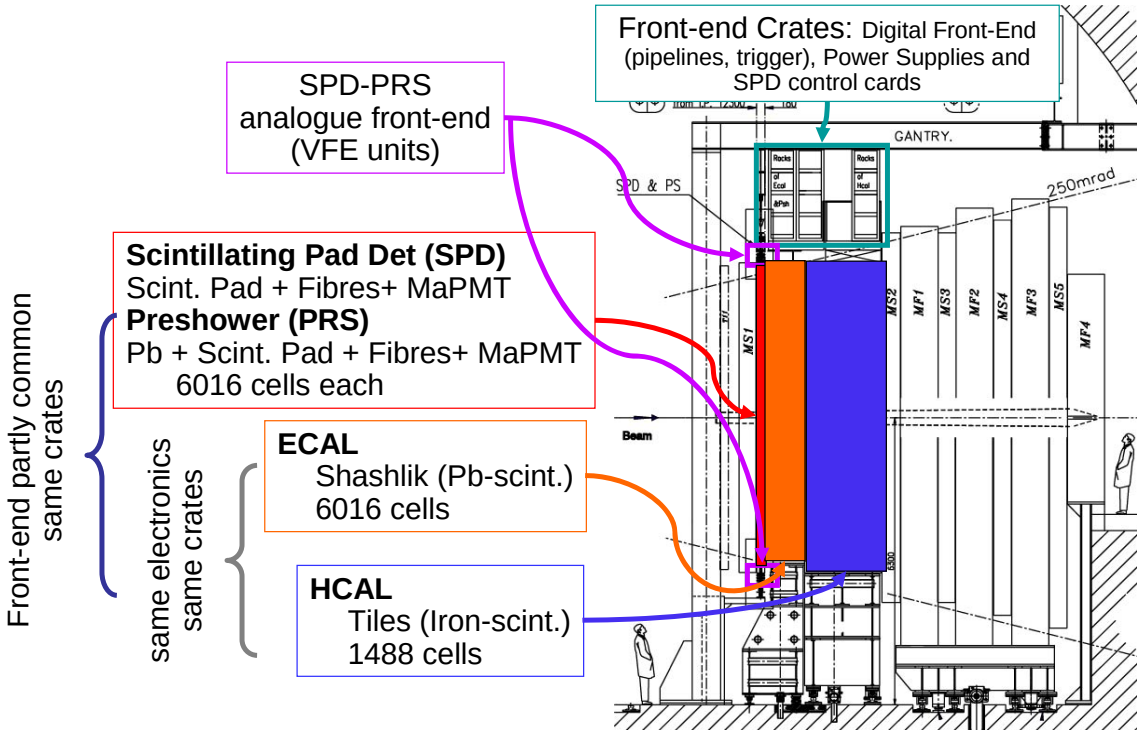

Figure 3-8. Location of the subsystems of the LHCb calorimetry

An overview of SPD sub-system and its main connections are shown in Figure 3-9. The front-end electronics of the LHCb calorimeter [148], except the VFE cards, will be placed in crates at the top of the calorimeters. 14 ECAL and 4 HCAL crates receive respectively 6016 and 1488 channels. 8 PS crates receive a total of 6016 channels from the PS's VFE and another 6016 channels from the SPD's VFE.

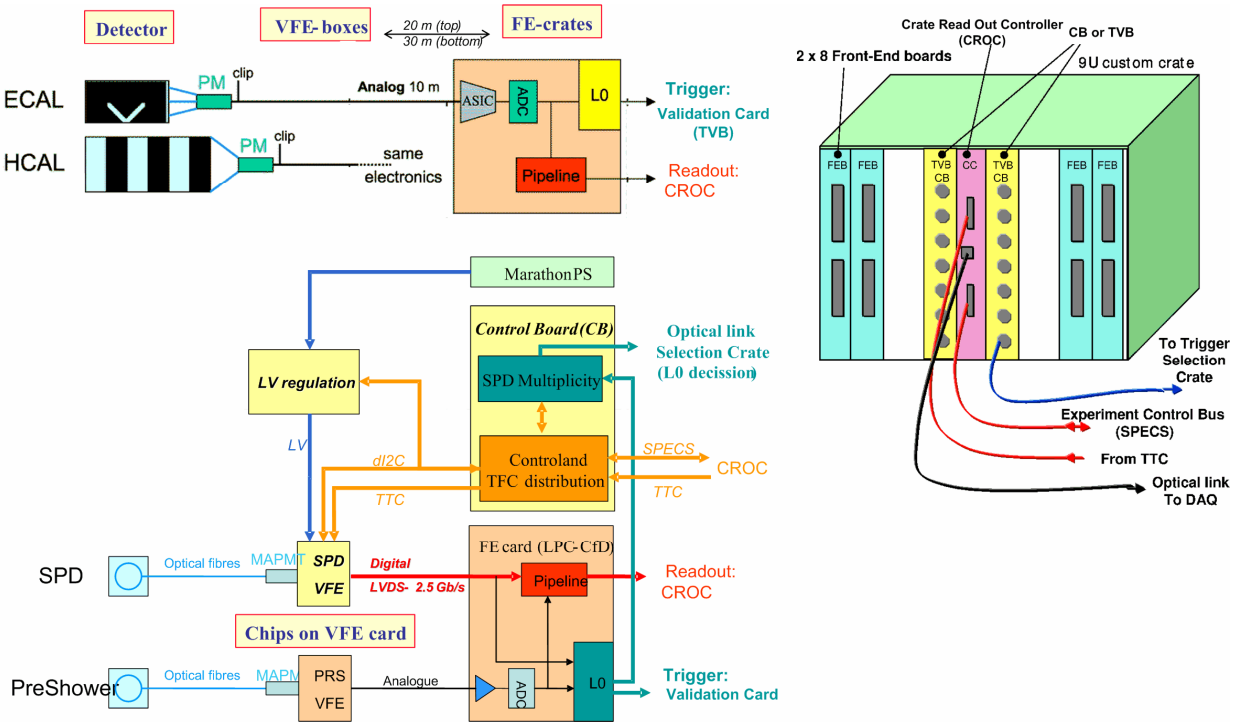

Figure 3-9. Block diagram of the SPD front-end elements.

The ECAL/HCAL PM signals are connected directly to the front-end boards (FEBs) through 10 meters of coaxial cables, whereas 20 m to 30 m differential pairs are used to send the output of the PS (analogue) and SPD cards (digital) VFE cards to a common PS/SPD FEB [149]. There are 16 FEBs in the crates, each receiving 32 signals for ECAL/HCAL crates and 64 signals from each detector for PS/SPD crates.

The FEBs have two different data paths: the trigger one and the readout one. The outputs of these boards are connected to the standardized custom backplane, sending signals using LVDS levels to the Calorimeter Readout Controller (CROC) for the readout data path and to the Validation boards for the trigger data path. The CROC also receives the Experiment Control System (ECS) [146] implemented under SPECS protocol [147] and the 40 MHz bunch crossing clock, trigger and synchronous commands from the LHCb Timing and Fast Control system (TFC) [144] and there from distributes them over the whole crate.

The CB is placed in the FE crates; there are two for each of the 8 crates corresponding to the PS/SPD subsystem. The purpose of the CB is twofold:

- To provide to the VFE cards a link to the ECS and TFC system. A phase alignment of the experiment clock [144] is also performed in the CB.
- Each PS/SPD FEB counts the number of SPD hits in the corresponding SPD VFE card. Up to 8 PS/SPD FEBs send this number to 1 CB through the backplane. The CB sums the 8 numbers and sends the result to Selection Crate in barracks to use this information in the trigger decision.

A water cooled magnetic field and radiation tolerant floating power supply system (MARATON) [150] feeds the crates and the VFE cards. The long distance between FE crates and VFE cards force to use local regulation close to the sensitive electronics. Regulator cards have monitoring capabilities and are also connected to ECS through the CB.

3.4.1 Radiation tolerance qualification of L0 front end electronics

The radiation hardness or tolerance qualification of electronics components is mandatory both for total dose and single events effects. Integrated circuits must be verified to be immune to single event latch-up.

For digital circuits, the effects of single event upsets on the reliability of the electronics must be evaluated and the detection and recovery from such failures must be considered.

A clear distinction must be made between accumulated effects and single event effects. Single event effects are of statistical nature and may therefore occur at any time and at any place (obviously proportional to flux of particles and sensitivity of components). For single event effects it is important to ensure that the time between failures is sufficiently long to guarantee an effective running of the whole experiment over extended periods. Single event upsets can be recovered by a simple re-initialization of the electronics. The re-initialization of the electronics can be done at several levels. State-machines or pipeline registers can normally be recovered by a "simple" reset. Single event upsets in configuration registers will require a reloading of parameters via the ECS. In both cases it will be necessary to restart active data taking with the DAQ system. It is important to ensure that this kind of soft failure do not occur so often that the system will spend a significant part of its time resolving random single event upsets. Single event upsets that prevents single detector channels to work correctly can in many cases be accepted during limited time periods, if and only if this do not significantly affect the physics and the triggers of the experiment. Bit flips in event data itself can normally be tolerated if they do not have any effect on the correct handling of following events. Single event latchup (and single event burnout) will in many cases be a fatal failure requiring repair, unless special latchup protection circuits have been used. Single event Latchup must therefore be proven to happen sufficiently seldom that the whole LHCb experiment can work for several weeks without repair. Even hard failures can in some cases be accepted during extended periods if it can be guaranteed that the failure do not seriously affect the physics performance of the experiment. In many

cases a few local "dead" detector channels will not have a significant effect on the physics of the experiment. It must though be ensured that local failures are prevented from disturbing higher levels of the system and thereby affect data collected from other parts of the detector.

Cumulative effects risk to make large parts of an electronic system unusable after a given radiation threshold has been reached. Such a situation may occur after several years of operation at a time when the components used have become obsolete and can not be purchased commercially. For systems with large variations in radiation levels for different parts of the system (e.g., small part of front-end electronics very close to beam line) it can be envisaged to exchange limited parts of the electronics system after a certain number of years. For systems with a more uniform radiation exposure it is unrealistic to start exchanging components when they start to fail one by one. In this case it must be proven that the system can stand the radiation levels over many years of operation (10 years). This is the case of the SPD front end electronics.

The radiation level estimations for LHCb are generated from Monte Carlo simulations with FLUKA [145]. The simulations of the radiation levels at the location of the SPD front end electronics are summarized in Table 3-1.

Total dose [Krad] per 10 years	
Mean	3.5
Max	5.8
Fluence [particles/cm^2] in 1 MeV Neutron equivalent units per 10 years	
Mean	$8.2 \cdot 10^{11}$
Max	$9.3 \cdot 10^{11}$
Fluence [particles/cm^2] of hadrons >20 MeV per 10 years	
Mean	$4.1 \cdot 10^{10}$
Max	$4.8 \cdot 10^{10}$

Table 3-1. Radiation levels at the location of the SPD front end electronics

Uncertainties related to the Monte Carlo simulations and their assumptions on interaction models are normally estimated to be of an order of a factor two. The radiation hardness qualification of components will also have uncertainties associated with them (e.g. dosimeter uncertainties). The components themselves may have significant uncertainties depending on the origin of the components. ASICs from a well defined processing batch will only have a relatively small uncertainty on their measured radiation hardness. Therefore, some safety factors should be added to the total doses expected when a component is qualified: factor 2 for simulation uncertainty, factor 2 for radiation qualification uncertainty and factor 2 for component to component variation. The safety factor for the simulation uncertainty is already taken into account in Table 3-1, thus a total safety factor of 4 must be applied.

3.4.2 Synchronization

The synchronization of the experiment is based on a set of synchronization signals from the LHC machine. The bunch-crossing rate is given by the LHC bunch-crossing clock, delivered with a constant phase to the real bunch crossings. The longitudinal dimension of the LHC bunches is expected to give a 175ps RMS (4σ = ~700ps) time variation (jitter) in the real interactions in relation to this reference. The synchronization to the LHC machine cycle is obtained from a LHC machine cycle synchronization signal. The LHC synchronization signals are received by the readout supervisor, which generates the required synchronization signals to the TFC system [144] (based on optical links). The readout supervisor will be capable of delaying the machine cycle synchronization of up to one complete LHC machine cycle period.

The sampling of the analog detector signals at the measurement time T_m must be phase aligned to the bunch crossings with a precision and stability of a few nanoseconds (high-resolution detectors may need even better phase alignment). The bunch-crossing clock, delivered to the front-end by the TTC system, has a constant but unknown phase to the LHC machine clock (drivers, cable delays, receivers), and therefore, to T_m.

In some cases the clock phase alignment must be performed on a channel by channel basis. In most cases the clock phase alignment can be performed on groups of channels, when delay differences (skew) between channels in a group are kept under tight control (same time of flight, small detector differences, common high voltage supply, matched cable lengths, front-end chips from same production batch, small temperature gradients, etc.)

The clock phase alignment to the beam crossings will typically consist of a clock phase sweep, until sampling at the maximum signal amplitude has been obtained (peak find). Because of the relative low occupancy of detector channels in many detectors, a large set of triggers must be generated to collect sufficient information to insure a correct clock phase alignment of all channels. If a group of channels by construction has equivalent timing characteristics they can be time calibrated as one thereby decreasing the required number of triggers significantly. For detectors with significant drift time and/or sampling of discriminated detector signals, more elaborate schemes using track reconstruction between detector stations may be needed.

The phase synchronization of the SPD analogue front end (of the VFE unit) is done trough the SPD Control Board (CB) that sends the LHC clock to the analogue front end (see Figure 3-4). On that card a delay unit will delay properly the LHC clock (up to 1 complete period in steps of 1 ns), a delay sweep will be performed until maximum signal amplitude has been obtained (peak find). It is obvious that SPD channels are grouped according the division in VFE units, where 64 tiles of the same length are read out using a single MaPMT.

3.4.3 Error Checking and Communication protocols

During data taking with the complete LHCb experiment large amounts of data must be collected from many sources (~1 million) at high speed (40 MHz). Correct processing of all data in the trigger systems and in the DAQ system relies on the correct synchronization and correct function of a large number of front-end chips (~50 K), modules (~1500), links (thousands) and processors (thousands). Malfunctions (hard and soft) of components in such a large system must be expected during data taking, making it vital to include extensive error checking/recovery functions in the system.

Several levels of error checking/recovery functions must be built into the front-end electronics system:

- Generation of special error checking events.
- Running self-tests at regular intervals.
- Re-initialize system at regular intervals.
- Continuous self check of front-end parameters.
- Error detecting/correcting codes on critical event data (e.g. parity/hamming/CRC/etc.).
- Self checking state machines and logic. (e.g. one hot encoded with continuous state verification)
- Single event upset immune architectures (e.g. 3 to 1 majority logic)
- Watch dog timers.

As shown in Figure 3-4 a Control unit (implemented through an EEPROM Actel FPGA of the ProAsicPlus family) will perform most of these functions and the digital parameters of the ASIC will be programmed and monitorized through a serial interface. Therefore, any configuration register

inside the ASIC will be protected with triple voting and will readable to perform error checking, as required in [144].

The control, monitoring, and verification of the front-end electronics are performed by the ECS. The global ECS system will communicate with the front-end electronics via the ECS interfaces. The ECS interface to the front-end electronics has been standardized, to insure a consistent and well functioning control and monitoring system. For front-end electronics located in the cavern special solutions, with built-in immunity to radiation induced single events, are needed. For the cavern itself, with limited radiation levels, an ECS interface called SPECS (Serial Protocol for Experiment Control System) has been chosen as an appropriate solution. SPECS is based on a serial protocol running on standard cat5 cables with a maximum distance of 100 meters. A SPECS slave interface, with built-in immunity to single event upsets, is available as a standard component within LHCb. An alternative solution based on a special SEU immune CAN slave, called the ELMB, is also used in some other parts of the experiment.

For front-end electronics, located inside the detector in a high radiation level environment, special solutions are needed. Limited distance (~10m) simple serial protocols like I2C and JTAG are used to reach SPECS and CAN slave modules in the cavern. Seven SPD VFE units (Figure 3-4) are controlled and monitorized by one SPD Control Board (see Figure 3-4) using the I2C interface. The SPD control card is located in the Front End Crates (see Figure 3-8) and it will provide the interface to the SPECS bus.

3.4.4 Cooling and power consumption

PS and SPD VFE units are located in metallic boxes (see Figure 3-10) on the top and the bottom of the scintillator layer. Each box could contain between 3 to 11VFE units and they are closed for proper optical and electrical shielding. Therefore, cooling is a complicated issue.

Fans can not be used due to the high magnetic field created by the magnet. Cooling is performed using a radiator thermally connected to a water circuit as shown in Figure 3-10.

The power dissipation of a VFE box is limited to 100W, therefore the power dissipation of a VFE unit should be smaller than 9 W, taking 3 W for control and interface electronics it remains 6 W for the signal processing. Therefore the power consumption must be less than 100 mW per signal processing channel.

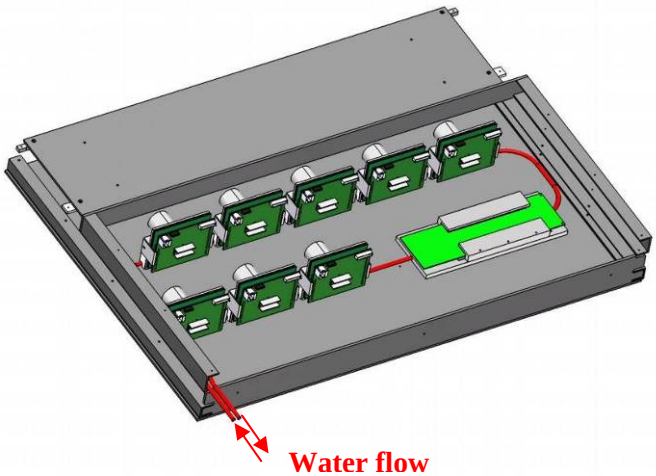

Figure 3-10. Boxes containing VFE units.

3.5 Proposal of an integrated Mixed-Mode solution

In order to minimize the ballistic deficit a flat top pulse shaper is preferred, being the gated integrator the simplest solution for a VLSI implementation. To achieve a 25 nanoseconds measurement time means that the integrator has to operate without any dead time, there are two possible solutions to achieve this:

1. Use delay line clipping to subtract a delayed and inverted input signal. This solution is used in the front electronics of the LHCb ECAL/HCAL [148].
2. Use two identical processing channels (called sub-channels) working in parallel. The reset switches of the gated integrators manage an interleaved operation: while one sub-channel is integrating the detector signal the other one is being reset.

The drawback of the first solution is the amount of space needed for a 25 nanoseconds delay line of good quality. The use of switches might be a problem due to the inevitable injection of charge. This injection of charge generates pedestal and pedestal drifts. A pedestal is not a problem, just a systematic offset that will be combined with the offset due to other parts of the circuit. Since pedestal drifts below the level of the required resolution are achievable and room constraints are quite severe the second solution is taken.

Figure 3-11 shows the proposed functional architecture of signal processing. The configuration is based on two interleaved processing units per channel to avoid dead time and to be able to perform the pile-up compensation. This solution does not require external components such as delay lines.

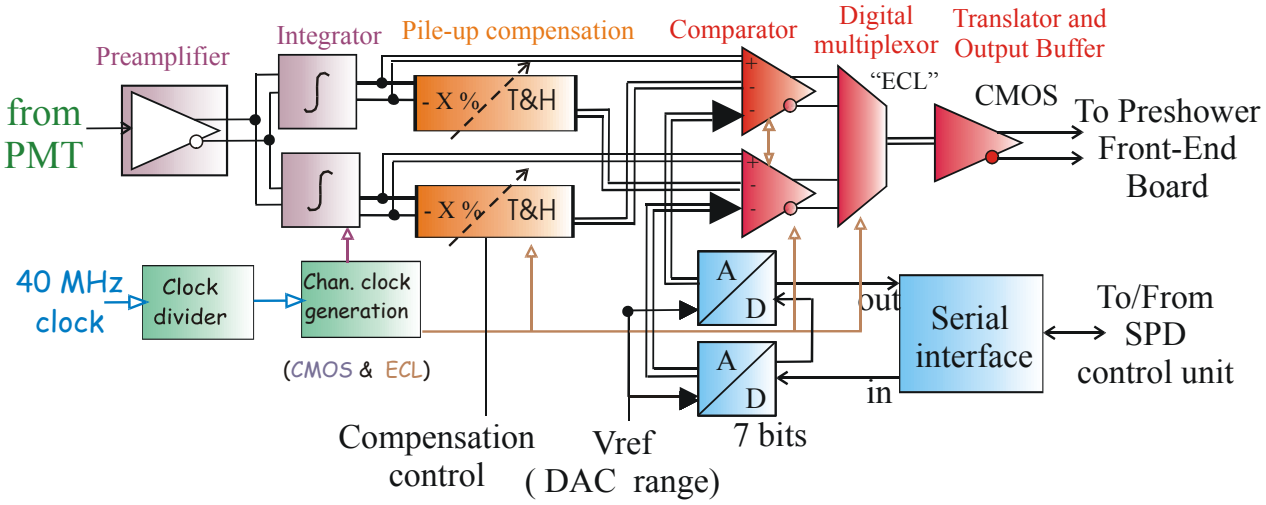

Figure 3-11. Functional diagram of a discriminator channel.

The bunch-crossing clock is divided and then used to multiplex by level the two paths of the channel each 25 ns. To prevent digital crosstalk on sensitive analogue parts, the system and each block are fully differential. This kind of solution is also adopted for the PS chip [151]. Main drawback of using fully differential circuitry is doubling the area and the power consumption.

Figure 3-12 shows the typical operation of the discriminator. The PMT signal is single ended; it is preamplified and converted to differential by the first block of the discriminator. As explained in the previous section the signal shape is rather unpredictable and spreads over more than one clock period of 25 ns. Thus, to optimize the measurement of the energy deposition the input signal is integrated for the whole period. While one integrator is reset the other performs the integration and its output is continuously corrected and compared with a programmed threshold. The comparison is latched just before the end of the integration period. The pile-up compensation system takes a fraction of the integrator output at this time (ideally the fraction that would appear in the next period) and stores it on a track and hold circuit. The fraction to subtract is tunable through an analogue control signal in order

to correct differences in the time response coming from differences in cell sizes, fiber lengths or radiation doses.

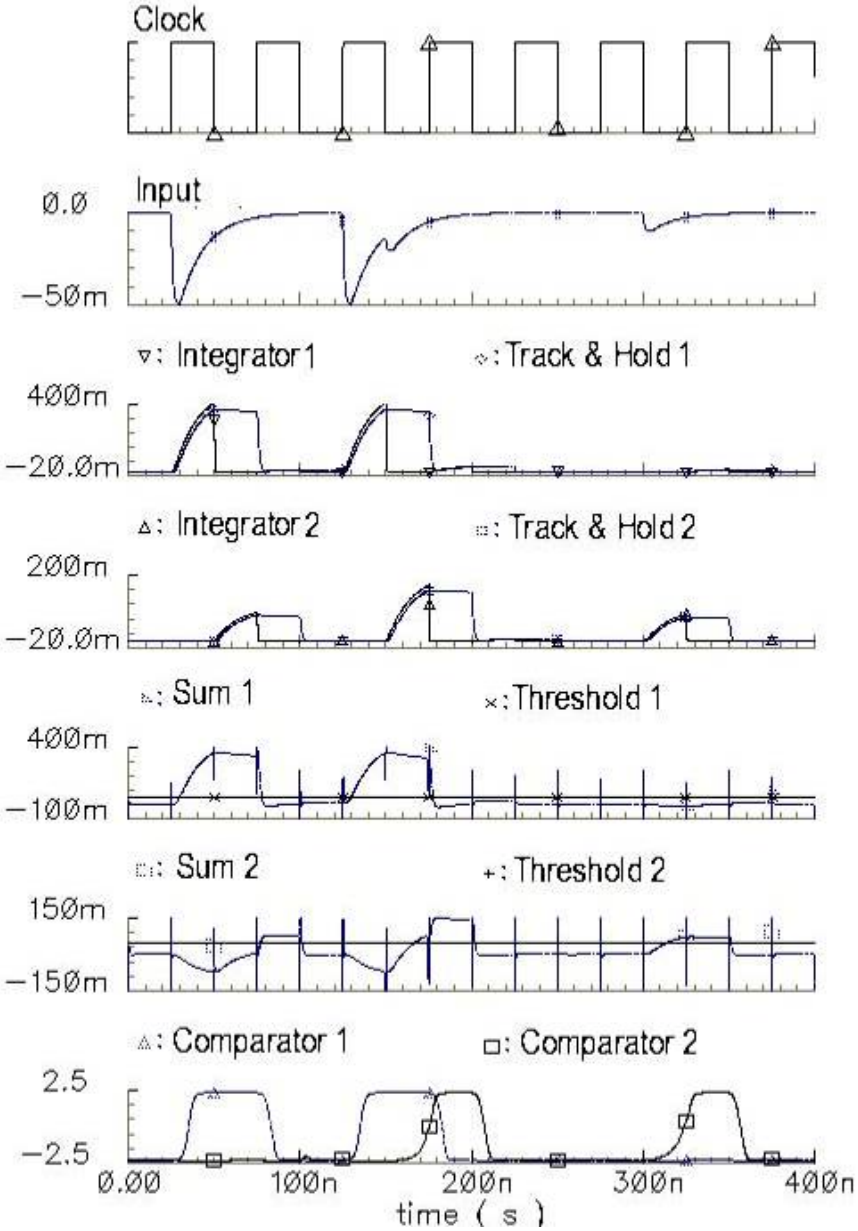

Figure 3-12. Simulation of the operation of the two sub-channels.

The comparison stage continuously subtracts from the integrator output the value stored in pile-up compensation block of the other path (that corresponds to the previous sample). The threshold value is set by 7 bits DAC. A latched comparator, whose output would be validated and latched just before the end of the integration period, evaluates the sign of this subtraction. The output of the comparator is an ECL type signal, to reduce pick-up noise. A multiplexer selects the comparator that it is in the latch state. An ECL to CMOS translator is needed to be able to drive the LVDS serialiser.

Each path uses an independent DAC to be able to compensate the offsets due to process variations between different subchannels. It is a multiplying converter that uses a common differential external reference that can be changed for calibration and test purposes. The DACs are programmed through a serial interface to reduce the pin count. The memory elements of the digital part use redundancy mechanisms to prevent the effect of single event upsets.

3.5.1 Design strategies

Although PMT input signal is single ended by definition the design of the circuit will follow fully differential and fully balanced approach in order to minimize the effect of pickup noise, which will be rejected as long as it is coupled as a common mode signal.Taking profit from the differential architecture, the power consumption of the analogue part is made static to minimize the conducted noise.

Different internal clocks are needed to control the integrator, the track and hold, the comparator and the multiplexer. Special care is needed on its generation because the offset and the noise of the system are very sensitive to differences between the phases of the clock and to the clock jitter. These clocks are made differential to minimize its effect as interference sources.

The digital channel output is balanced using a dummy inverted output to try to cancel the digital pick-up noise and balance the digital supply current.

Although maximum supply voltage in the chosen technology is 5.5 V, the supply voltage is reduced down to 3.3 V in order to fulfil the requirement of 100mW of power consumption per channel.

Since temperature variations could be non negligible inside the VFE boxes band gap references are used to provide a stable bias current. The temperature coefficient (TC) of the analogue circuitry must be considered at design level, and should be smaller than the 1%/K.

3.5.2 Technology choice

The Austriamicrosystems 0.8μm BiCMOS technology is chosen because bipolar transistors are well suited for the analogue parts, especially to reduce offsets, and because MOS transistors are used as switch elements and to reduce the power consumption in the digital parts.

On the one hand bipolar transistors are used as signal transistors in the analogue circuits. For the same bias current they do provide higher transconductance than the MOS transistors (in the same technology). With a f_T of 12 GHz they have lower input-referred noise for short measurement times. A smaller input referred offset voltage is also obtained with bipolar transistors; see section 6-5-13 in [67]. This is a critical parameter to maintain the dynamic range of the circuit as it will be shown in next chapter.

On the other hand MOS transistors are adequate for digital circuits, for analogue switches and they do provide a lot possibilities in designing electronic tunable transconductance circuits.

The analogue front end electronics of other elements of the LHCb calorimeter has been also implemented using this technology (see [148] and [151]).

The circuit has been designed and simulated with Spectre simulator of Cadence version 4.4.3.100.35 and the Austriamicrosystems Hit-Kit.

3.5.3 IC floorplan, power and packaging

After considering several possibilities, eight signal processing channels are integrated in each chip because:

- The number of channel per chip must be an integer divisor of the number of channels per VFE card (64).
- Higher number of channels (16, 32 or 64) is discarded because it implies a power consumption of more than 1 W chip which is too much for thermal resistance of a conventional package.
- Lower number of channels (4, 2 or 1) will lead to an inefficient occupation of the board.

- With eight channels per chip a die with an aspect ratio close to one can be achieved (5.254 mm x 5.500 mm) and 64 pads are enough. This fits very well with Quad Flat Pack (QFP) packages, that allows minimize the size of the chip and the bonding length (source of parasitic resistances and inductances).

The EDQUAD MQFP package from ASAT is chosen because it provides enhanced power dissipation. A reduction of factor 2-3 in thermal resistance compared to conventional QFP packages [152] thanks to a copper heatsink connected to the die substrate as shown in Figure 3-13. This package is available in 64 pin with 0.5 mm pitch, resulting in a total size of 12 mm x 12 mm, including leads.

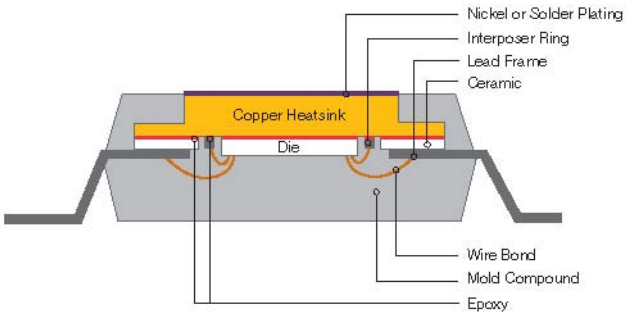

Figure 3-13. Die down configuration of the EDQUAD MQFP package.

4 Circuit design

4.1 Design history

The design of the chip started the year 2000 and the final prototype was submitted in 2003. In 2004 almost 2000 chips were produced. A total of 5 design iterations have been performed, Table 4-1 summarizes these prototypes. This work describes the final version of the chip, unless the contrary is specified.

Date	Prototype	Novel chip features
March 2000	1 chip with 3 different channels and several version of its building blocs (OTA, Integrator, Comparator, Subtractor)	• Supply voltage: 5V • Tail correction: fixed • Digital interface and DAC not included • JLCC 68 pin package
February 2001	2 chips: one with improved building blocs and other one with four complete channels	• Building blocs are selected and refined • One channel with embedded test probes.
September 2001	1 chip with 1 complete channel, digital interface, DAC and different track and hold circuits with tunable gain.	• Tail correction: adjustable • Digital interface and DAC included.
June 2002	2 chips: one with redesigned building blocks (supply voltage and current minimized) and other with one full channel with embedded probes	• Supply voltage decreased to 3.3V and channel bias current decreased down to 25 mA. • New voltage preamplifier. • Channel with embedded test probes.
August 2003	Final prototype with 8 channels (3.3 V, adjustable correction, digital interface)	• Improved SNR • JLCC 68 pin and EDQUAD QFP 64 pin

Table 4-1. Chip design iterations.

4.2 Analogue circuitry for amplification, shaping and discrimination (ASD)

As presented in section 3.2.2 the PMT current pulse response to a MIP particle ionization in the Scintillator can be approximated by[o] a pulse of exponential decay time constant τ of about 12 ns:

$$i_{PMT}(t) = -\frac{Q_{MIP}}{\tau} e^{-\frac{t}{\tau}} u(t) \qquad (4.1)$$

[o] Average shape, neglecting statiscal variations of incident light (photoelectrons) or variations in the PMT gain electron multiplication.

The pulse is negative, Q_{MIP} is the total charge corresponding to a MIP particle and u(t) is the step response function. A load resistance (R_{PMT}) at each MaPMT anode transforms the signal into a voltage signal that will be processed by the ASIC. The waveform shape of the voltage pulse is also influenced by the board stray capacitance (C_{stray}) and the input capacitance (C_{in}) of the ASIC. The input resistance of the ASIC is much higher than R_{PMT}, and thus can be neglected.

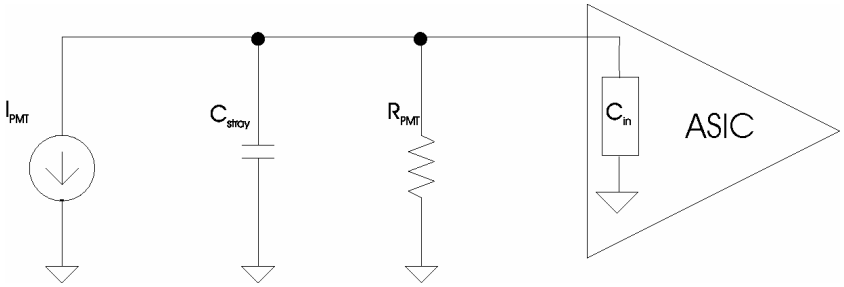

Figure 4-1. Circuit at the PMT anode.

Then taking $C_{par}= C_{stray}+ C_{in}$, we can write the differential equation for the voltage $v_i(t)$ at the ASIC input,

$$\frac{v_i(t)}{R_{PMT}} + C_{par}\frac{\partial v_i(t)}{\partial t} = i_{PMT}(t) = -\frac{Q_{MIP}}{\tau}e^{-\frac{t}{\tau}}u(t) \qquad (4.2)$$

If the capacitances are discharged at t=0, which is the usual situation when the PMT works in pulse mode, the solution of the ordinary first order differential equation (4.2) is

$$v_i(t) = \frac{Q_{MIP}}{\tau C_{par}}\left(e^{-\frac{t}{\tau_C}} - e^{-\frac{t}{\tau}}\right)\frac{1}{\frac{1}{\tau_C}-\frac{1}{\tau}}u(t) \qquad (4.3)$$

The time constant τ_C is the time constant of the load circuit $\tau_C= C_{par}\cdot R_{PMT}$. Depending on the relative values of the two time constants we can distinguish between two operation modes:

a) Voltage mode for $\tau_C>>\tau$. The amplitude of the voltage pulse is Q/ C_{par}, the PMT pulse current is integrated in the parasitic capacitance.

b) Current mode for $\tau_C<<\tau$. The voltage signal follows the current pulse shape.

In our case we need to operate the PMT in current mode for several reasons. First, the gain of the system must be known and its tolerance must be low. Second, the voltage pulse must be as fast as possible to avoid any pile-up. Then for current mode operation,

$$v_i(t) \simeq \Big|_{\tau_C \ll \tau} -\frac{Q_{MIP}}{\tau}R_{PMT}e^{-\frac{t}{\tau}}u(t) \qquad (4.4)$$

From (4.4) it is clear that increasing the load resistance of the PMT maximizes the signal at the input stage, which in general is good in terms of SNR as we will see later. However increasing R_{PMT} also increases τ_C, and to operate the PMT in current mode we need $\tau_C<<\tau$. Furthermore, since the measurement time of the system is fixed by the clock of the experiment to 25 ns, increasing too much R_{PMT} and then τ_C and the global decay time constant of $v_i(t)$ implies loosing signal. Figure 4-2 shows that to have at least the 80 % of the signal in a 25 nanoseconds period, the input time constant τ_C must be smaller than 5 ns. Having a typical parasitic capacitance of about 10 pF, the approximated limit for R_{PMT} is 500 Ω.

The preamplifier and integrator gain will be adjusted so that the combined gain is 1mV/fC with a resistor of 470 Ω. In this way a MIP signal varies at the comparator input from 100 mV to 25 mV, depending on variations of the gain between MaPMT and detector channels. To have a minimum SNR of 10, the noise at the comparator input must be smaller than 2 mV r.m.s. Finally, signal range of the analogue processing between integrator's output and comparator's input must be 1 V, indeed

the range will be ±1 V as all the blocks are differential, to have at least a range of 10 MIP, in order to avoid saturation of the tail cancellation system for high energy events.

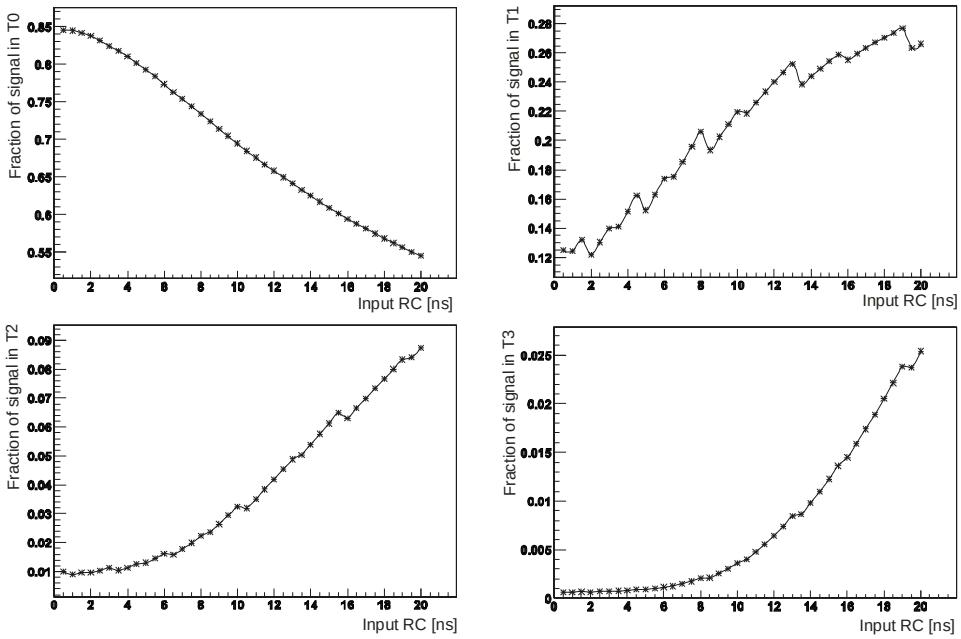

Figure 4-2. Fraction of signal in 4 consecutive clock cycles as a function of input time constant τ_C.

4.2.1 Preamplifier

The front-end preamplifier (see Figure 4-3) consists on a bipolar pair with emitter degeneration. The gain is adjusted by the ratio between collector resistors and emitter resistors, and it is about a factor 4.6. The linearity is good enough for the level of input signals that must be processed. So no compensation is needed. An emitter follower provides low impedance output, needed to decouple the effects of the switch on the integrators.

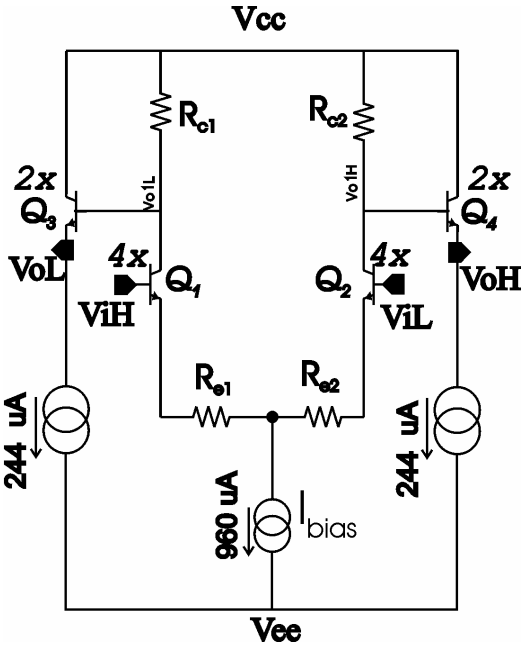

Figure 4-3. Preamplifier schematics

The bandwidth of the block is about 200MHz for load capacitances smaller than 1pF according to Spectre simulations. The temperature coefficient (TC) of the block is quite small (TC<0.1%/C) thanks to the cancellation of the TC of the emitter and collector resistors (both are same type of polysilicon resistors). This kind of open loop stage is widely used in other components because it allows to achieve high bandwidth, high input impedance, low TC and also to avoid stability issues, using a simple circuit of small layout area.

A detailed analysis of this stage will be done for two reasons:

1. Any noise or interference on the first stages (preamplifier and integrator) is magnified by the gain of the system. This is not the case for other blocks because the system gain is concentrated on firsts stages to optimize the noise.
2. This kind of open loop stage is widely used also in other blocks of the ASIC because it allows to have high bandwidth, high input impedance, low TC, small area and to avoid stability issues. Therefore, the extrapolation of conclusions for the preamplifier to other stages is straightforward.

The implementation of the tail current sources is described in section 4.5.1. The total current consumption of this stage is 1.5 mA.

4.2.1.1 Large signal DC transfer characteristic

The large signal behavior of a circuit is important because it illustrates the limited range of input voltages and the conditions over which the circuits behaves almost linearly.

In differential circuits differential variables (sub index *D*) and common-mode variables (sub index *C*) are usually defined [66] at the input and at the output as follows. The differential input, to which differential pairs are sensitive, is

$$V_{iD} = V_{iH} - V_{iL} \tag{4.5}$$

The common-mode or average input is

$$V_{iC} = \frac{V_{iH} + V_{iL}}{2} \tag{4.6}$$

Differential V_{oD} and common-mode V_{oC} outputs are defined in the same way.

From KVL (Kirchoff´s Voltage Law) around the input loop,

$$V_{iH} - V_{BE_1} - I_{C_1} R_{E_1} + V_{BE_2} + I_{C_2} R_{E_2} - V_{iL} = 0 \tag{4.7}$$

with $V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right)$, $V_{BE_1} - V_{BE_2} = V_T \ln\left(\frac{I_{C_1}}{I_{C_2}}\right)$, $I_{oD}=I_{C1}-I_{C2}$, $I_{oD}=(I_{C1}+I_{C2})/2$. Assuming $R_{E1}=R_{E2}=R_E$ the expression (4.7) can be rewritten in the form,

$$V_{iD} = V_T \ln\left(\frac{1+\frac{I_{oD}/2}{I_{oC}}}{1-\frac{I_{oD}/2}{I_{oC}}}\right) + I_{oD} R_E \tag{4.8}$$

Which, using the expansion in Taylor series $\ln\left(\frac{1+x}{1-x}\right) = 2\left[x + \frac{x^3}{3!} + \ldots\right]$, can be expressed as

$$V_{iD} = I_{oD}R_E + 2V_T\frac{I_{oD}/2}{I_{oC}} + 2V_T\frac{\left(\frac{I_{oD}/2}{I_{oC}}\right)^3}{3!} + \ldots \qquad (4.9)$$

Note that even-order terms are not present in the differential output; this is a well-known advantage of fully differential circuits.

Omitting 3rd and superior odd-order terms and using the typical expression for the transconductance g_m of the bipolar transistor $g_m=I_{oC}/V_T$, the differential output voltage follows an approximate linear relationship (4.10) with the input differential voltage

$$V_{oD} = R_C I_{oD} \simeq R_C \frac{g_m}{(1+g_m R_E)} V_{iD} \qquad (4.10)$$

The linearity error is given by the 3rd and superior order terms of the Taylor series, taking the approximated value for $I_{oD} \simeq \frac{g_m}{(1+g_m R_E)} V_{iD}$ the non-linear terms of (4.9) are negligible if $x = \frac{\frac{1}{2}\frac{g_m}{(1+g_m R_E)} V_{iD}}{I_{oC}} \ll 1$, thus the linear operation range for V_{iD} is

$$V_{iD} \ll \frac{1}{2}\frac{(1+g_m R_E)}{g_m} I_{oC} \qquad (4.11)$$

The common mode output current I_{oC} is $I_{bias}/2$, therefore $V_{iD} << 128$ mV. As pointed out in section 3.3.4 the input signal range is from 2fC to 1pC. The peak current I_{pk} of a pulse with a decay time τ of about 12 nanoseconds and charge Q is approximately Q/τ, thus the signal range in current is from 166 nA to 83 µA. For the maximum input signal $V_{iDmax}=I_{pkmax}\cdot R_S=38$ mV, the 3rd order term in (4.9) is about the 0.1% of the first order term.

Figure 4-4 shows results of the simulation for input (V_{iD} at left) and output (V_{oD} at right) voltages for different PMT peak currents.

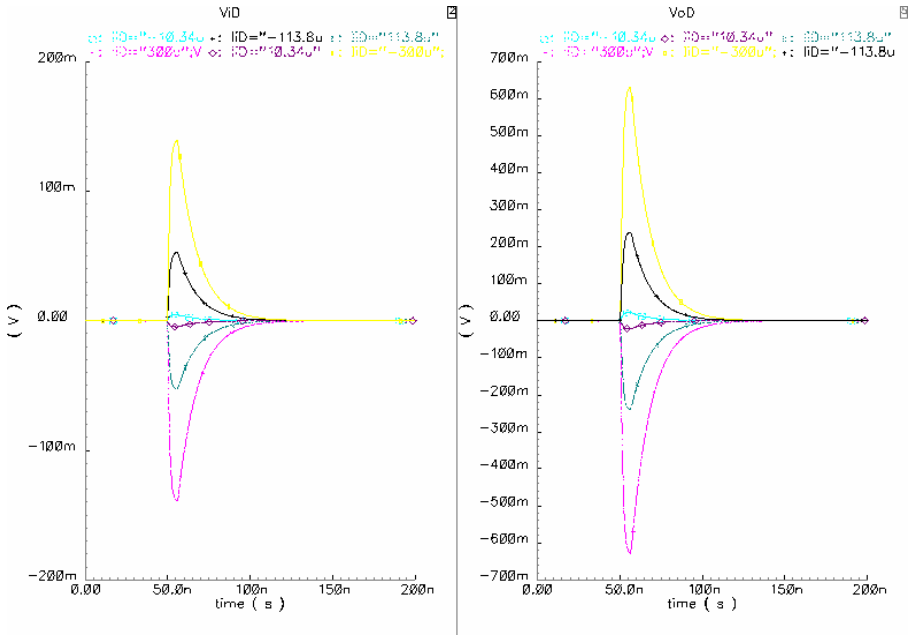

Figure 4-4. Transient simulation of preamplifier response: input (V_{iD} at left) and output (V_{oD} at right) voltages for different PMT peak currents.

In order to analyze preamplifier non-linearity V_{iDpeak}, V_{oDpeak} and the linearity error (*Error*) calculated as the deviation from a perfect linear response of the form $4.6 \cdot V_{iD}$, are simulated. Results are shown in Figure 4-5, maximum linearity error in the PMT signal range of ±100 µA is 100 µV for a V_{oDpeak} of 200 mV, i.e. the maximum linearity error is about 0.05 % of signal range.

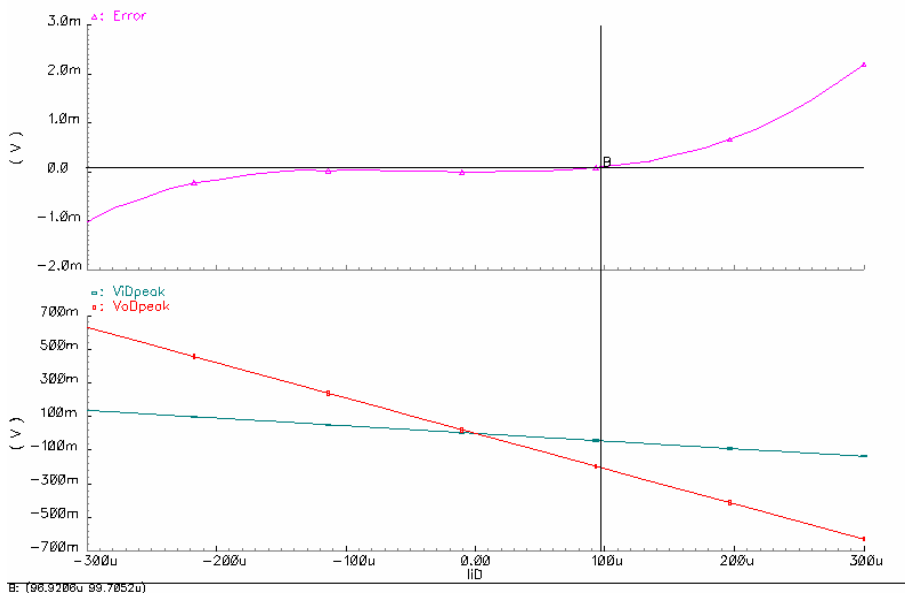

Figure 4-5. V_{iDpeak}, V_{oDpeak} and linearity error (*Error*) as a function of PMT peak current.

4.2.1.2 Frequency response

The frequency response to the input differential voltage V_{iD} will be analyzed. First, it will be considered the input differential pair (Q_1-Q_2) with emitter degeneration and later the effect of the output (emitter follower) stage. For small-signal differential inputs (v_{iD}) the node where the two emitter resistors R_E are connected to the current source is a virtual ground (see proof in section 4.2 of [161]) and we can use the concept of differential-mode "half circuit" ([66] or [161]).

Figure 4-6 shows the small-signal equivalent half circuit of the differential input stage of the preamplifier. The C_{par} term accounts for parasitic (interconnection and package) capacitances. R_s is the PMT load resistor (and also to provide base bias current). C_L is the load capacitance of the input stage and that basically corresponds to the input capacitance of an emitter follower (Q_3-Q_4) which is C_{π}[p]. The simplified AC small-signal hybrid-π model has been adopted for the bipolar transistor ([66]).

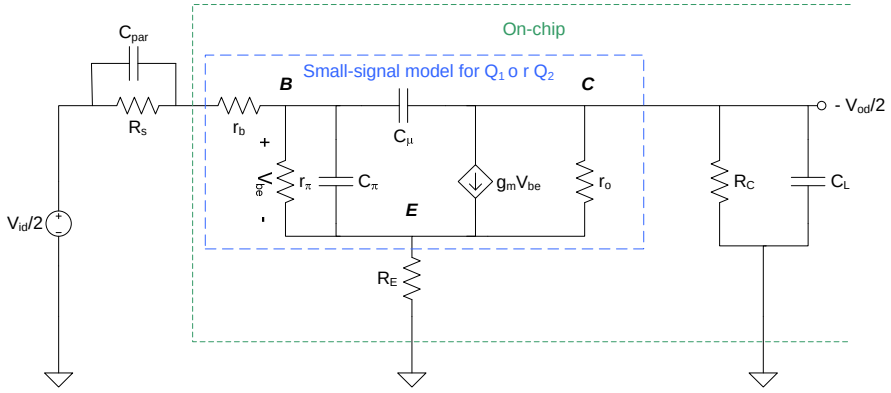

Figure 4-6. Small-signal equivalent half circuit of the differential input stage of the preamplifier.

[p] Input resistance of Q_3-Q_4 is much higher than R_C and can be simplified.

The contribution of C_{par} depends on the external conditions and will not be included in the preamplifier response. The zero-value time constant analysis method ([66]) will be used to estimate the bandwidth ω_{-3dB} of the circuit in Figure 4-7. According to this method, if there are no dominant zeros in the circuit transfer function,

$$\omega_{-3dB} \approx \frac{1}{\sum T_0} \qquad (4.12)$$

where $\sum T_0$ is the sum of the zero-value time constants. A zero-value time constant is the time constant of each capacitor of the circuit times the driving-point resistance at its nodes with all other capacitors put equal to zero (open circuit).

The first time constant corresponds to C_π, which is composed by the base-charging capacitance C_b and the emitter-base depletion layer capacitance C_{je}. The base-charging or diffusion capacitance is an apparent input capacitance. The variation in v_{BE} causes a variation of the injected charge Q_F in the base which is accumulated in the base and then diffuses to the collector [67]. The ratio of the variations has capacitance units $C_b = \frac{dQ_F}{dv_{be}} = \frac{dQ_F}{di_c}\frac{di_c}{dv_{be}} = \tau_F g_m$, where i_c is the collector current and τ_F is the base transit time. The base transit time τ_F is the average time in which the electrons diffuse through the base from the emitter side to the collector side. Is thus a measure of the maximum frequency of the transistor: $f_{T_{max}} = 1/2\pi\tau_F$. For the selected BiCMOS technology and transistor size τ_F is about 8.1 ps [73] and being $i_c = I_{bias}/2 = 0.5$ mA, $g_m = i_C/(kT/q)$ is 0.02 S, thus C_b is about 160 fF. The BE junction is forward biased in the operation of the amplifier; therefore C_{je} corresponds to the capacitance of a forward biased PN junction. Using the Gummel-Poon model (see Appendix A: A.1.1), C_{je} is about 56 fF and then C_π is about 236 fF. The driving-point resistance $R_{\pi 0}$ of C_π is $R_{\pi 0} = r_\pi \,||\, \frac{R_S + r_b + R_E}{1 + g_m R_E}$ (see section 7.3 in [66]). The input resistance r_π is the ratio between the ac component v_{be} and the ac component of i_b: $r_\pi = \frac{dv_{be}}{di_c}\frac{di_c}{di_b} = \frac{\beta_{AC}}{g_m}$, where β_{AC} is the current gain at a particular collector current, as $\beta \approx 100$, r_π is about 50KΩ. The base resistance r_b is related to the large resistivity underneath the emitter and it is 180 Ω (see Appendix A: A.1.4). With an emitter resistance R_E equal to 460 Ω and a R_S equal to 470 Ω, $R_{\pi 0}$ is about 108 Ω and the zero time constant $\tau_{C\pi}$ is 26 ps.

The half circuit model is exactly the same as the common-emitter (CE) amplifier with emitter degeneration. In [66] it is shown that a common-emitter amplifier can be simplified to a two-port equivalent circuit. Small-signal half circuit with this simplification and without the contribution of C_π which has been already evaluated is shown in Figure 4-7.

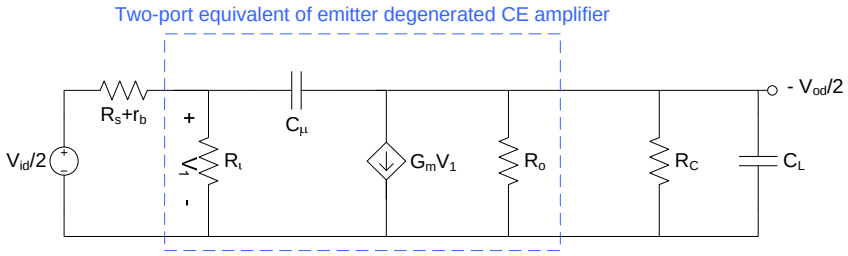

Figure 4-7. Small signal model of the half-circuit of the differential input stage of the preamplifier with CE amplifier with emitter degeneration equivalent circuit (without the contribution of C_π).

The new transconductance G_m of the equivalent two port circuit is given by,

$$G_m \simeq \left(\frac{g_m}{1 + g_m R_E} \right) \qquad (4.13)$$

Input resistance R_i is,

$$R_i \simeq r_\pi \left(1 + g_m R_E\right) \qquad (4.14)$$

Output resistance R_o is,

$$R_o \simeq r_o \left(1 + g_m R_E\right) \qquad (4.15)$$

The emitter degeneration can be regarded as a local series-series feedback, therefore both input resistance and output resistance are increased by the application of emitter feedback. For this circuit this in convenient in both cases.

The transconductance G_m of the stage benefits also from feedback: if $g_m R_E >> 1$, then $G_m \approx 1/R_E$. The differential mode voltage gain (A_{DM}) for low frequencies ($\omega << \omega_{-3dB}$) is given by,

$$\frac{v_{oD}}{v_{iD}} = A_{DM} = G_m R_C \simeq \frac{R_C}{R_E} \qquad (4.16)$$

The voltage gain of the stage depends on the ratio of two precise and matched polysilicon resistors, not on the bipolar transconductance, thus minimizing the effect of process variations. *For these reasons, the emitter degeneration will be employed in many open and closed loop blocks of the design.*

The second zero time constant corresponds to C_μ which is the base-collector junction capacitance C_{jc} and it is reverse biased for the operation in the active region, using the Gummel-Poon model (see Appendix A: A.1.2) an approximation for its value is12 fF. Taking the simplified model of Figure 4-7, it can be shown (section 7.3. in [66]) that the resistance R_μ seen across the terminals of C_μ is

$$R_\mu = R_i \,||\, (R_S + r_b) + R_C + G_m R_C \left(R_i \,||\, (R_S + r_b)\right) \qquad (4.17)$$

The term $G_m R_C$ corresponds to the voltage gain of the stage and it will multiply the time constant $\left(R_i \,||\, (R_S + r_b)\right) C_\mu$ that usually becomes the dominant term for this zero time constant. This effect can be regarded also as the creation of an apparent input capacitance which is C_μ times the voltage gain of the circuit, this is the so-called Miller effect. The value of R_μ is 5.14 KΩ and the zero time constant $\tau_{C\mu}$ is 62 ps.

The third time constant corresponds to C_L, which corresponds essentially to the collector substrate capacitance C_{js} and to the input capacitance of the emitter follower (Q_3 or Q_4) of the output. The former corresponds to a reverse junction depletion capacitance (usually the largest junction capacitance because it covers the largest area) and is about 113 fF (see Appendix A: A.1.3). Neglecting the effect of the base resistance, the latter can be approximated by the C_π capacitance of the transistors Q_3 or Q_4 and, taking into account that the scaling factor, both in area and in currents between Q_1-Q_2 and Q_3-Q_4 is 2, it should the half of the C_π of Q_1-Q_2, that is to say 118 fF. Therefore C_L is about 230 fF .The load capacitance sees a resistance equal to R_C, since the input resistance of Q_3 or Q_4 is much higher than R_C (2.4 KΩ) and it is in parallel. Thus the value of the zero time constant associated to C_L, named τ_{CL} is about 552 ps and will be the dominant one.

Thus the bandwidth of the input stage is,

$$f_{-3dB} \approx \frac{1}{2\pi \sum T_0} = \frac{1}{2\pi \left(26\ ps + 62\ ps + 552\ ps\right)} \approx 250\ MHz \qquad (4.18)$$

The output stage is a classical emitter follower configuration (Q_3 for V_{oL} and Q_4 for V_{oH}). It provides good capability of load driving thanks to its low output impedance (about 200 Ω in this case)

and voltage gain close to unity. If the load resistance of the emitter follower is much higher than the source resistance the pole of its transfer function is close to the ω_T of the device [66]. In this case the condition is fulfilled since the source resistance is the base resistance of the transistor (about 1 KΩ) and the load resistance is the output resistance of the current source in parallel with the input resistance of the next stage (much higher than 10 KΩ). Therefore, the frequency response is dominated by the pole of differential input stage.

Figure 4-8 shows a Spectre simulation of the frequency response of the preamplifier as a function of the input resistor or PMT load resistor (R_S). The bandwidth for its nominal value R_S = 470 Ω is 257 MHz for a load resistance of 100 KΩ and load capacitance (after the emitter follower) of 100 fF, which is in reasonably good agreement with the zero time constant estimation. The DC voltage gain is 4.5 or 13.1 dB, this is a bit lower than the ratio R_C/R_E = 5.2. The condition $g_mR_E>>1$ is hold only partially since g_mR_E=8.5. The non simplified expression for the voltage gain $\frac{v_o}{v_i} = G_m R_C = \left(\frac{g_m}{1+g_m R_E}\right) R_C = 4.67$ gives a more accurate result. A higher R_E would improve the performance of the emitter feedback but other considerations, such as noise, must be taken into account. In Figure 4-8 it is also shown that small values of R_S do not affect the frequency response of the preamplifier because other terms dominate. When R_S (4.7 Ω and 47 Ω) is much smaller than the base resistance r_b the effect is completely negligible. For R_S = 470 Ω there is some effect but still the contribution of the C_L capacitance is dominant. For R_S = 4k7 Ω the time constant related to $\tau_{C\mu}$ is about 360 ps, comparable to τC_L and the effect on the bandwidth is quit relevant. For R_S = 47 kΩ, $\tau_{C\mu}$ = 3.6 ns (BW about 40 MHz) would be the dominating time constant.

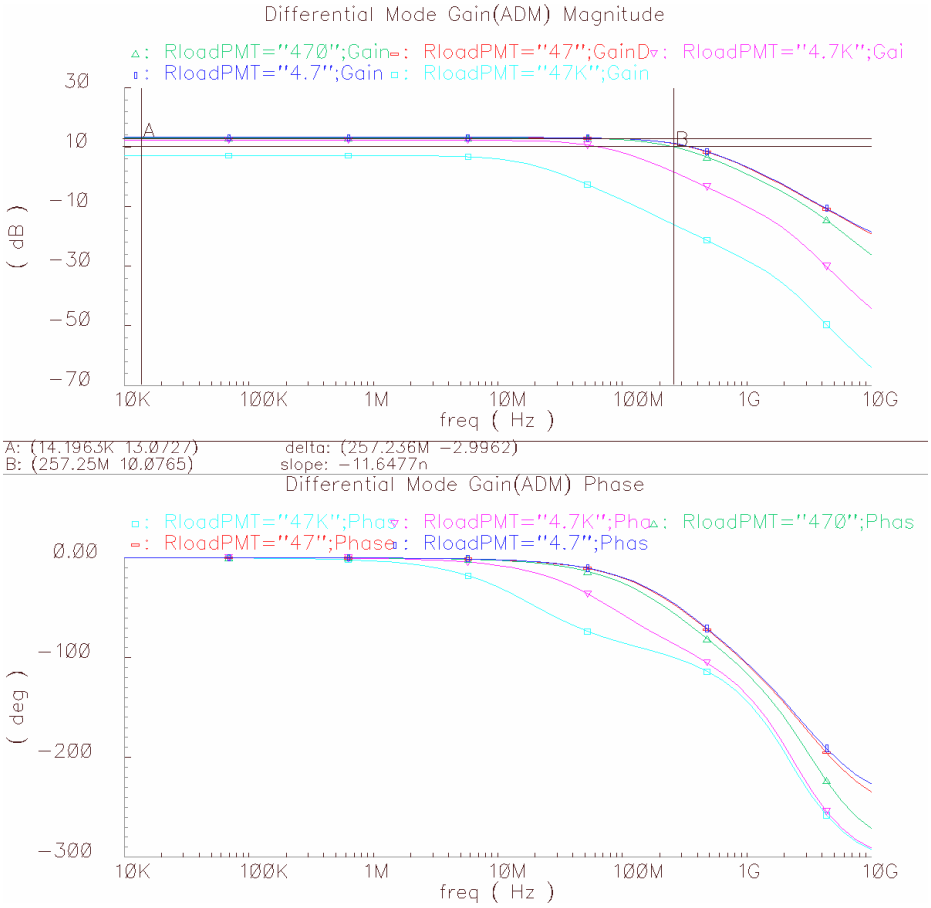

Figure 4-8. Simulation of the frequency response (DM gain) of the preamplifier for different PMT resistor loads (RloadPMT is R_S). Magnitude (in dB) at top and phase at bottom.

Although the zero time constant analysis is an approximation with certain error, especially when the circuit has not a dominant pole [66], it gives useful information on the contribution of different circuit nodes or elements to the overall frequency response. In order to check the first order estimation of the values of the non-dominants zero time constants, the response of the circuit is simulated for each capacitor contribution with other capacitors put equal to zero (open circuit). Doing this the inverse of the dominant pole (by simulation) for C_π is 29 ps, for C_μ is 53 ps and for C_{js} is 250 ps which are in quite good agreement with the estimations [q].

Post layout simulations, taking into account the effect of stray and other parasitic capacitances have been performed, and the cut off frequency is reduced down to 180 MHz mainly due to the poly to substrate parasitic capacitance of the poly resistors R_C and also R_E. The effect of load capacitance (the input capacitance of the integrator, which will be of the order of C_π) is negligible up to 1 pF (bandwidth of 174 MHz), for 10 pF the cut off frequency is reduced down to 88 MHz.

4.2.1.3 Common mode gain

Bias current source lies along the topological line of symmetry that divides the preamplifier circuit of Figure 4-3 in two identical parts. Such elements carry a current twice that present in one side and therefore its impedance in common-mode half circuit must be twice. In other words, elements lying along the line of symmetry can be split into two identical parallel elements. Of course, the value of parallel elements has to be chosen so that its parallel combination results in the original one, i.e. if they are impedances the value of element in common-mode half circuit is twice the value of the original one but if they are current sources the value of the element in common-mode half circuit is half the value of the original. This is depicted in Figure 4-9 for the bias current source.

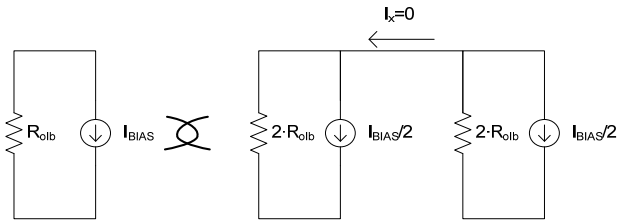

Figure 4-9. Splitting a current source into two equivalent identical parallel networks.

For common-mode signals, the two halves of the circuit are not only identical, but also independent because they are joined by a branch (the connection of the emitter of Q_1 and Q_2) that conducts no small-signal current (i_x=0). The small signal response of the preamplifier to the common-mode (CM) input voltage V_{iC} can be analyzed through the half-mod common circuit, shown in Figure 4-10. The output resistance R_{oIb} and output capacitance C_{oIb} of the current source I_{BIAS} are split into two parallel resistors, each of value twice of the original, and into two parallel capacitors (each of half of C_{oIb}) respectively.

[q] It was not possible with the simulation methods available to put to 0 Cπ of Q_1-Q_2 without putting to 0 Cπ of Q_3-Q_4, only the substrate collector capacitance of C_L can be compared. Hand estimation for C_{js0} time constant is 270 ps

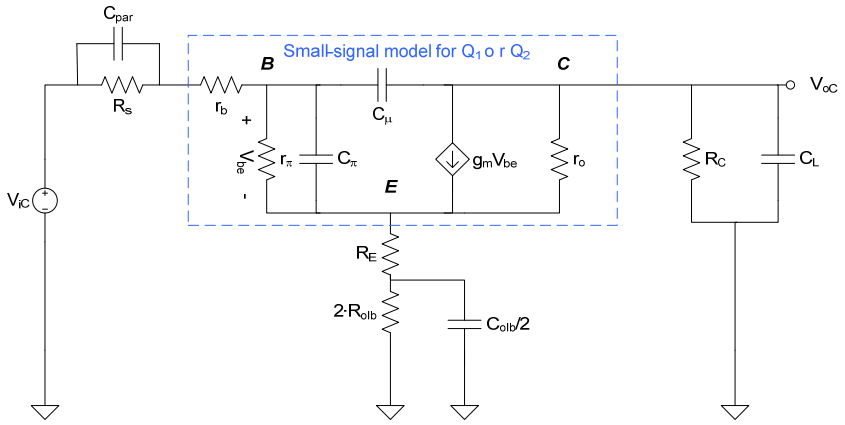

Figure 4-10. Small signal equivalent common mode circuit.

The low frequency gain is exactly the same as the differential mode (DM) half circuit, but with an emitter resistor equal to $R_E + R_{oIb}$. Therefore, the low frequency CM gain (A_{CM}) is:

$$\frac{v_{oC}}{v_{iC}} = A_{CM} = -G_m R_C \simeq -\frac{R_C}{R_E + 2R_{oIb}} \qquad (4.19)$$

As first approximation to study the high frequency CM gain, it is assumed that C_{oIb} is the only significant capacitance. We replace the current source resistance R_{oIb} by the complex impedance $Z_{oIb}(s) = 2R_{oIb} \,||\, \frac{1}{s \cdot C_{oIb}/2} = \frac{2R_{oIb}}{1 + sR_{oIb}C_{oIb}}$ in expression (4.19) having

$$A_{CM}(s) \approx -\frac{R_C}{R_E} \frac{s + 1/R_{oIb}C_{oIb}}{s + 1/0.5R_E C_{oIb}} \qquad (4.20)$$

The current source of the preamplifier is composed by 8 units in parallel, therefore the output resistance R_{oIb} is about 135 KΩ (see section 4.5.1. Bias current). The capacitance C_{oIb} has two components that are added (are in parallel):

- The collector to substrate capacitance of the bipolar transistors of the current source, for eight current units in parallel it is about 350 fF (see appendix A.1.5).
- The base to collector capacitance of the bipolar transistors of the current sources in series with a big decoupling capacitor (500 fF) between base of the current master and the negative rail (AC ground). According to A.1.6 the base collector depletion capacitance for the eight current units in parallel is about 100 fF.

Thus C_{oIb} is about 450 fF and the zero $1/ 2\pi C_{oIb}R_{oIb}$ for the CM gain is about 2.5 MHz and the pole about 1.5 GHz. The CM gain has a dominant zero at about 2 MHz, which causes the CM gain to rise at 6dB/octave above this frequency. The increase in CM gain is undesirable because it should ideally be as small as possible.

Figure 4-11 shows the simulated CM response of the preamplifier. A dominant zero is found a 1.8 MHz, close to the approximation of $1/ 2\pi C_{oIb}R_{oIb}$. The CM gain at low frequencies is -40.4 dB or 9.5e-3, according to (4.20) it should be about $R_C/2R_{oIb} \approx 9e\text{-}3$. The other capacitors cause the CM gain to fall at higher frequencies.

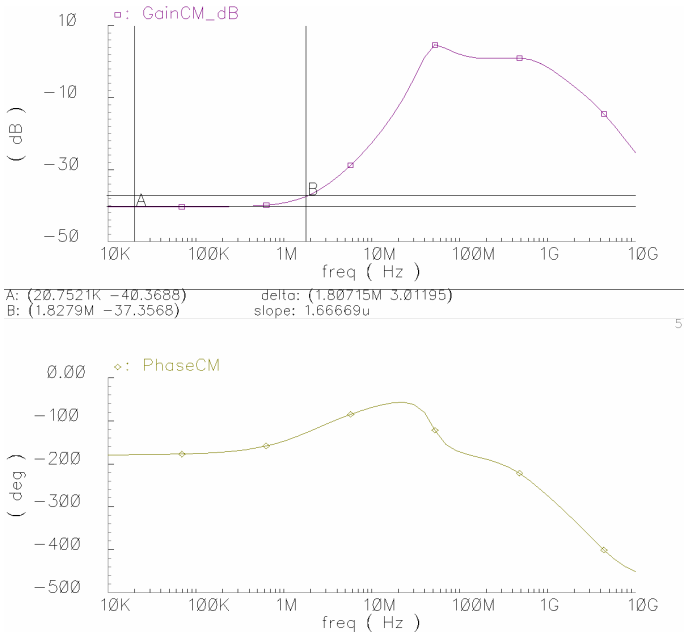

Figure 4-11. Simulation of the CM gain of the preamplifier. Magnitude at top and phase at bottom.

The ratio $|A_{DM}|/|A_{CM}|$ is called [132] discrimination factor for differential amplifiers, although in single-ended amplifiers it is known as common mode rejection ratio (CMRR). Figure 4-12 shows the discrimination factor of the preamplifier. There is a dominant pole at the frequency corresponding to dominant zero of A_{CM}.

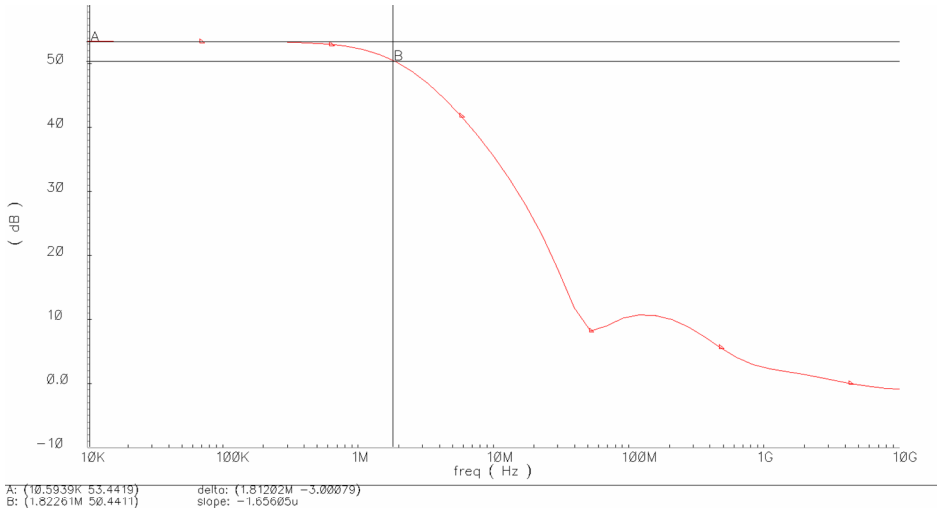

Figure 4-12. Simulation of the discrimination factor of the preamplifier.

4.2.1.4 Device mismatch effects in the transfer function of the preamplifier.

In differential amplifiers with perfect symmetry, each component on the side of one output corresponds to an identical component on the side of the other output. In those perfectly balanced amplifiers the common mode value of the inputs has no effect on the differential mode output and the differential mode value of inputs has no effect on common mode output, but the tolerances of the fabrication process cause that there are no perfectly balanced amplifiers. Taking into account this effect. four gains are needed to define the transfer function of a differential amplifier,

$$V_{oD} = A_{DM}V_{iD} + A_{CM-DM}V_{iC}$$
$$V_{oC} = A_{DM-CM}V_{iD} + A_{CM}V_{iC} \qquad (4.21)$$

It is useful to refer to the relevant input, the differential one, the effects on the differential output

$$V_{oD} = A_{DM}\left(V_{iD} + \frac{A_{CM-DM}}{A_{DM}}V_{iC}\right) = A_{DM}\left(V_{iD} + \frac{1}{CMRR}V_{iC}\right) \qquad (4.22)$$

From (4.22) we define the CMRR

$$CMRR \equiv \frac{A_{DM}}{A_{CM-DM}} \qquad (4.23)$$

it corresponds to the ratio or relative value of differential-mode output produced by differential-mode and common-mode inputs.

In [132] and [66] a half-circuit method to analyze the effect of device mismatches in gain is presented. Common mode and differential mode half circuits with mismatch generators are shown in Figure 4-13. ΔR and Δg_m (depends on saturation current mismatch I_S) are the mismatch or difference of the resistance and transconductance values between an ideally matched resistor pair or between an ideally matched transistor pair. Mismatch in other small-signal parameters of bipolar transistor such Δr_π (depends on I_S and β mismatches) or Δr_o (depends on I_S mismatch) could be considered, however all these parameters depend at the end on saturation current and β mismatches, which are not independent since both depend on the same physical parameters (base width, doping densities, emitter area, etc). Indeed, the β mismatch and g_m mismatch in the Austriamicrosystem Monte Carlo npn121 transistor model depend on the same random variable, so they are fully correlated. For the analysis of mismatch in gain (and for PSRR) it is enough to consider transconductance mismatch Δg_m in bipolar transistors, because it is by far the most relevant paremeter of the bipolar transistor in most small signal circuits.

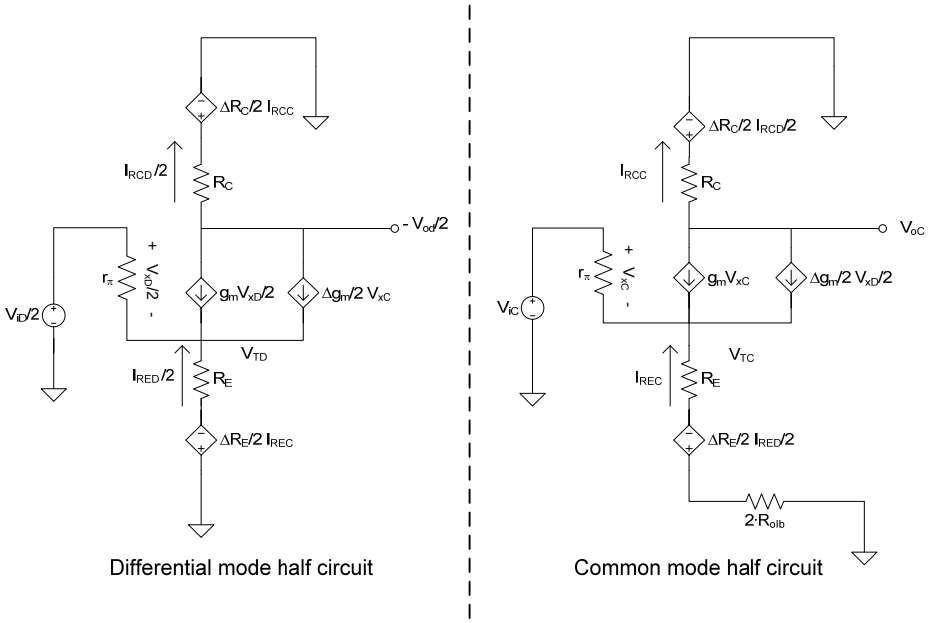

Figure 4-13. DM (right) and CM (left) half circuits with mismatch generators.

Taking into account the mismatch terms common mode and differential mode half circuits are not independent but coupled: the common mode signal depends in part on the differential signals and viceversa. Using the following differential half circuit equations,

$$V_{TD} = \left(g_m \frac{V_{xD}}{2} + \frac{\Delta g_m}{2} V_{xC} + \frac{1}{r_\pi} \frac{V_{xD}}{2} \right) R_E - \frac{\Delta R_E}{2} I_{REC}$$
$$\frac{V_{oD}}{2} = \left(g_m \frac{V_{xD}}{2} + \frac{\Delta g_m}{2} V_{xC} \right) R_C - \frac{\Delta R_C}{2} I_{RCC} \qquad (4.24)$$
$$\frac{V_{xD}}{2} = \frac{V_{iD}}{2} - V_{TD}$$

The V_{oD} equation of (4.21) can be obtained, and with $1/r_\pi \ll g_m$,

$$\frac{V_{oD}}{2} = \frac{g_m R_C}{1+g_m R_E} \frac{V_{iD}}{2} - \frac{g_m R_C}{1+g_m R_E} R_E \frac{\Delta g_m}{2} V_{xC} + \frac{g_m R_C}{1+g_m R_E} \frac{\Delta R_E}{2} I_{REC} + R_C \frac{\Delta g_m}{2} V_{xC} - \frac{\Delta R_C}{2} I_{RCC} \quad (4.25)$$

In the same way, for the common mode circuit,

$$V_{TC} = \left(g_m V_{xC} + \frac{\Delta g_m}{2} \frac{V_{xD}}{2} + \frac{V_{xC}}{r_\pi} \right) \left(R_E + 2R_{olb} \right) - \frac{\Delta R_E}{2} \frac{I_{RED}}{2}$$
$$V_{oC} = -\left(g_m V_{xC} + \frac{\Delta g_m}{2} \frac{V_{xD}}{2} \right) R_C + \frac{\Delta R_C}{2} \frac{I_{RCD}}{2} \qquad (4.26)$$
$$V_{xC} = V_{iC} - V_{TC}$$

The V_{oC} equation of (4.21) would be ($1/r_\pi \ll g_m$),

$$V_{oC} = -\frac{g_m R_C}{1+g_m \left(R_E + 2R_{olbE} \right)} V_{iC} + \frac{g_m R_C}{1+g_m \left(R_E + 2R_{olbE} \right)} \left(R_E + 2R_{olbE} \right) \frac{\Delta g_m}{2} \frac{V_{xD}}{2}$$
$$- \frac{g_m R_C}{1+g_m \left(R_E + 2R_{olbE} \right)} \frac{\Delta R_E}{2} \frac{I_{RED}}{2} - R_C \frac{\Delta g_m}{2} \frac{V_{xD}}{2} + \frac{\Delta R_C}{2} \frac{I_{RED}}{2} \qquad (4.27)$$

Although the analysis of half-circuits gives exact results, it requires simultaneous consideration of both circuits (circuits are coupled through the mismatch terms), which is about as complicated as the direct analysis of the entire circuit. In practice, the mismatch terms are usually a small fraction of the corresponding average values. As a result, the dominant contributions to the differential signals that control the mismatch generators in the common-mode half circuit stem from differential inputs. Similarly, the dominant part of the common mode signals that control the mismatch generators in the differential half circuit arise from common-mode inputs. Therefore, we will assume that the signals controlling the mismatch generators can be found approximately by analyzing each half circuit independently without mismatch, as in Figure 4-14. The signals that control mismatch generators in Figure 4-13 are I_{RCC}, I_{REC}, V_{xC}, $I_{RCD}/2$, $I_{RED}/2$ and $V_{xD}/2$. We will find approximations to these quantities, I_{RCC}, I_{REC}, V_{xC}, $I_{RCD}/2$, $I_{RED}/2$ and $V_{xD}/2$.

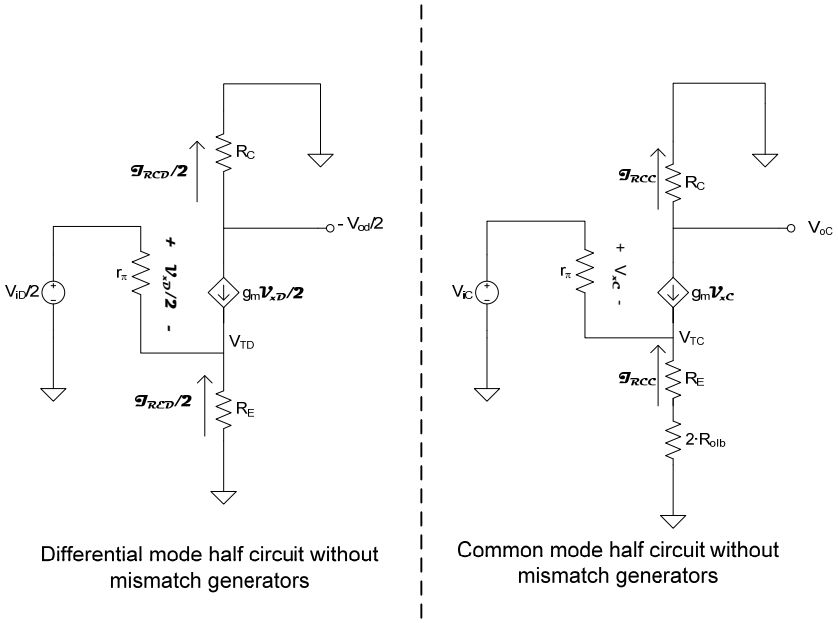

Figure 4-14. Differential mode (right) and common mode (left) half circuits without mismatch generators.

Using the half circuits shown in Figure 4-14, where the mismatch terms are set to zero,

$$\begin{aligned}
&\frac{\boldsymbol{v}_{xD}}{\boldsymbol{2}} = \frac{V_{iD}}{2} - g_m \frac{\boldsymbol{v}_{xD}}{\boldsymbol{2}} R_E = \frac{1}{1+g_m R_E}\frac{V_{iD}}{2} \\
&\frac{\boldsymbol{\mathcal{I}}_{RCD}}{\boldsymbol{2}} = \frac{\boldsymbol{\mathcal{I}}_{RED}}{\boldsymbol{2}} = -g_m \frac{\boldsymbol{v}_{xD}}{\boldsymbol{2}} = -g_m \frac{1}{1+g_m R_E}\frac{V_{iD}}{2} \\
&\boldsymbol{v}_{xC} = V_{iC} - g_m \boldsymbol{v}_{xC}\left(R_E + 2R_{olb}\right) = \frac{V_{iC}}{1+g_m\left(R_E+2R_{olb}\right)} \\
&\boldsymbol{\mathcal{I}}_{RCC} = \boldsymbol{\mathcal{I}}_{REC} = -g_m \boldsymbol{v}_{xC} = -g_m \frac{V_{iC}}{1+g_m\left(R_E+2R_{olb}\right)}
\end{aligned} \tag{4.28}$$

Therefore, replacing I_{RCC} by $\boldsymbol{\mathcal{I}}_{RCC}$, I_{REC} by $\boldsymbol{\mathcal{I}}_{REC}$ and V_{xC} by $\boldsymbol{v}_{xC}$ in (4.25) the approximated differential-mode output voltage is:

$$\begin{aligned}
\frac{V_{oD}}{2} \simeq{}& \frac{g_m R_C}{1+g_m R_E}\frac{V_{iD}}{2} - \frac{g_m R_C}{1+g_m R_E} R_E \frac{\Delta g_m}{2}\frac{V_{iC}}{1+g_m\left(R_E+2R_{olb}\right)} - \frac{g_m R_C}{1+g_m R_E}\frac{\Delta R_E}{2} g_m \frac{V_{iC}}{1+g_m\left(R_E+2R_{olb}\right)} + \\
&+ R_C \frac{\Delta g_m}{2}\frac{V_{iC}}{1+g_m\left(R_E+2R_{olb}\right)} + \frac{\Delta R_C}{2} g_m \frac{V_{iC}}{1+g_m\left(R_E+2R_{olb}\right)}
\end{aligned} \tag{4.29}$$

In the same way $I_{RCD}/2$ by $\boldsymbol{\mathcal{I}}_{RCD}/\boldsymbol{2}$, $I_{RED}/2$ by $\boldsymbol{\mathcal{I}}_{RED}/\boldsymbol{2}$ and $V_{xD}/2$ by $\boldsymbol{v}_{xD}/\boldsymbol{2}$ in (4.27) the approximated common-mode output voltage is:

$$\begin{aligned}
V_{oC} \simeq{}& -\frac{g_m R_C}{1+g_m\left(R_E+2R_{olbE}\right)} V_{iC} + \frac{g_m R_C}{1+g_m\left(R_E+2R_{olbE}\right)}\left(R_E+2R_{olbE}\right)\frac{\Delta g_m}{2}\frac{1}{1+g_m R_E}\frac{V_{iD}}{2} + \\
&+ \frac{g_m R_C}{1+g_m\left(R_E+2R_{olbE}\right)}\frac{\Delta R_E}{2} g_m \frac{1}{1+g_m R_E}\frac{V_{iD}}{2} - R_C \frac{\Delta g_m}{2}\frac{1}{1+g_m R_E}\frac{V_{iD}}{2} - \frac{\Delta R_C}{2} g_m \frac{1}{1+g_m R_E}\frac{V_{iD}}{2}
\end{aligned} \tag{4.30}$$

From (4.28) and (4.29) the differential-mode to differential-mode voltage gain (A_{DM}) is,

$$A_{DM} \equiv \left.\frac{V_{oD}}{V_{iD}}\right|_{V_{iC}=0} \simeq \frac{g_m R_C}{1+g_m R_E} \tag{4.31}$$

A_{DM} is approximately equal to the Differential Mode gain derived in previous sections without considering the mismatch. The common-mode to differential-mode voltage gain ($A_{CM\text{-}DM}$) is,

$$\begin{aligned} A_{CM-DM} &\equiv \left.\frac{V_{oD}}{V_{iC}}\right|_{V_{iD}=0} \simeq \frac{1}{1+g_m\left(R_E+2R_{olb}\right)}\left(-\frac{g_m R_C R_E}{1+g_m R_E}\Delta g_m - \frac{g_m^2 R_C}{1+g_m R_E}\Delta R_E + \Delta g_m R_C + \Delta R_C g_m\right) = \\ &= \frac{1}{1+g_m\left(R_E+2R_{olb}\right)}\left(\frac{R_C}{1+g_m R_E}\Delta g_m - \frac{g_m^2 R_C}{1+g_m R_E}\Delta R_E + \Delta R_C g_m\right) \simeq \\ &\simeq \Big|_{g_m(R_E+2R_{olb})\gg 1} \frac{R_C}{\left(R_E+2R_{olb}\right)}\left(\frac{1}{1+g_m R_E}\frac{\Delta g_m}{g_m} - \frac{g_m}{1+g_m R_E}\Delta R_E + \frac{\Delta R_C}{R_C}\right) \simeq \\ &\simeq \Big|_{g_m R_E\gg 1} \frac{R_C}{\left(R_E+2R_{olb}\right)}\left(\frac{1}{1+g_m R_E}\frac{\Delta g_m}{g_m} - \frac{\Delta R_E}{R_E} + \frac{\Delta R_C}{R_C}\right) \end{aligned} \tag{4.32}$$

$A_{CM\text{-}DM}$ is very important since it provides estimation on the effect of common-mode input signals such pick up noise on the differential output. It is crucial to minimize it; because once such signals are converted to differential-mode they will be undistinguishable from the ordinary differential signal. It is also interesting to note that the transistor mismatch term (usually bigger than resistor mismatch) is "attenuated" in (4.32), its impact in $A_{CM\text{-}DM}$ is inversely proportional to $g_m R_E$. Also note that to have a high output impedance current source is very important to minimize $A_{CM\text{-}DM}$.

From (4.28) and (4.30) the common-mode to common-mode voltage gain (A_{CM}) is,

$$A_{CM} \equiv \left.\frac{V_{oC}}{V_{iC}}\right|_{V_{iD}=0} \simeq -\frac{g_m R_C}{1+g_m\left(R_E+2R_{olbE}\right)} \simeq \Big|_{g_m(R_E+2R_{olbE})\gg 1} -\frac{R_C}{R_E+2R_{olbE}} \tag{4.33}$$

and the differential-mode to common-mode voltage gain ($A_{DM\text{-}CM}$) is,

$$\begin{aligned} A_{DM-CM} &\equiv \left.\frac{V_{oC}}{V_{iD}}\right|_{V_{iC}=0} \simeq \frac{\left(R_E+2R_{olbE}\right)}{1+g_m\left(R_E+2R_{olbE}\right)}\frac{g_m R_C}{1+g_m R_E}\frac{\Delta g_m}{4} + \frac{g_m R_C}{1+g_m\left(R_E+2R_{olbE}\right)}\frac{g_m}{1+g_m R_E}\frac{\Delta R_E}{4} - \\ &- \frac{R_C}{1+g_m R_E}\frac{\Delta g_m}{4} - \frac{g_m}{1+g_m R_E}\frac{\Delta R_C}{4} = \\ &= \frac{1}{1+g_m\left(R_E+2R_{olbE}\right)}\frac{g_m R_C}{1+g_m R_E}\frac{1}{4}\left(\frac{\Delta g_m}{g_m} + g_m \Delta R_E\right) - \frac{g_m}{1+g_m R_E}\frac{\Delta R_C}{4} \simeq \\ &\simeq \Big|_{\substack{g_m(R_E+2R_{olbE})\gg 1 \\ g_m R_E\gg 1}} \frac{1}{4}\frac{R_C}{R_E+2R_{olbE}}\left(\frac{1}{g_m R_E}\frac{\Delta g_m}{g_m} + \frac{\Delta R_E}{R_E}\right) - \frac{1}{4}\frac{R_C}{R_E}\frac{\Delta R_C}{R_C} \end{aligned} \tag{4.34}$$

Note that in (4.34) the transistor and emitter resistor mismatch terms are canceled if $g_m(R_E+2R_{olb})>>1$ and that the term corresponding to R_C mismatch does not cancel even for R_{olb} approaching to infinite.

Mismatch factors ΔR, Δr_π and Δg_m are actually random parameters that take on a different value for each circuit fabricated, and the distribution of the observed values is described by a probability distribution. Thus, expressions (4.32) and (4.34) relate respectively the $A_{CM\text{-}DM}$ and the $A_{DM\text{-}CM}$ gains to the mismatch of a given circuit sample. A parameter of more interest to the circuit designer than the $A_{CM\text{-}DM}$ and the $A_{DM\text{-}CM}$ of one sample is the mean and the standard deviation of the random variable determined by the device mismatch, i.e. $A_{CM\text{-}DM}$ and the $A_{DM\text{-}CM}$ gains on this case. Mean $A_{CM\text{-}DM}$ and the $A_{DM\text{-}CM}$ gains should be zero, since there is no systematic mismatch in the circuit design or layout.

Figure 4-15 shows the result of ten Monte Carlo simulation runs for A_{CM-DM} and the A_{DM} gains. Both process and mismatch variations are simulated. Note that for the A_{DM} gain there is a clear systematic component whereas for the A_{CM-DM} gain the mean value is about zero (phase changes from 0º to -180º from iteration to iteration).

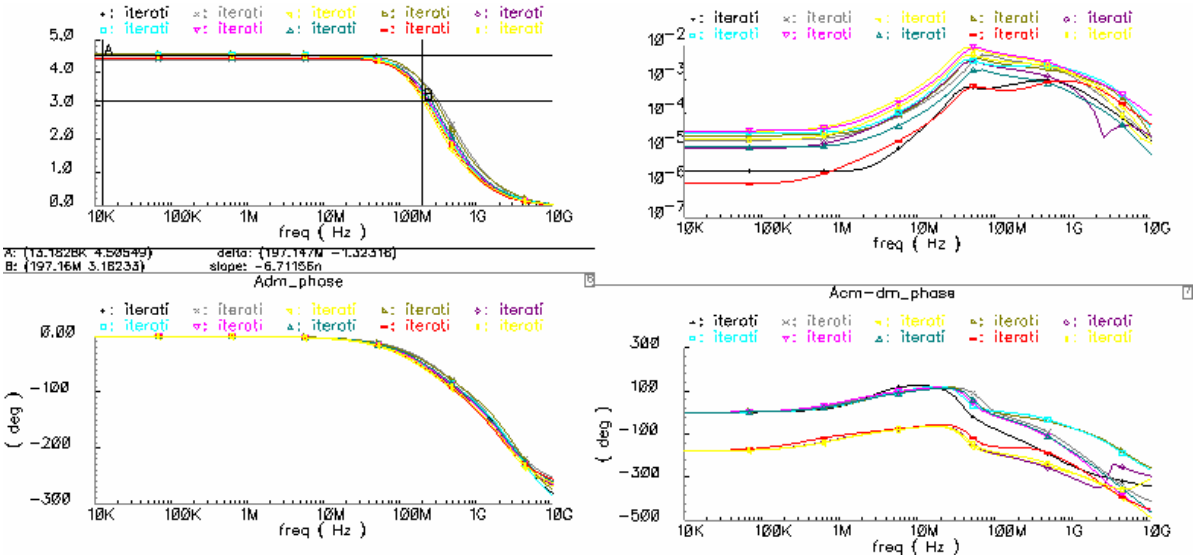

Figure 4-15. Monte Carlo simulations (10 runs) for the A_{DM} (left) and the A_{CM-DM} (right) gains. Magnitude at top and phase at bottom. Process and mismatch variations.

Although expressions for A_{DM} gain do not show any dependence on mismatch from Figure 4-15 it is clear that it exists. In order to simplify the calculations the controlling signals of the mismatch generators of the differential-mode half circuit was derived from the common-mode circuit without mismatch generators, therefore the controlling signals of mismatch generators of the differential-mode half circuit only depend on common-mode input signals in the expression (4.29). If the controlling signals of the mismatch generators of the differential-mode half circuit were derived from the common-mode circuit with mismatch generators the mismatch generators of the differential-mode circuits would have depend on differential input signals also, introducing a dependence on the mismatch for the A_{DM} gain. However, this dependence is not significant compared to the systematic component. Even if we think on evaluating circuit tolerances becomes irrelevant compared to tolerances introduced by process variations, as will be shown later.

The cut off frequency of the A_{DM} gain is about 200 MHz for the worst case. For A_{CM-DM} gain, as in the case of A_{CM} gain, there is a dominant zero at $1/ 2\pi C_{olb}R_{olb}$ (about 2 MHz) for the same reason: if we compare expression (4.32) with expression (4.19) we see that both depend on $1/ Z_{olb}(s)$ and for frequencies higher than 1 MHz the effect of C_{olb} becomes relevant and the current source impedance begins to drop and the gain increases. For higher frequencies the effect of non-dominant poles becomes evident.

Figure 4-16 shows the result of ten Monte Carlo simulation runs for A_{DM-CM} and the A_{CM} gains. Both process and mismatch variations are simulated. Also note that for the A_{CM} gain there is a clear systematic component whereas for the A_{DM-CM} gain the mean value is about zero (phase changes).

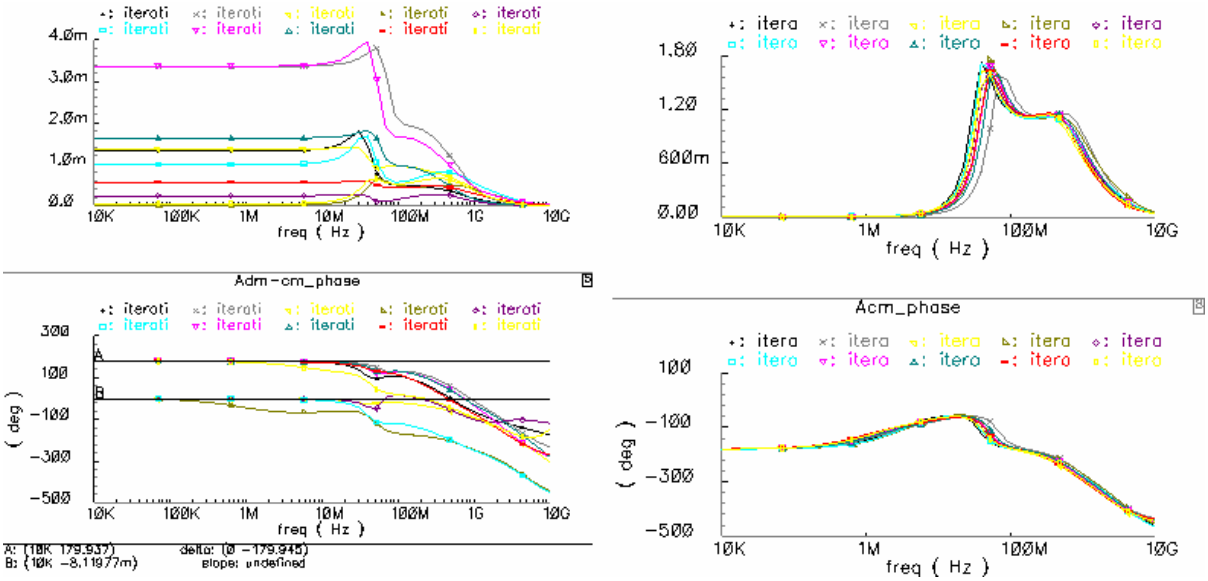

Figure 4-16. Monte Carlo simulations (10 runs) for the A_{DM-CM} (left) and the A_{CM} (right) gains. Magnitude at top and phase at bottom. Process and mismatch variations.

As analyzed in section 4.2.1.3 A_{CM} gain has a dominant zero at about 2 MHz. The case of A_{DM-CM} is more subtle: if we look at expression (4.34) we see that there is a first term that depends of current source impedance Z_{olb} and a second one that depends on R_C. For the first term one may expect the same behavior found for A_{CM-DM} and A_{CM} gains: Z_{olb} starts to drop at 2 MHz and this is seen as a dominant zero in the frequency response. As the time constant associated to R_C is much smaller, the second term is constant at such frequencies. Then, and taking into account that the magnitude of second term is typically much higher, the effect of the dominant zero related to Z_{olb} is typically annulated or visible only at higher frequencies (depending on the Monte Carlo run) where the decrease of Z_{olb} makes the magnitude of the first comparable to the second one.

Since the A_{CM-DM} (4.32) and the A_{DM-CM} (4.34) gains are the sum of uncorrelated random parameters, the standard deviation of the sum is equal to the square root of the sum of the squares of the standard deviation of the mismatch contributions. The typical resistor standard deviation $\sigma_{\Delta R_E/R}$ of 0.25 % and $\sigma_{\Delta R_C/R}$ of 0.22 % can be computed directly from [73]. The variance of the transconductance mismatch $\sigma^2_{\Delta g_m}$ related to process variations can be estimated through the dependence on collector current: $g_m = \frac{1}{V_T} I_C$ and considering that the mismatch of collector current is given by the mismatch in saturation current I_S for the Monte Carlo transistor model then,

$$\frac{\sigma_{\Delta g_m}}{g_m} = \frac{\sigma_{\Delta I_C}}{I_C} = \frac{\sigma_{\Delta I_S}}{I_S} \qquad (4.35)$$

According to [73] and [162] for an emitter area of 3 units and a multiplier parameter of 4 the variance of the mismatch of the saturation current is $\frac{\sigma_{\Delta g_m}}{g_m} = \frac{\sigma_{\Delta I_C}}{I_C} = \frac{\sigma_{\Delta I_S}}{I_S} = 0.7\,\%$.

For the low frequency A_{CM-DM} (4.32) gain

$$\sigma_{A_{CM-DM}} \simeq \frac{R_C}{(R_E+2R_{olb})}\sqrt{\left(\frac{1}{1+g_m R_E}\left(\frac{\sigma_{\Delta g_m}}{g_m}\right)\right)^2+\left(\frac{\sigma_{\Delta R_E}}{R_E}\right)^2+\left(\frac{\sigma_{\Delta R_C}}{R_C}\right)^2} = \frac{R_C}{(R_E+2R_{olb})}\sqrt{\left(\frac{1}{1+g_m R_E}\left(\frac{\sigma_{\Delta I_S}}{I_S}\right)\right)^2+\left(\frac{\sigma_{\Delta R_E}}{R_E}\right)^2+\left(\frac{\sigma_{\Delta R_C}}{R_C}\right)^2} = \pm 30\cdot 10^{-6}\ rms \quad (4.36)$$

And for low frequency $A_{DM\text{-}CM}$ (4.34) gain,

$$\sigma_{A_{DM-CM}} \simeq \frac{1}{4}\sqrt{\left(\frac{R_C}{R_E+2R_{olbE}}\right)^2\left(\left(\frac{1}{g_m R_E}\frac{\sigma_{\Delta g_m}}{g_m}\right)^2+\left(\frac{\sigma_{\Delta R_E}}{R_E}\right)^2\right)+\left(\frac{R_C}{R_E}\frac{\sigma_{\Delta R_C}}{R_C}\right)^2} = \frac{1}{4}\sqrt{\left(\frac{R_C}{R_E+2R_{olbE}}\right)^2\left(\left(\frac{1}{g_m R_E}\left(\frac{\sigma_{\Delta I_S}}{I_S}\right)\right)^2+\left(\frac{\sigma_{\Delta R_E}}{R_E}\right)^2\right)+\left(\frac{R_C}{R_E}\frac{\sigma_{\Delta R_C}}{R_C}\right)^2} = \pm 2.5\cdot 10^{-3}\ rms \quad (4.37)$$

In order to compare simulation results with previous calculations only the effect of device matching variations at low frequency has to be taken into account. Monte Carlo simulations with only mismatch variations (100 runs) have been performed, results are depicted in Figure 4-17.

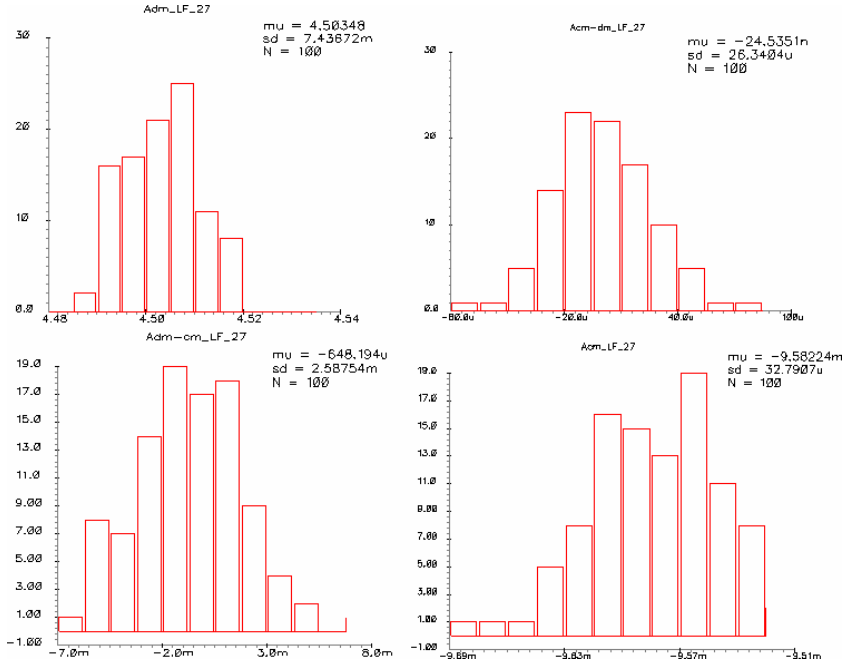

Figure 4-17. Histograms of the low frequency gains of the preamplifier. Mismatch variations in Monte Carlo simulations (100 runs).

For A_{DM} and A_{CM} gains, standard deviation is a small fraction of the mean gain (about 0.3 %). As expected the mean values for $A_{CM\text{-}DM}$ and for $A_{DM\text{-}CM}$ are about zero. $\sigma_{A_{CM-DM}}$ is about $26\cdot 10^{-6}$ and $\sigma_{A_{CM-DM}}$ is about $2.6\cdot 10^{-3}$, close to the approximated values given in (4.36) and in (4.37). Results are summarized in table Table 4-2.

	Calculations		Monte Carlo	
	Mean	Std. Dev.	Mean	Std. Dev.
A_{DM}	4.6	-	4.5	$7 \cdot 10^{-3}$
A_{CM-DM}	0	$30 \cdot 10^{-6}$	≈0	$26 \cdot 10^{-6}$
A_{DM-CM}	0	$2.5 \cdot 10^{-3}$	≈0	$2.6 \cdot 10^{-3}$
A_{CM}	$-9 \cdot 10^{-3}$	-	$-9.6 \cdot 10^{-3}$	$33 \cdot 10^{-6}$
CMRR	∞	104 dB	∞	105 dB

Table 4-2. Statistical parameters of preamplifier gain for first order approximation and Monte Carlo simulations of matching variations.

Figure 4-18 shows the histograms of the low frequency gains corresponding to Monte Carlo simulations of both matching and process variations. The effect of process variations on A_{CM-DM} and A_{DM-CM} is negligible as these gains are determined by the matching variations. However for A_{DM} and A_{CM} there is a significant increase in standard in deviation but also a change in distribution shape, since process variations are modeled through a uniform distribution.

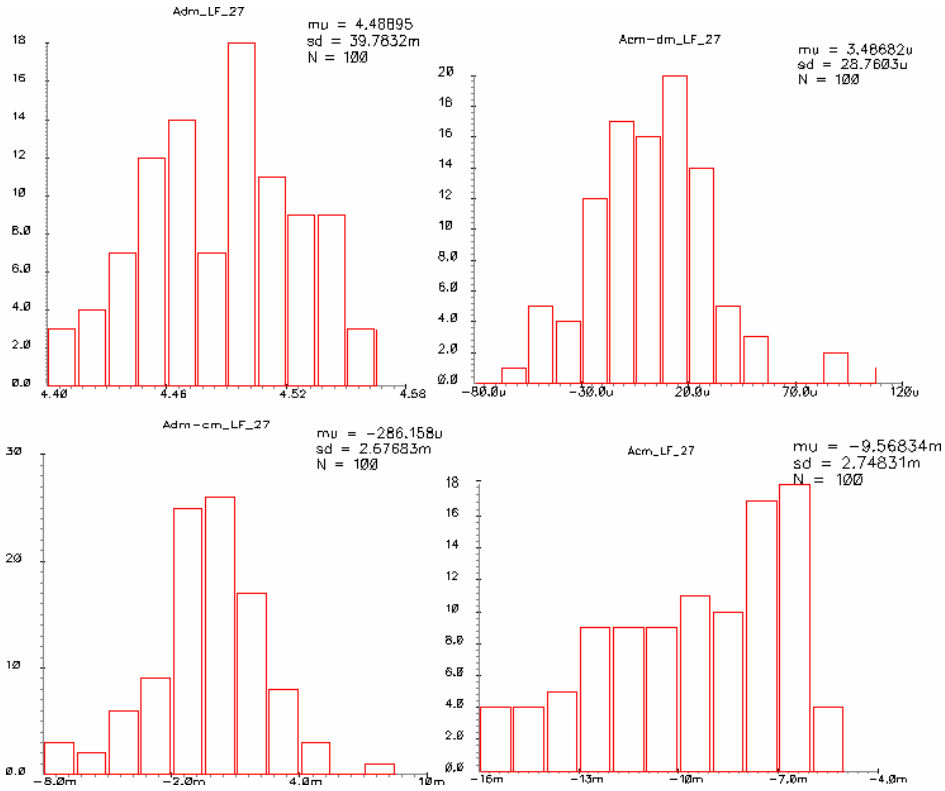

Figure 4-18. Histograms of the low frequency gains. Mismatch and process variations in Monte Carlo simulations (100 runs).

Now we will estimate analytically the tolerance we can expect on the gain due to process variations. Standard deviation of differential mode gain is a function of the standard deviation of the resistor and transconductance values, by the Theory of Error propagation,

$$\sigma^2_{A_{DM}(R_C,R_E,g_m)} = \left(\frac{\partial A_{DM}}{\partial R_C}\right)^2 \sigma^2_{R_C} + \left(\frac{\partial A_{DM}}{\partial R_E}\right)^2 \sigma^2_{R_E} + \left(\frac{\partial A_{DM}}{\partial g_m}\right)^2 \sigma^2_{g_m} + 2\,\mathrm{cov}(R_C,R_E)\left(\frac{\partial A_{DM}}{\partial R_C}\right)\left(\frac{\partial A_{DM}}{\partial R_E}\right) +$$
$$+ 2\,\mathrm{cov}(R_C,g_m)\left(\frac{\partial A_{DM}}{\partial R_C}\right)\left(\frac{\partial A_{DM}}{\partial g_m}\right) + 2\,\mathrm{cov}(R_E,g_m)\left(\frac{\partial A_{DM}}{\partial R_E}\right)\left(\frac{\partial A_{DM}}{\partial g_m}\right) \tag{4.38}$$

Using (4.31),

$$\sigma^2_{A_{DM}(R_C,R_E,g_m)} = \left(\frac{g_m}{1+g_mR_E}\right)^2\left(R_C\frac{\sigma_{R_C}}{R_C}\right)^2 + \left(-\frac{g_m^2R_C}{(1+g_mR_E)^2}\right)^2\left(R_E\frac{\sigma_{R_E}}{R_E}\right)^2 + \left(\frac{R_C}{(1+g_mR_E)^2}\right)^2\sigma^2_{g_m} +$$
$$+2\left(\frac{g_m}{1+g_mR_E}\right)\left(-\frac{g_m^2R_C}{(1+g_mR_E)^2}\right)\mathrm{cov}(R_C,R_E) + 2\left(\frac{g_m}{1+g_mR_E}\right)\left(\frac{R_C}{(1+g_mR_E)^2}\right)\mathrm{cov}(R_C,g_m) + \quad (4.39)$$
$$+2\left(-\frac{g_m^2R_C}{(1+g_mR_E)^2}\right)\left(\frac{R_C}{(1+g_mR_E)^2}\right)\mathrm{cov}(R_E,g_m)$$

R_C and R_E are same type of resistor (same poly-silicon type), therefore process variations will affect both in same way; i.e. R_C and R_E are fully correlated random variables. The transconductance g_m only depends on the biasing collector current and this is determined by the biasing current source I_b. The current source derives the current using poly resistors for the current master (see section 4.5.1); therefore g_m and resistor values will also be correlated. Figure 4-19 shows the correlation between bias collector current and poly resistance process variations, the correlation coefficient is almost the unity, hence g_m and R_E and R_C will be considered also fully correlated.

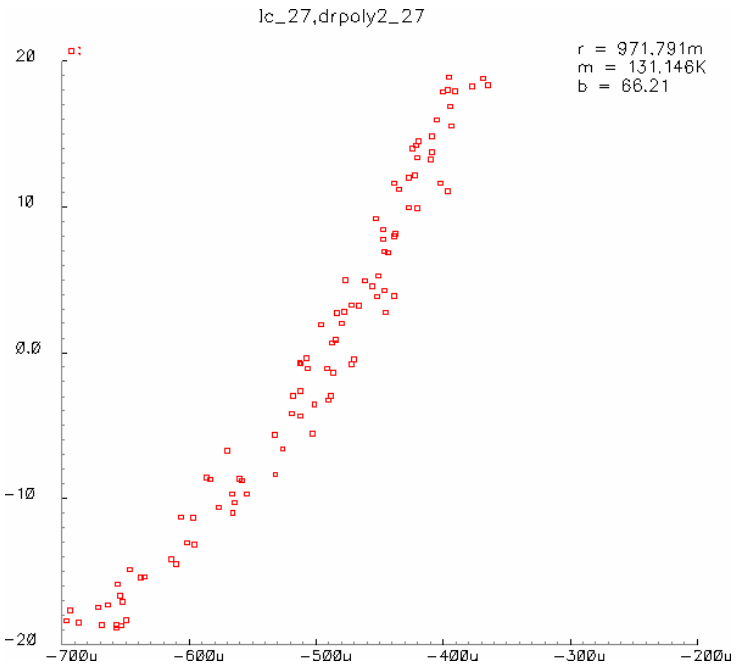

Figure 4-19. Correlation between bias collector current and poly resistance process variations.

If X and Y are fully correlated real-valued random variables,

$$\mathrm{cov}(X,Y) = \sigma_X\sigma_Y \quad (4.40)$$

Using(4.40), and considering $\frac{\sigma_{R_C}}{R_C} \equiv \frac{\sigma_{R_E}}{R_E}$,

$$\sigma^2_{A_{DM}(R_C,R_E,g_m)} = \left(\frac{g_m}{1+g_mR_E}\right)^2\left(R_C\frac{\sigma_R}{R}\right)^2 + \left(-\frac{g_m^2R_C}{(1+g_mR_E)^2}\right)^2\left(R_E\frac{\sigma_R}{R}\right)^2 + \left(\frac{R_C}{(1+g_mR_E)^2}\right)^2\sigma^2_{g_m} -$$

$$-2\left(\frac{g_m}{1+g_mR_E}\right)\left(\frac{g_m^2R_C}{(1+g_mR_E)^2}\right)\left(R_C\frac{\sigma_R}{R}\right)\left(R_E\frac{\sigma_R}{R}\right)+2\left(\frac{g_m}{1+g_mR_E}\right)\left(\frac{R_C}{(1+g_mR_E)^2}\right)\left(R_C\frac{\sigma_R}{R}\right)\sigma_{g_m} -$$

$$-2\left(\frac{g_m^2R_C}{(1+g_mR_E)^2}\right)\left(\frac{R_C}{(1+g_mR_E)^2}\right)\left(R_E\frac{\sigma_R}{R}\right)\sigma_{g_m} =$$

$$=\left(\left(\frac{g_mR_C}{1+g_mR_E}\right)^2+\left(\frac{g_m^2R_CR_E}{(1+g_mR_E)^2}\right)^2-2\left(\frac{g_m^3R_C^2R_E}{(1+g_mR_E)^3}\right)\right)\left(\frac{\sigma_R}{R}\right)^2+\left(\frac{R_C}{(1+g_mR_E)^2}\right)^2\sigma^2_{g_m}+$$

$$+2\sigma_{g_m}\frac{\sigma_R}{R}\frac{g_mR_C^2}{(1+g_mR_E)^3}\left(1-\frac{g_mR_E}{(1+g_mR_E)}\right)\simeq\Big|_{g_mR_E>>1}$$

$$\simeq\left(\left(\frac{R_C}{R_E}\right)^2+\left(\frac{R_C}{R_E}\right)^2-2\left(\frac{R_C^2}{R_E^2}\right)\right)\left(\frac{\sigma_R}{R}\right)^2+\left(\frac{R_C}{(1+g_mR_E)^2}\right)^2\sigma^2_{g_m}+2\sigma_{g_m}\frac{\sigma_R}{R}\frac{g_mR_C^2}{(1+g_mR_E)^3}(1-1)=$$

$$=\left(\frac{R_C}{(1+g_mR_E)^2}\right)^2\sigma^2_{g_m}$$

(4.41)

Expression (4.41) reflects how emitter degeneration helps to minimize the effect of process variations in differential gain, through the cancellation of collector and emitter resistance variations. The transconductance variance $\sigma^2_{g_m}$ related to process variations can be estimated through the dependence on collector bias current: $\sigma_{g_m} = \frac{1}{V_T}\sigma_{I_C}$ and then,

$$\frac{\sigma_{g_m}}{g_m} = \frac{\sigma_{I_C}}{I_C} \qquad (4.42)$$

As said above, collector bias current process variations are fully correlated with resistor process variations, thus $\frac{\sigma_{g_m}}{g_m} = \frac{\sigma_{I_C}}{I_C} = \frac{\sigma_R}{R}$. According to [73] resistors integrated with the second level of polysilicon have minimum value (lower limit of production acceptance) of 55 Ω/□, a maximum value of 80 Ω/□ and a typical value of 67 Ω/□, assuming a uniform distribution:

$$\frac{\sigma_{g_m}}{g_m} = \frac{\sigma_{I_C}}{I_C} = \frac{\sigma_R}{R} = \frac{\frac{R_{MAX}-R_{MIN}}{\sqrt{12}}}{R_{TYP}} = 10\,\% \qquad (4.43)$$

Using (4.41) and (4.43) the estimation for the gain variation due to process variations is $\sigma_{A_{DM}(R_C,R_E,g_m)} \simeq \left(\frac{R_C}{(1+g_mR_E)^2}\right)\sigma_{g_m} \simeq 0.05$. Then the expected tolerance of the preamplifier gain for a large production is $\frac{\sigma_{A_{DM}}}{A_{DM}} \simeq 1\,\%$, in agreement with results of simulations (Figure 4-18).

4.2.1.5 Gain temperature coefficient

The temperature dependence $\frac{\partial A_{DM}}{\partial T}$ of the differential mode gain A_{DM} is,

$$\frac{\partial A_{DM}}{\partial T} = \frac{\partial A_{DM}}{\partial R_C}\frac{\partial R_C}{\partial T} + \frac{\partial A_{DM}}{\partial R_E}\frac{\partial R_E}{\partial T} + \frac{\partial A_{DM}}{\partial g_m}\frac{\partial g_m}{\partial T} \tag{4.44}$$

Using (4.31),

$$\begin{aligned} \frac{\partial A_{DM}}{\partial R_C} &= \frac{g_m}{1+g_m R_E} \simeq \Big|_{g_m R_E \gg 1} \frac{1}{R_E} \\ \frac{\partial A_{DM}}{\partial R_E} &= \frac{-g_m^2 R_C}{\left(1+g_m R_E\right)^2} \simeq \Big|_{g_m R_E \gg 1} -\frac{R_C}{R_E^2} \\ \frac{\partial A_{DM}}{\partial g_m} &= \frac{R_C}{\left(1+g_m R_E\right)^2} \simeq \Big|_{g_m R_E \gg 1} \frac{R_C}{g_m^2 R_E^2} \end{aligned} \tag{4.45}$$

The effective temperature coefficient for the poly 2 resistors is, according to [73],

$$TC_{POLY2} \equiv \frac{1}{R_{T0}}\frac{R_T - R_{T0}}{T - T0} = -0,3\cdot 10^{-3}\left[\frac{1}{\Omega}\right] \tag{4.46}$$

And taking the effective temperature coefficient as nominal temperature coefficient,

$$\begin{aligned} \frac{\partial R_C}{\partial T} &= R_C TC_{POLY2} \\ \frac{\partial R_E}{\partial T} &= R_E TC_{POLY2} \end{aligned} \tag{4.47}$$

The temperature coefficient for the transconductance is,

$$\frac{\partial g_m}{\partial T} = \frac{\partial g_m}{\partial I_C}\frac{\partial I_C}{\partial T} + \frac{\partial g_m}{\partial V_T}\frac{\partial V_T}{\partial T} = \frac{1}{V_T}\frac{\partial I_C}{\partial T} - \frac{I_C}{V_T^2}\frac{k}{q} \tag{4.48}$$

The using previous expressions,

$$\begin{aligned} \frac{\partial A_{DM}}{\partial T} &\simeq \frac{1}{R_E} R_C TC_{POLY2} - \frac{R_C}{R_E^2} R_E TC_{POLY2} + \frac{R_C}{g_m^2 R_E^2}\left(\frac{1}{V_T}\frac{\partial I_C}{\partial T} - \frac{I_C}{V_T^2}\frac{k}{q}\right) \simeq \\ &\simeq \frac{R_C}{g_m^2 R_E^2}\left(\frac{1}{V_T}\frac{\partial I_C}{\partial T} - \frac{I_C}{V_T^2}\frac{k}{q}\right) \end{aligned} \tag{4.49}$$

The temperature dependence of gain on R_C and on R_E cancels out, thus this stage is independent on resistor temperature variations thanks to the emitter degeneration. The current source is a based on band-gap reference, being the $\frac{\partial I_C}{\partial T} \simeq 200\frac{nA}{K}$. V_T is 26 mV at 300 K, the collector current I_C is $I_{bias}/2$=500 μA, q is the electron charge $q=1.6\cdot 10^{-19}$ C and $k=1.38\cdot 10^{-23}$ J/K is the Boltzmann's constant. Then, $\frac{\partial A_{DM}}{\partial T} \simeq -1,6\cdot 10^{-3}\frac{1}{K}$ and the differential gain temperature coefficient,

$$TC_{A_{DM}} \equiv \frac{1}{A_{DM}}\frac{\partial A_{DM}}{\partial T} \simeq -350\,\frac{ppm}{K} \tag{4.50}$$

According to Spectre simulations the $TC_{A_{DM}} \simeq -270\,\frac{ppm}{K}$

4.2.1.6 Layout

Figure 4-20 shows the layout of the preamplifier, cell size is 200 μm x 260 μm.

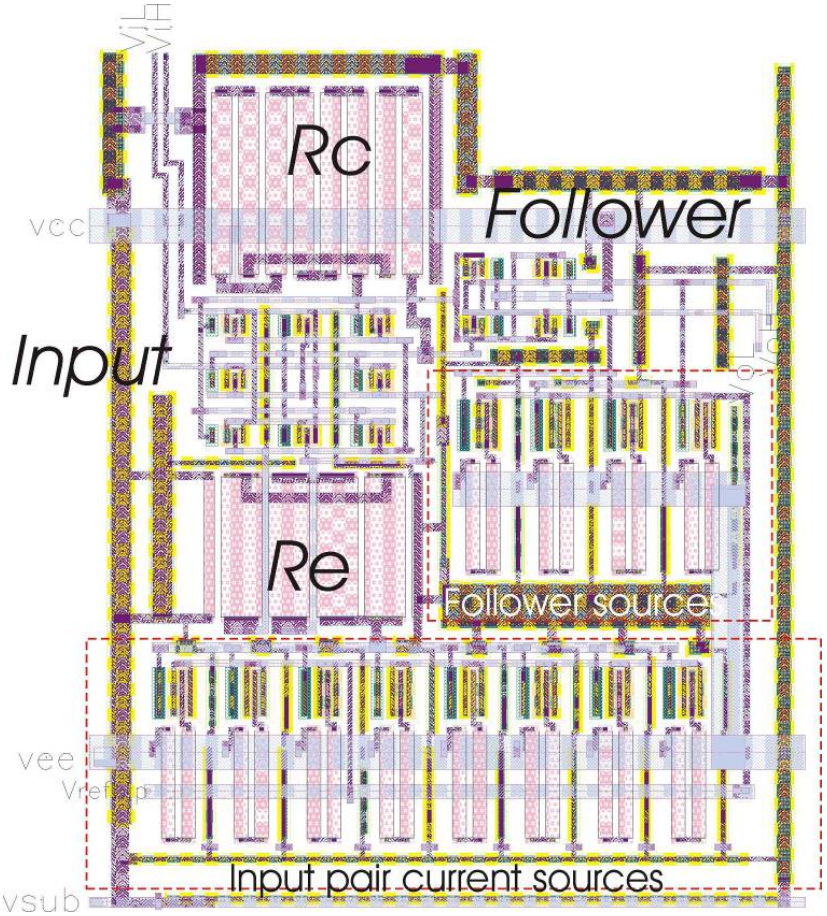

Figure 4-20. Layout of the preamplifier

In previous section it has been stated that crucial characteristics such input common-mode to output differential-mode rejection, power supply rejection and also offset are strongly dependent on device mismatch in fully differential circuits like this preamplifier. The estimation and the simulation of device mismatch effects that have been presented so far only account for local variations, thus improper layout could worsen the presented results: for example placing two matched components at long distance will introduce the effect of parameter gradients across the wafer. Therefore it is very important to apply proper layout techniques ([68] and [133]) to improve device matching:

- Transistor pair Q_1-Q_2 is split in 4+4 elementary transistors and are matched through the common centroid layout technique.
- Layout of emitter matched resistors R_{E1}-R_{E2} is an interleaved layout with dummy resistors at the sides and with matched number of contacts.
- Same for collector matched resistors R_{C1}-R_{c2}.
- Output followers Q_3-Q_4 are doubled and placed with common-centroid.
- Current source units are placed with same orientation.

An extensive use of substrate contacts is adopted to minimize the substrate noise, this is a technique employed in general in this ASIC.

4.2.2 Integrator

The design of the integrator block is shown in Figure 4-21. The input stage, which is also a bipolar pair with emitter degeneration (R_E), acts as a transconductor converting the input voltage to a differential current. This current is integrated by a fully-differential integrator made with an OpAmp with capacitive feedback (C_1-C_2). For fast pulses almost all the differential current of the input pair flows through the feedback capacitors. The CMOS switches placed in parallel with these capacitors perform the reset and the ones connected to the input are intended to pull these nodes to zero during the reset phase. The integration time constant (τ_i) is given by $\tau_i = C \cdot R_E$.

The OpAmp is a fully balanced amplifier (FDOA), having two stages and continuous common mode feedback (CMFB) circuit. The unity gain frequency of the OpAmp causes a pole in the integrator response. To fulfill the system bandwidth requirements the gain bandwidth product (GBW) of the OpAmp must be higher than 100MHz. The total current consumption of the stage is 2.5 mA.

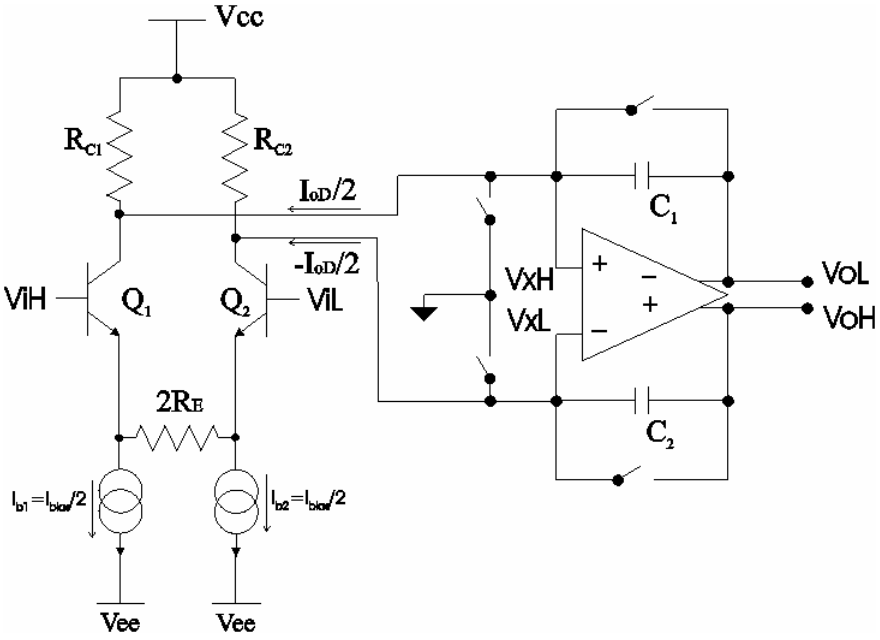

Figure 4-21. Schematics of the integrator block.

4.2.2.1 Input stage (transconductor)

The input stage provides high input impedance and acts as a differential transconductor, converting an input differential voltage into a differential current I_{oD} that will be integrated in the FDOA with capacitive feedback. It is a differential pair with emitter degeneration. The topology of emitter degeneration is different from the preamplifier one, improving gain matching, as emitter resistor is a single resistor there is no mismatch term related to this and the matching of the current sources does not affect the differential-mode half circuit in a first approximation as will be shown later (source impedance is in parallel with R_E and current mismatch will affect offset but not parasitic gains). Another advantage of this configuration is its better input CM signal range (see Appendix B). However, this configuration worsens signal to noise ratio and for this reason is not adopted in the preamplifier stage.

4.2.2.1.1 Large signal analysis

From KVL around the input loop,

$$V_{iH} - V_{BE_1} - I_{R_E} 2R_E + V_{BE_2} - V_{iL} = 0 \qquad (4.51)$$

From the KCL (Kirchoff's Current Law) inthe emitter node of Q_1 and Q_2 respectively, and approximating emitter current by collector current,

$$\begin{aligned} I_{C_1} &= I_{R_E} + I_{b_1} \\ I_{C_2} + I_{R_E} &= I_{b_2} \end{aligned} \tag{4.52}$$

According to (4.52) and since with perfect current matching $I_{b1}=I_{b2}=I_{bias}/2$,

$$I_{R_E} = \frac{I_{C_1} - I_{C_2}}{2} \tag{4.53}$$

Using expression (4.51) and expression (4.53),

$$V_{iH} - V_{BE_1} - I_{C_1}R_E + I_{C_2}R_E + V_{BE_2} - V_{iL} = 0 \tag{4.54}$$

With $V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right)$ and $V_{BE_1} - V_{BE_2} = V_T \ln\left(\frac{I_{C_1}}{I_{C_2}}\right)$. If the load impedance is much smaller than R_C, $I_{oD} \approx I_{C1} - I_{C2}$, and $I_{oD} \approx (I_{C1}+I_{C2})/2$, then expression (4.54) yields,

$$V_{iD} = V_T \ln\left(\frac{1 + \frac{I_{oD}/2}{I_{oC}}}{1 - \frac{I_{oD}/2}{I_{oC}}}\right) + I_{oD}R_E \tag{4.55}$$

Which is equivalent to expression (4.8) of the preamplifier, with the difference that in the preamplifier case it was needed to assume $R_{E1}=R_{E2}=R_E$, i.e. perfect matching of emitter resistors whereas in this topology there is only one emitter resistor and no mismatch will be introduced for this reason. As said before, matching will be an issue for the bias currents I_{b1} and I_{b2}.

Using Taylor series for $\ln\left(\frac{1+x}{1-x}\right) = 2\left[x + \frac{x^3}{3!} + \ldots\right]$,

$$V_{iD} = I_{oD}R_E + 2V_T \frac{I_{oD}/2}{I_{oC}} + 2V_T \frac{\left(\frac{I_{oD}/2}{I_{oC}}\right)^3}{3!} + \ldots \tag{4.56}$$

If the 3rd and superior order terms are omitted and with the transconductance g_m of the transistors $g_m = I_{oC}/V_T$, the differential output current follows an approximate linear relationship with the input differential voltage

$$I_{oD} \simeq \frac{g_m}{(1 + g_m R_E)} V_{iD} \tag{4.57}$$

The linearity error is given by the 3rd and superior order terms of the Taylor series, the non-linear terms of (4.56) are negligible if $x = \frac{\frac{1}{2}\frac{g_m}{(1+g_m R_E)} V_{iD}}{I_{oC}} \ll 1$, thus the linear operation range for V_{iD} is

$$V_{iD} \ll \frac{1}{2}\frac{(1 + g_m R_E)}{g_m} I_{oC} \tag{4.58}$$

The common mode output current I_{oC} is $I_{bias}/2$ = 360 µA, g_m= 13 mS and R_E = 1 kΩ, therefore V_{iD} << 500 mV. For the maximum input signal is $V_{iDmax} \cdot A_{DMpreamp} = I_{pkmax} \cdot R_S \cdot A_{DMpreamp}$ = 175 mV, the 3rd order term in (4.9) is about the 0.1% of the first order term.

Figure 4-22 shows input voltage and output current for several typical inputs. In order to analyze non-linearity, the linearity error is calculated as the deviation from a perfect linear response. Signal range of ±200 mV is 400 nA for an I_{oDpeak} of about 200 µA, i.e. the maximum linearity error is about 0.02 % of signal range.

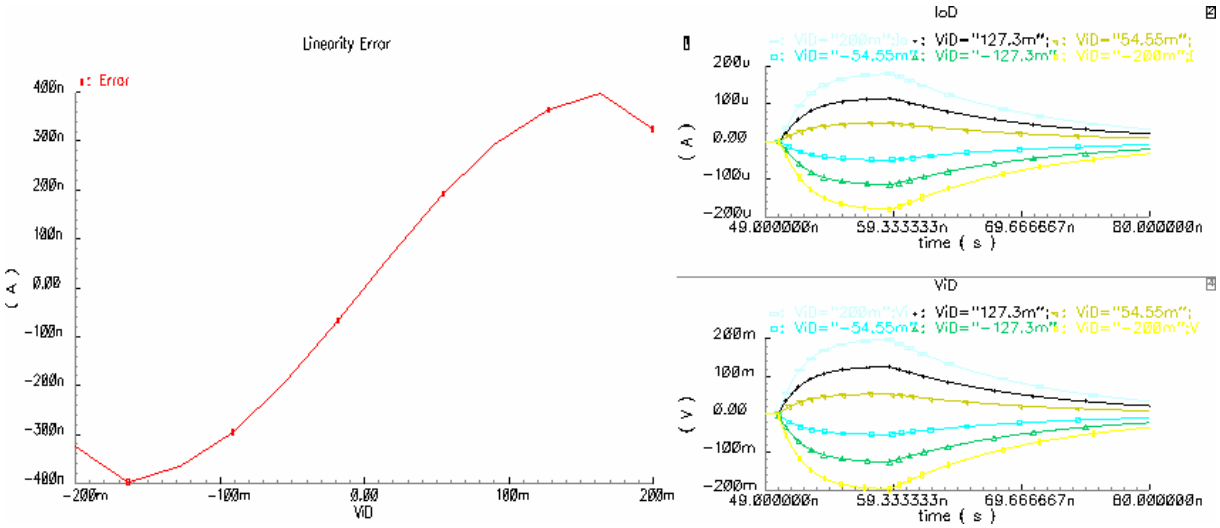

Figure 4-22. Linearity error (left) for several typical input signals (right bottom). Output current is also shown (right top).

4.2.2.1.2 Small signal gains

As said before, the unbalancing on differential circuits introduces "correlations" between differential-mode and common-mode signals, thus they are needed four gains or transconductances to define the transfer function of this stage,

$$\begin{aligned} i_{oD} &= G_{DM} v_{iD} + G_{CM-DM} v_{iC} \\ i_{oC} &= G_{DM-CM} v_{iD} + G_{CM} v_{iC} \end{aligned} \qquad (4.59)$$

To derive this gains same methodology used in preamplifier analysis will be adopted. First, the common-mode and differential-mode half circuits have to be deduced. Figure 4-23 shows the transconductor with the resistance $2R_E$ divided into 2 identical resistors of value R_E and connected at the central point P.

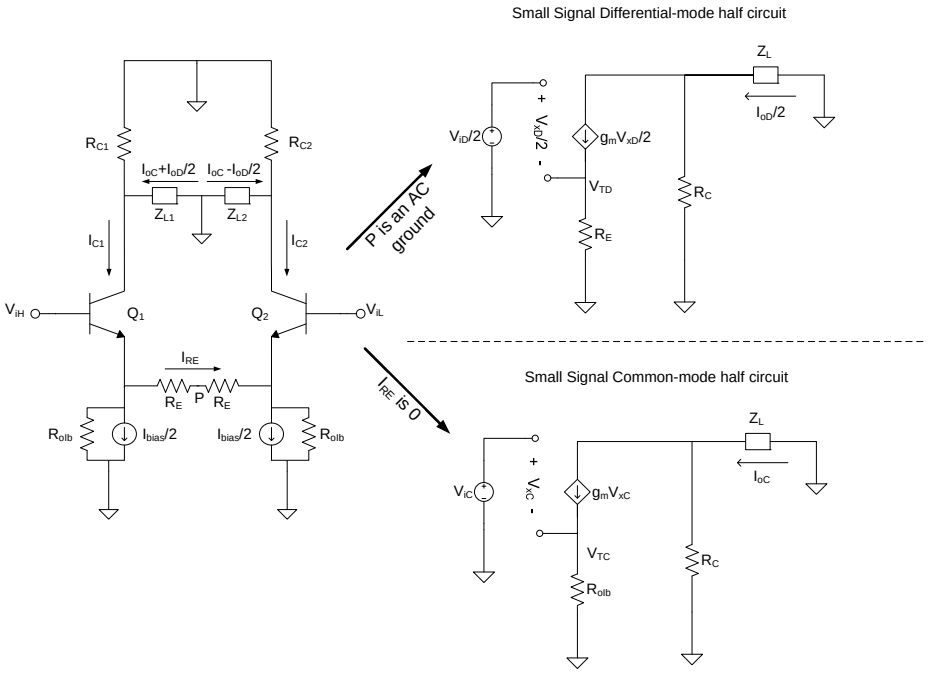

Figure 4-23. Differential-mode and common-mode half circuits.

For pure differential-mode inputs, same magnitude but opposite sign, if V_{iH} changes in ΔV_i, then V_{iL} changes in $-\Delta V_i$ (same amount). On the other hand, base emitter voltages will change by ΔV_{BE1} and ΔV_{BE2}. The output currents therefore change by $g_m\Delta V_{BE1}$ and by $g_m\Delta V_{BE2}$. According to (4.52) and considering the current source impedance $R_{OIb} >> R_E$, $I_{C1}+I_{C2} = I_{bias}$, with I_{bias} constant $g_m\Delta V_{BE1} + g_m\Delta V_{BE2}=0$, then $\Delta V_{BE1}=-\Delta V_{BE2}$. We also know that $V_{E1P} = -V_{E2P}$ and therefore $\Delta V_{E1P} = -\Delta V_{E2P}$. The voltage at point P is $V_P = V_{iH} -V_{BE1}-V_{E1P}= V_{iL} -V_{BE2}-V_{E2P}$. The common mode values get simplified and $\Delta V_i-\Delta V_{BE1}-\Delta V_{E1P} = -\Delta V_i -\Delta V_{BE2}-\Delta V_{E2P}$, using $\Delta V_{BE1} = -\Delta V_{BE2}$ and $\Delta V_{E1P} = -\Delta V_{E2P}$, we have $\Delta V_i = \Delta V_{BE1}+\Delta V_{E1P}$. Since $V_P = V_{iH} -V_{BE1}-V_{E1P} = (V_{iCM}+\Delta V_i) - (V_{BE1CM}+\Delta V_{BE1}) - (V_{E1PCM}+\Delta V_{E1P}) = V_{iCM}-V_{BE1CM}-V_{E1PCM}$, therefore V_P depends on the common-mode values, it is constant and it is a virtual AC ground for differential mode signals. The differential pair can be divided in two differential-mode half circuits as shown in Figure 4-23 for pure differential inputs, again we consider $R_{OIb}>>R_E$ and R_{OIb} since is in parallel with R_E when P is considered a small-signal virtual ground. The small-signal resistance r_π is omitted for simplicity (output resistance of preamplifier is much smaller). A load impedance Z_L is included for analysis purposes.

For pure common-mode inputs, same magnitude and same sign, if V_{iH} changes in ΔV_i, then V_{iL} changes in ΔV_i. On the other hand, base emitter voltages will change by ΔV_{BE1} and ΔV_{BE2}. The output currents therefore change by $g_m\Delta V_{BE1}$ and by $g_m\Delta V_{BE2}$. According to (4.52) and considering the current source impedance $R_{OIb}>>R_E$, $I_{C1}+I_{C2}=I_{bias}$, with I_{bias} constant $g_m\Delta V_{BE1} + g_m\Delta V_{BE2} = 0$, then $\Delta V_{BE1}=-\Delta V_{BE2}$. We also know that $V_{E1P}=-V_{E2P}$ and therefore $\Delta V_{E1P} = -\Delta V_{E2P}$. The voltage at point P is $V_P = V_{iH} -V_{BE1}-V_{E1P} = V_{iL} -V_{BE2}-V_{E2P}$. For common mode change, $\Delta V_{BE1}-\Delta V_{E1P} = \Delta V_{BE2}-\Delta V_{E2P}$ using $\Delta V_{BE1} = -\Delta V_{BE2}$ and $\Delta V_{E1P} = -\Delta V_{E2P}$, we have $\Delta V_{BE1} = -\Delta V_{E1P}$. For infinite source impedance $I_{RE} = g_m\Delta V_{BE1}$, therefore $\Delta V_{E1P} = g_m\Delta V_{BE1}R_E$. The only solution for $\Delta V_{BE1} = -\Delta V_{E1P}$ and $\Delta V_{E1P} = g_m\Delta V_{BE1}R_E$, is $\Delta V_{BE1} = \Delta V_{E1P} = 0$. This means that I_{RE} is zero, so that no current flows through the emitter resistor and circuit can be divided as in Figure 4-23. This also means that a change in input common-mode has no impact on the circuit, but this is only true for infinity current source impedance. Anyhow, even for finite source impedances, the circuit is divided in two identical halves, and because each half is driven by the same voltage (for pure common-mode signals) emitter voltages must be equal and no current will flow through the emitter resistor.

So far perfectly balanced circuits have been considered, now device mismatch will be considered in order to estimate the transconductance parameters of the expression (4.59). As in preamplifier analysis, two half circuits coupled through the mismatch generators will be used, they are shown in Figure 4-24.

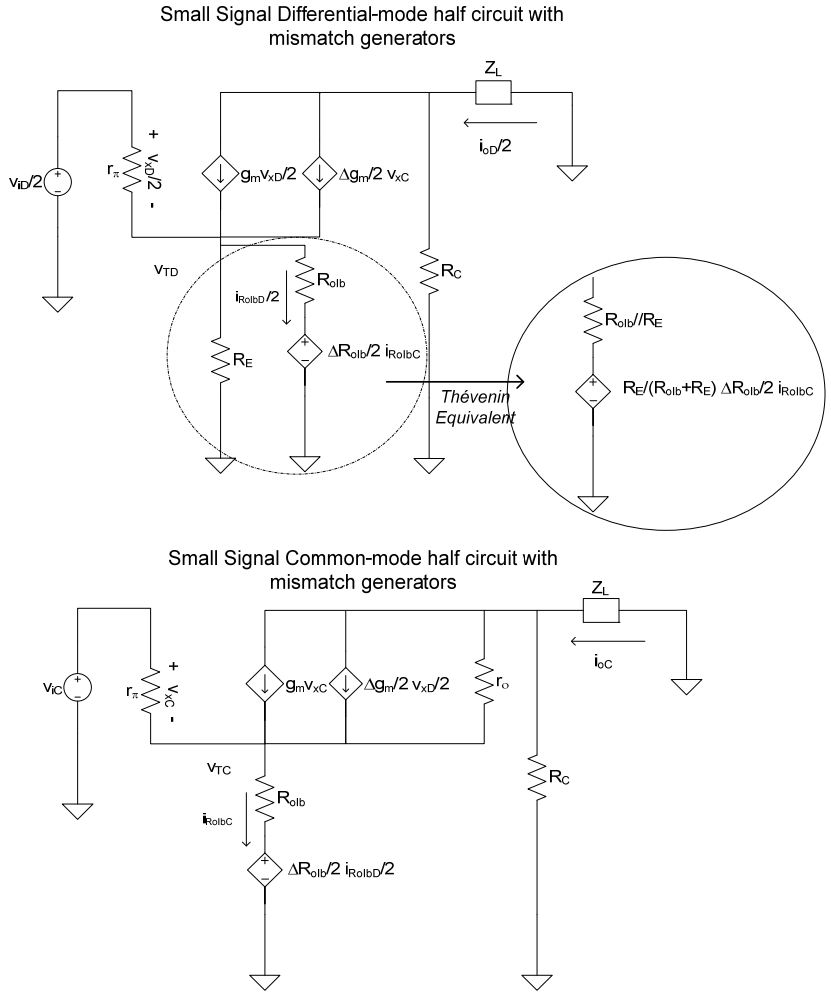

Figure 4-24. Differential-mode (top) and common-mode (bottom) half circuits for Integrator input stage with mismatch generators.

The emitter resistor R_E has no mismatch term since it is virtual resistor, a half of the unique emitter resistor. As said above, in this topology matching between emitter resistors is replaced by matching between bias current sources I_{b1} and I_{b2}. Mismatch between sources has two effects: mismatch in collector currents and mismatch in current source output resistances (R_{oIb}). The current unbalancing does not depend neither on input common-mode nor on differential-mode voltages and, therefore, it does not contribute to "gain" terms of (4.59). As it is a fixed term it will contribute to the offset, it will be studied later. Regarding mismatch in R_{oIb}, using the Thévenin theorem we see that the mismatch generator for current source output resistance in differential-mode half circuit is multiplied by a factor $\frac{R_E}{R_E + R_{oIb}} \simeq 2 \cdot 10^{-3}$.

The effect of mismatch on collector resistor is not taken into account since we are interested in the current output, and the output impedance r_o of Q_1-Q_2 is much larger than R_C. Since we are interested in output currents, not in output voltages, the mismatch collector resistor is not relevant at first approximation; it will have some minor effect because the output resistance of the transistors of the differential pair is not infinity but it is of the order of MΩ thanks to emitter degeneration. The output

impedance r_o of Q_1-Q_2 is included in common-mode half circuit because the common-mode current flowing through it is comparable to the common-mode current flowing through the emitter resistor, which includes R_{oIb}.

As said before, if the mismatches are small, the controlling voltages of the mismatch generators can be computed from a circuit without mismatch. This simplification yields to approximate results, but greatly simplifies calculations decoupling both half circuits. In addition the mismatch generators in each half circuit become independent. They do depend on a parameter which is external to the half circuit (depend on the other half circuit), and superposition can be applied.

For the differential-mode circuit (Figure 4-24) output current depends on differential input (v_{iD}) and transistor (Δg_m) and current source (ΔR_{oIb}) matching generators, by superposition

$$\frac{i_{oD}}{2} = \left.\frac{i_{oD}}{2}\right|_{v_{iD}} + \left.\frac{i_{oD}}{2}\right|_{\Delta g_m} + \left.\frac{i_{oD}}{2}\right|_{\Delta R_{olb}} \tag{4.60}$$

For the component depending on the differential input (v_{iD}):

$$\left.\frac{i_{oD}}{2}\right|_{v_{iD}} = \frac{R_C}{R_C + Z_L}\frac{g_m}{1 + g_m R_E + \dfrac{R_E}{r_\pi}}\frac{v_{iD}}{2} \simeq\Big|_{g_m \gg \frac{1}{r_\pi}} \frac{R_C}{R_C + Z_L}\frac{g_m}{1 + g_m R_E}\frac{v_{iD}}{2} \tag{4.61}$$

And the controlling signal of the transistor transconductance when differential-mode input is the only independent source in differential circuit is

$$\left.\frac{v_{xD}}{2}\right|_{v_{id}} = -\frac{1}{1 + g_m R_E + \dfrac{R_E}{r_\pi}}\frac{v_{id}}{2} \simeq\Big|_{g_m \gg \frac{1}{r_\pi}} -\frac{1}{1 + g_m R_E}\frac{v_{id}}{2} \tag{4.62}$$

As will be seen later, it is important to calculate the differential-mode current trough R_{oIb} when differential-mode input is the only independent source in differential circuit

$$\left.\frac{i_{RoIbD}}{2}\right|_{v_{iD}} = \frac{R_E}{R_{oIb} + R_E}\frac{\left.\dfrac{v_{iD}}{2} - \dfrac{v_{xD}}{2}\right|_{v_{iD}}}{R_E} \simeq\Big|_{R_{oIb} \gg R_E} \frac{g_m R_E}{R_{oIb}\left(1 + g_m R_E\right)}\frac{v_{id}}{2} \simeq\Big|_{g_m R_E \gg 1} \frac{1}{R_{oIb}}\frac{v_{id}}{2} \tag{4.63}$$

For the output current component that depends on transistor matching generator:

$$\left.\frac{i_{oD}}{2}\right|_{\Delta g_m} = \frac{R_C}{R_C + Z_L}\left(g_m \frac{v_{xD}}{2} + \frac{\Delta g_m}{2} v_{xC}\right) \tag{4.64}$$

Using KCL and KVL

$$\begin{aligned} \left.\frac{v_{xD}}{2}\right|_{\Delta g_m} &= -v_{TD}\big|_{\Delta g_m} \\ v_{TD}\big|_{\Delta g_m} &= \left(g_m \left.\frac{v_{xD}}{2}\right|_{\Delta g_m} + \frac{\Delta g_m}{2} v_{xC} + \left.\frac{v_{xD}}{2}\right|_{\Delta g_m} \frac{1}{r_\pi}\right) R_E \end{aligned} \tag{4.65}$$

We find the controlling signal of the transistor transconductance when transistor mismatch generator is the only independent source in differential circuit,

$$\left.\frac{v_{xD}}{2}\right|_{\Delta g_m} = -\frac{R_E}{1 + g_m R_E + \dfrac{R_E}{r_\pi}}\frac{\Delta g_m}{2} v_{xC} \simeq\Big|_{g_m \gg \frac{1}{r_\pi}} -\frac{R_E}{1 + g_m R_E}\frac{\Delta g_m}{2} v_{xC} \tag{4.66}$$

Using (4.66) in (4.64)

$$\left.\frac{i_{oD}}{2}\right|_{\Delta g_m} \simeq \frac{R_C}{R_C+Z_L}\left(-\frac{g_m R_E}{1+g_m R_E}\frac{\Delta g_m}{2}v_{xC}+\frac{\Delta g_m}{2}v_{xC}\right)\simeq \frac{R_C}{R_C+Z_L}\frac{1}{1+g_m R_E}\frac{\Delta g_m}{2}v_{xC} \quad (4.67)$$

For current source matching generator (ΔR_{oIb}):

$$\left.\frac{i_{oD}}{2}\right|_{\Delta R_{olb}} \simeq \frac{R_C}{R_C+Z_L}\frac{g_m}{1+g_m R_E}\frac{R_E}{R_E+R_{olb}}\frac{\Delta R_{olb}}{2}i_{RoIbC} \simeq\Big|_{R_{olbC}\gg R_E} \frac{1}{2}\frac{R_C}{R_C+Z_L}\frac{g_m R_E}{1+g_m R_E}\frac{\Delta R_{olb}}{R_{olb}}i_{RoIbC} \quad (4.68)$$

Then the total differential mode output current is

$$\frac{i_{oD}}{2}=\left.\frac{i_{oD}}{2}\right|_{v_{iD}}+\left.\frac{i_{oD}}{2}\right|_{\Delta g_m}+\left.\frac{i_{oD}}{2}\right|_{\Delta R_{olb}}=\frac{R_C}{R_C+Z_L}\frac{1}{1+g_m R_E}\left(g_m\frac{v_{iD}}{2}+\frac{\Delta g_m}{2}v_{xC}+g_m R_E\frac{1}{R_{olb}}\frac{\Delta R_{olb}}{2}i_{RoIbC}\right) \quad (4.69)$$

For the common-mode half circuit (Figure 4-24) output current depends on common-mode input (v_{iC}) and transistor (Δg_m) and current source (ΔR_{oIb}) matching generators.

First, we calculate the component of the common-mode output current that depends only on v_{iC}. Following equations can be written using KCL and KVL from the common-mode half circuit (Figure 4-24),

$$\begin{aligned} i_{oC}\big|_{v_{iC}} &= \frac{R_C}{R_C+Z_L}\left(g_m v_{xC}\big|_{v_{iC}}-\frac{v_{TC}\big|_{v_{iC}}}{r_o}\right)\\ v_{iC} &= v_{xC}\big|_{v_{iC}}+v_{TC}\big|_{v_{iC}} \\ v_{TC}\big|_{v_{iC}} &= \left(g_m v_{xC}\big|_{v_{iC}}+\frac{v_{xC}\big|_{v_{iC}}}{r_\pi}\right)\left(R_{oIb}//r_o\right)\end{aligned} \quad (4.70)$$

it results,

$$v_{xC}\big|_{v_{iC}}=\frac{v_{iC}}{1+g_m r_o^{'}} \qquad where\ \ r_o^{'}=R_{oIb}//r_o \quad (4.71)$$

and the output current component depending on common-mode input (v_{iC})

$$i_{oC}\big|_{v_{iC}} \simeq \frac{R_C}{R_C+Z_L}\frac{r_o-r_o^{'}}{r_o r_o^{'}}v_{iC} \quad (4.72)$$

As will be seen later, it is important to calculate the common-mode current trough R_{oIb} when common-mode input is the only independent source in differential circuit

$$i_{RoIbC}\big|_{v_{iC}}=\frac{v_{iC}-v_{xC}\big|_{v_{iC}}}{R_{oIb}}=\frac{v_{iC}-\frac{v_{iC}}{1+g_m r_o^{'}}}{R_{oIb}}=\frac{g_m r_o^{'}}{R_{oIb}\left(1+g_m r_o^{'}\right)}v_{iC}\simeq\Big|_{g_m r_o^{'}\gg 1}\frac{1}{R_{oIb}}v_{iC} \quad (4.73)$$

Second, we calculate the component of the common-mode output current that depends only on transistor matching generator

$$i_{oC}\big|_{\Delta g_m}=\frac{R_C}{R_C+Z_L}\left(g_m v_{xC}\big|_{\Delta g_m}+\frac{\Delta g_m}{2}\frac{v_{xD}}{2}\right) \quad (4.74)$$

Using KCL and KVL

$$\begin{aligned} v_{xC}\big|_{\Delta g_m} &= -v_{TC}\big|_{\Delta g_m}\\ v_{TC}\big|_{\Delta g_m} &= \left(g_m v_{xC}\big|_{\Delta g_m}+\frac{\Delta g_m}{2}\frac{v_{xD}}{2}+v_{xC}\big|_{\Delta g_m}\frac{1}{r_\pi}\right)R_{oIb}\end{aligned} \quad (4.75)$$

We find the controlling signal of the transistor transconductance when transistor mismatch generator is the only independent source in common-mode half circuit,

$$v_{xC}\big|_{\Delta g_m} = -\frac{R_{oIb}}{1+g_m R_{oIb}+\dfrac{R_{oIb}}{r_\pi}}\frac{\Delta g_m}{2}\frac{v_{xD}}{2} \qquad (4.76)$$

Using (4.76) in (4.74),

$$i_{oC}\big|_{\Delta g_m} = \frac{R_C}{R_C+Z_L}\frac{1+\dfrac{R_{oIb}}{r_\pi}}{1+g_m R_{oIb}+\dfrac{R_{oIb}}{r_\pi}}\frac{\Delta g_m}{2}\frac{v_{xD}}{2} \simeq \Big|_{\substack{g_m \gg \frac{1}{r_\pi} \\ \frac{R_{oIb}}{r_\pi} \gg 1}} \frac{R_C}{R_C+Z_L}\frac{1}{g_m r_\pi}\frac{\Delta g_m}{2}\frac{v_{xD}}{2} \qquad (4.77)$$

and finally, for current source matching generator (ΔR_{oIb}):

$$i_{oC}\big|_{\Delta R_{oIb}} \simeq \frac{R_C}{R_C+Z_L}\frac{g_m}{1+g_m R_{oIb}}\frac{\Delta R_{oIb}}{2} i_{RoIbC} \simeq \Big|_{g_m R_{oIbC} \gg 1} \frac{R_C}{R_C+Z_L}\frac{1}{R_{oIb}}\frac{\Delta R_{oIb}}{2}\frac{i_{RoIbD}}{2} \qquad (4.78)$$

Then, the total common-mode output current is

$$i_{oC} = i_{oC}\big|_{v_{iC}} + \frac{i_{oD}}{2}\bigg|_{\Delta g_m} + \frac{i_{oD}}{2}\bigg|_{\Delta R_{oIb}} = \frac{R_C}{R_C+Z_L}\left(\frac{r_o - r_o'}{r_o r_o'} v_{iC} + \frac{1}{g_m r_\pi}\frac{\Delta g_m}{2}\frac{v_{xD}}{2} + \frac{1}{R_{oIb}}\frac{\Delta R_{oIb}}{2}\frac{i_{RoIbD}}{2}\right) \qquad (4.79)$$

Now, controlling signals of mismatch generators in differential-mode have to be deduce from the common-mode half circuit without mismatch generators (neglecting second order effects). For $v_{xC,}$

$$v_{xC} \approx v_{xC}\big|_{NO\ MISMATCH} \equiv v_{xC}\big|_{v_{iC}} = \frac{v_{iC}}{1+g_m r_o'} \qquad (4.80)$$

and for i_{RoIbC},

$$i_{RoIbC} \approx i_{RoIbC}\big|_{NO\ MISMATCH} \equiv i_{RoIbC}\big|_{v_{iC}} \simeq \frac{1}{R_{oIb}} v_{iC} \qquad (4.81)$$

In the same way, the expressions for the controlling signals of mismatch generators in common-mode are deduced from the differential-mode half circuit without mismatch generators. For $v_{xD}/2$,

$$\frac{V_{xD}}{2} \approx \frac{V_{xD}}{2}\bigg|_{NO\ MISMATCH} \equiv \frac{v_{xD}}{2}\bigg|_{v_{iD}} \simeq -\frac{1}{1+g_m R_E}\frac{v_{iD}}{2} \qquad (4.82)$$

and for $i_{RoIbD}/2$,

$$\frac{I_{RoIbD}}{2} \simeq \frac{I_{RoIbD}}{2}\bigg|_{NO\ MISMATCH} \equiv \frac{i_{RoIbD}}{2}\bigg|_{v_{iD}} \simeq \frac{1}{R_{oIb}}\frac{v_{iD}}{2} \qquad (4.83)$$

Substituting (4.80) and (4.81) in (4.69) we found the expression for the differential-mode output current,

$$\frac{i_{oD}}{2} = \frac{R_C}{R_C+Z_L}\frac{1}{1+g_m R_E}\left(g_m\frac{v_{iD}}{2} + \frac{\Delta g_m}{2}\frac{v_{iC}}{1+g_m r_o'} + \frac{g_m R_E}{R_{oIb}}\frac{\Delta R_{oIb}}{2}\frac{1}{R_{oIb}} v_{iC}\right)$$

In the same way, for the common-mode current,

$$i_{oC} = \frac{R_C}{R_C+Z_L}\left(\frac{r_o - r_o'}{r_o r_o'} v_{iC} - \frac{1}{g_m r_\pi}\frac{\Delta g_m}{2}\frac{1}{1+g_m R_E}\frac{v_{iD}}{2} + \frac{1}{R_{oIb}}\frac{\Delta R_{oIb}}{2}\frac{1}{R_{oIb}}\frac{v_{iD}}{2}\right) \qquad (4.84)$$

and the differential input to differential output transconductance

$$G_{DM} = \left.\frac{i_{oD}}{v_{iD}}\right|_{v_{iC}=0} = \frac{R_C}{R_C + Z_L}\frac{g_m}{1+g_m R_E} \quad (4.85)$$

Which is the same result obtained in the large signal analysis if we assume $R_C >> Z_L$. The common-mode input to differential output transconductance is

$$G_{CM-DM} = \left.\frac{i_{oD}}{v_{iC}}\right|_{v_{iD}=0} \simeq_{|g_m r_o' \gg 1} \frac{R_C}{R_C + Z_L}\frac{1}{1+g_m R_E}\left(\frac{1}{r_o'}\frac{\Delta g_m}{g_m} + \frac{g_m R_E}{R_{olb}}\frac{\Delta R_{olb}}{R_{olb}}\right) \quad (4.86)$$

The differential input to common-mode output transconductance is

$$G_{DM-CM} = \left.\frac{i_{oC}}{v_{iD}}\right|_{v_{iC}=0} \simeq \frac{R_C}{R_C + Z_L}\frac{1}{4}\left(-\frac{1}{(1+g_m R_E) r_\pi}\frac{\Delta g_m}{g_m} + \frac{1}{R_{olb}}\frac{\Delta R_{olb}}{R_{olb}}\right) \quad (4.87)$$

and the common-mode input to common-mode output transconductance is

$$G_{CM} = \left.\frac{i_{oC}}{v_{iC}}\right|_{v_{iD}=0} = \frac{R_C}{R_C + Z_L}\frac{r_o - r_o'}{r_o r_o'} \quad (4.88)$$

In order to have quantitative results the case $R_C >> Z_L$ will be considered. Some circuit parameters have to be estimated. Each current source of the transconductors is composed by 3 units in parallel, therefore the output resistance R_{olb} is about 500 kΩ (see section 4.5.1. Bias current). As said above, g_m is about 14 mS and R_E is 1 kΩ. To estimate the typical values of transconductance terms it is needed to estimate the standard deviation of the mismatch of g_m and R_{olb}. Although they are made of several elementary devices, we will consider them as a single equivalent compound device, which is statiscally equivalent, as demonstrated in section 1.2.4.1.

The variance of the transconductance mismatch $\sigma^2_{\Delta g_m}$ can be estimated through the dependence on collector current: $g_m = \frac{1}{V_T} I_C$ and considering that the mismatch of collector current is given by the mismatch in saturation current I_S for the Monte Carlo transistor model then,

$$\frac{\sigma_{\Delta g_m}}{g_m} = \frac{\sigma_{\Delta I_C}}{I_C} = \frac{\sigma_{\Delta I_S}}{I_S} \quad (4.89)$$

According to [73] and [162] for an emitter area of 3 units and a multiplier parameter of 2 the variance of the mismatch of the saturation current is $\frac{\sigma_{\Delta g_m}}{g_m} = \frac{\sigma_{\Delta I_C}}{I_C} = \frac{\sigma_{\Delta I_S}}{I_S} = 0.9\,\%$.

Considering $R_{olb} = r_o\left(1 + g_m R_{E_b}\right) =_{|g_m R_{E_b} \gg 1} r_o g_m R_{E_b} = \frac{V_E}{I_C}\frac{I_C}{V_T} R_{E_b} = \frac{V_E}{V_T} R_{E_b}$, the matching variations of the output resistance of the current source depend on the resistor matching, and then $\sigma^2_{\Delta R_{olb}}\Big|_{UNIT} = \left(\frac{\partial\left(\frac{V_E}{V_T} R_{E_b}\right)}{\partial R_{E_b}}\right)^2 \sigma^2_{R_{E_b}} = \left(\frac{V_E}{V_T}\right)^2 \sigma^2_{R_{E_b}}$ for each current source unit. Thus, the relative matching of the current source output resistance is $\sigma_{\Delta R_{olb}}\Big|_{UNIT} \Big/ R_{olb}\Big|_{UNIT} = \sigma_{R_{E_b}} \Big/ R_{E_b}$. It can be shown (see section 1.2.4.1) that for three units in parallel $\sigma_{\Delta R_{olb}} \Big/ R_{olb} = 1 \Big/ \sqrt{3}\,\sigma_{\Delta R_{olb}}\Big|_{UNIT} \Big/ R_{olb}\Big|_{UNIT}$. The value of circuit parameters is summarized in Table 4-3.

Parameter	Value	Parameter	Value
$g_{m\,=\,3\,x\,}g_{mb1}$	14 mS	I_{b1}, I_{b2}	360 µA
r_π	10 kΩ	$r_{oM2//M3}$	400 kΩ
r_o	120 kΩ	C_{sbM23}	300 fF
$\sigma_{\Delta Rc}/R_C$	0.2 %	R_{oIb}	500 kΩ
$\sigma_{\Delta Is}/Is=\sigma_{\Delta gm}/g_m$	0.9 %	C_{oIb}	200 fF
C_π	150 fF	R_{Eb2}/R_{Eb1}	1.5
R_E	1 kΩ	$\sigma_{\Delta REb1}/R_{Eb1}$	0.5 %
R_C	4 kΩ	g_{mb2}	3 mS

Table 4-3. Value of device parameters

Estimation for G_{DM} and G_{CM} in reset state ($Z_L \rightarrow 0$) would be, then

$$G_{DM} = \frac{g_m}{1+g_m R_E} = 0.93 \text{ mS} \qquad G_{CM} \simeq -\frac{r_o - r_o'}{r_o r_o'} = 2.4 \text{ µS} \qquad (4.90)$$

The "cross-transconductances" $G_{CM\text{-}DM}$ and $G_{DM\text{-}CM}$ depend on device matching, therefore the mean value is zero and the standard deviation is

$$\sigma_{G_{CM-DM}} \simeq \frac{1}{1+g_m R_E}\sqrt{\left(\frac{1}{r_o'}\frac{\sigma_{\Delta g_m}}{g_m}\right)^2 + \left(\frac{g_m R_E}{R_{oIb}}\frac{\sigma_{\Delta R_{oIb}}}{R_{oIb}}\right)^2} \simeq 7.2 \text{ nS} \quad \text{rms}$$

$$\sigma_{G_{DM-CM}} \simeq \frac{1}{4}\sqrt{\left(\frac{1}{(1+g_m R_E)r_\pi}\frac{\sigma_{\Delta g_m}}{g_m}\right)^2 + \left(\frac{1}{R_{oIb}}\frac{\sigma_{\Delta R_{oIb}}}{R_{oIb}}\right)^2} = 15 \text{ nS} \quad \text{rms} \qquad (4.91)$$

Figure 4-25 shows results of Monte Carlo simulations for the transconductances. As expected mean value is about zero for cross-terms: $G_{CM\text{-}DM}$ and $G_{DM\text{-}CM}$. Simulation results are in agreement with approximated calculations.

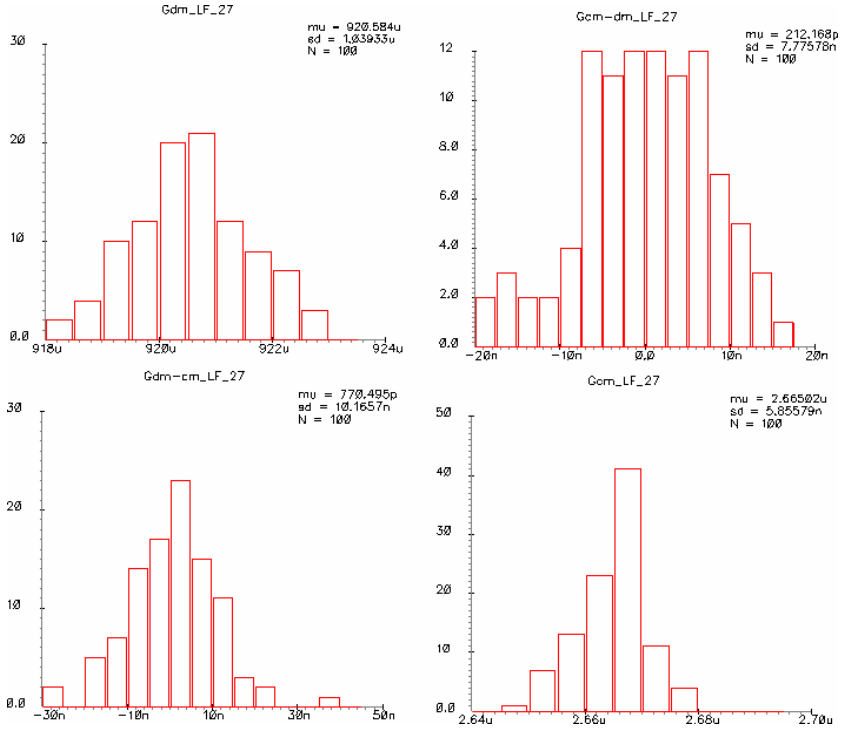

Figure 4-25. Histograms of the low frequency transconductances. Mismatch variations (100 runs).

It is also important to consider the frequency dependence of transconductor gains, this is shown in Figure 4-26. The transconductance G_{DM} has a dominant zero at about 600 MHz. The dominant time constant for G_{DM} is given by the emitter resistance R_E and the current source output capacitance C_{olb}, if R_E is replaced by the complex impedance $Z_E(s) = R_E // (1/sC_{olb}) = R_E / 1 + sR_E C_{olb}$ in (4.85),

$$G_{DM}(s) = \frac{R_C}{R_C + Z_L}\frac{1}{Z_E(s)} = \frac{R_C}{R_C + Z_L}\frac{(1 + sR_E C_{olb})}{R_E} \qquad (4.92)$$

According to (4.92) the differential-mode input to output transfer function has a dominant zero, which is not the typical dominant pole situation for voltage gain. The zero is linked to a reduction of the emitter degeneration effect as emitter impedance is reduced, resulting $G_{DM}\big|_{HF} \to g_m$.

The capacitance C_{olb} has two components that are added (are in parallel):

- The collector to substrate capacitance of the bipolar transistors of the current source, for eight current units in parallel it is about 150 fF (see appendix A.2.1).
- The base to collector capacitance of the bipolar transistors of the current sources in series with a big decoupling capacitor (500 fF) between base of the current master and the negative rail (AC ground). According to A.2.2 the base collector depletion capacitance for four current units in parallel is about 50 fF.

Thus C_{olb} is about 200 fF and the zero $1/2\pi C_{olb}R_E$ for the DM transconductance should be at about 800 MHz. Discrepancy with simulation could be provoked by small differences in parasitic capacitances of the transistors of the current sources or of the input pair. The other circuit time constants, given by $C\pi$ and $C\mu$ capacitances of the input pair transistors, become relevant at few GHz, introducing poles that decrease all the transconductances.

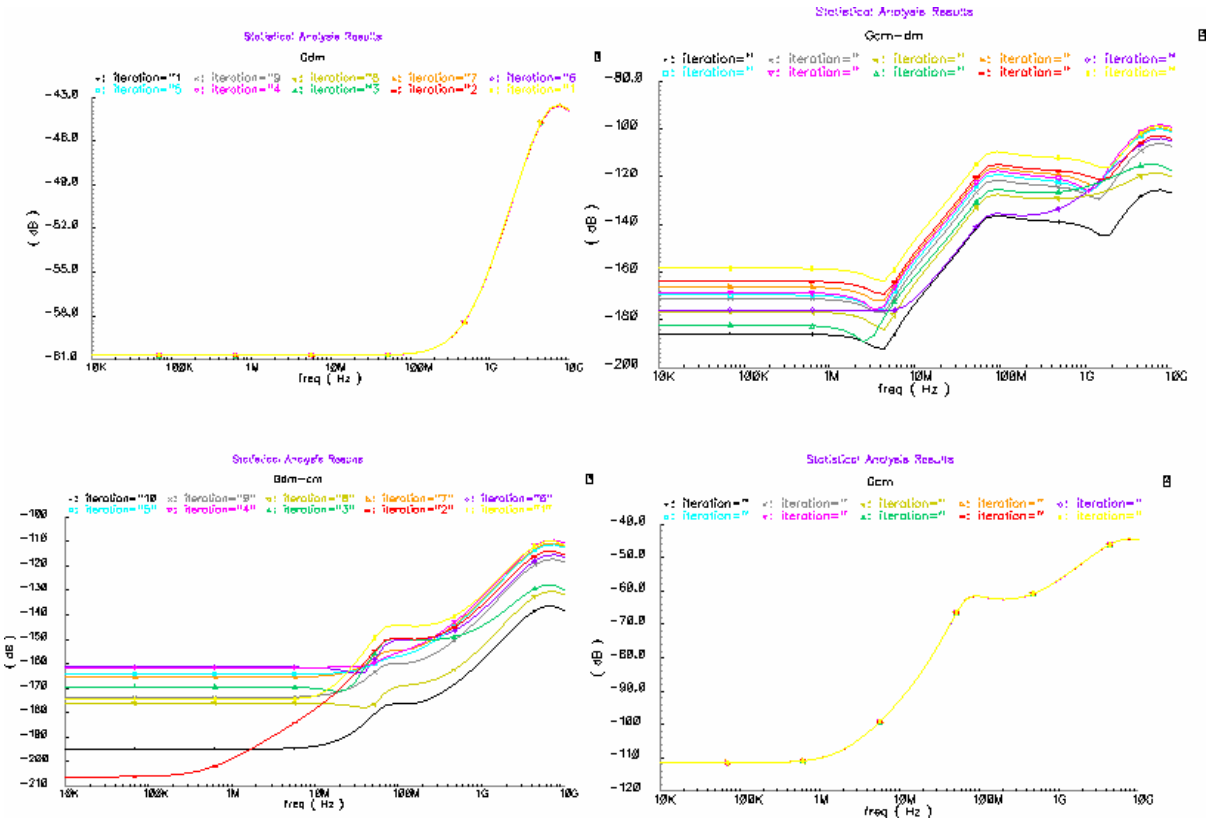

Figure 4-26. Small-signal transconductances for the integrator input stage. Mismatch variations in Monte Carlo simulations (10 runs).

The transconductance G_{CM} will increase as soon as the current source output impedance starts to decrease due to the current source output capacitance C_{oIb}. We replace the current source resistance R_{oIb} by the complex impedance $Z_{oIb}(s)$ in expression (4.85) having,

$$G_{CM}(s) \simeq \frac{R_C}{R_C + Z_L}\left(1 + sC_{oIb}\frac{r_o r_o^{'}}{r_o - r_o^{'}}\right)\frac{r_o - r_o^{'}}{r_o r_o^{'}} \qquad (4.93)$$

So, there is a dominant zero at $1/2\pi C_{oIb}\left(r_o r_o^{'}/\left(r_o - r_o^{'}\right)\right)$.

The analysis of $G_{CM\text{-}DM}$ is more subtle. It depends on $Z_o^{'}(s) = r_o^{'}/\left(1 + sr_o^{'}\left(C_{oIb} + C_\pi\right)\right)$ (C_π is base-emitter capacitance of Q_1-Q_2), but also the mismatch term ΔR_{oIb} has to be replaced by $\Delta Z_{oIb}(s) = f\left(\Delta R_{oIb}\right)$. By Error Propagation Theory:

$$\Delta Z_{oIb(s)} = \frac{\partial Z_{oIb(s)}}{\partial R_{oIb}}\Delta R_{oIb} = \frac{1}{\left(1 + sR_{oIb}C_{oIb}\right)^2}\Delta R_{oIb} \qquad (4.94)$$

and replacing r_o‘ by $Z_o^{'}(s)$ and ΔR_{oIb} by $\Delta Z_{oIb(s)}$ in (4.86)

$$G_{CM-DM}(s) \simeq \Big|_{\substack{Z_{oIb}(s) \gg R_E \\ Z_L \to 0}} \frac{1}{g_m R_E}\left(\frac{\left(1 + sr_o^{'}\left(C_{oIb} + C_\pi\right)\right)}{r_o^{'}}\frac{\Delta g_m}{g_m} + \frac{g_m R_E}{R_{oIb}}\frac{\Delta R_{oIb}}{R_{oIb}}\right) \qquad (4.95)$$

Both terms, the one depending on $\Delta R_{oIb}/R_{oIb}$ and the one depending on $\Delta g_m/g_m$, are comparable at DC but the former is frequency independent (up to few tens of MHz), whereas the later term is affected by the zero $1/2\pi r_o^{'}\left(C_{oIb} + C_\pi\right)$. The -3dB frequency is function of the zero position but is also influenced by the relative DC value of both terms and thus by matching.

$G_{CM\text{-}DM}$ depends on $Z_\pi(s) = R_\pi/\left(1 + sR_\pi\left(C_{oIb} + C_\pi\right)\right)$ and also on $\Delta Z_{oIb}(s)$,

$$G_{DM-CM}(s) \simeq \Big|_{Z_L \to 0} \frac{1}{4}\left(\frac{1 + sr_\pi\left(C_{oIb} + C_\pi\right)}{\left(1 + g_m R_E\right)r_\pi}\frac{\Delta g_m}{g_m} + \frac{1}{R_{oIb}}\frac{\Delta R_{oIb}}{R_{oIb}}\right) \qquad (4.96)$$

Since first term is typically much significant than second one, there is a dominant zero at a frequency $1/2\pi r_\pi\left(C_{oIb} + C_\pi\right)$. Also for $G_{CM\text{-}DM}$ some dependence of the zero on matching is possible when second term becomes comparable to the first one.

In Table 4-4 a detailed comparison between hand calculations and Monte Carlo simulations is given.

	Hand Calculation		Monte Carlo	
	Low Freq. [dB]	f-3dB [MHz]	Low Freq. [dB]	f-3dB [MHz]
G_{DM}	- 61	800	- 61	600
$G_{CM\text{-}DM}$	- 161 r.m.s	5*	- 162 r.m.s.	5*
G_{CM}	- 112	1.5	- 112	1.6
$G_{DM\text{-}CM}$	- 156 r.m.s	45*	- 160 r.m.s	30*
CMRR	**100 r.m.s**	**5 (pole)**	**101 r.m.s**	**5 (pole)**

Table 4-4. Hand calculation and simulation results of small-signal gains with $Z_L << R_C$.

4.2.2.2 Fully Differential Op Amp (FDOA)

The fully balanced Op Amp (Figure 4-27) is composed by two stages and a Common Mode Feedback (CMFB) circuit. The first one is a differential folded cascode stage ($Q_{1(d)} - M_{2(d)}$) with cascode loads ($M_{3(d)} - M_{4(d)}$). This is a high bandwidth stage: $Q_{1(d)}$ is loaded with low-input impedance stage, thus there is no voltage gain for $Q_{1(d)}$ and there is no Miller effect, and we obtain on that way, a low input capacitance. The use of bipolar devices allows achieving low offset voltage. Emitter degeneration resistors ($R_{E(d)}$) improve the input impedance, slew rate and the matching. The use of a cascode current source ($M_{1b1} - M_{2b1}$) is important to get a high CMRR. The current source is biased through an improved high-swing cascode circuit [167] which allows to have high output range (from $2 \cdot V_{SAT}$ to V_{cc}) and to compensate the Early effect, thus improving the current matching. This technique for biasing is also used for the cascode loads and the CMFB pair. The first stage is loaded through cascoded nMOS to have a gain of about 100 with low bias current.

The output stage is formed by a Darlington stage ($Q_{6(d)} - Q_{7(d)}$) and an emitter follower ($Q_{8(d)}$) to drive resistive loads. A pole splitting compensation is performed through and pole-zero network ($R_Z - C_C$) that applies local feedback on the output stage. A first order circuit analysis shows that the Gain-Bandwidth product (GBW) of the Op-Amp depends mainly on the transconductance of the first stage ($\approx 1/R_E$) and on the compensation capacitor (C_C):

$$GBW \simeq \frac{1}{2\pi R_E C_C} \tag{4.97}$$

The non-dominant poles depends on the zero of the compensation network (controlled through R_Z) and on the biasing output stage. The critical device parameters have been calculated first through simple models and then adjusted through simulation, obtaining: $R_E = 2k$, $C_C = 600fF$ and $R_Z = 2.6k$. The low frequency gain is about 30000, higher than the 60 dB that were required.

The CMFB circuit is based on an error amplifier ($Q_{9(d)}$) [168] which compares the reference for the output common mode (V_{CMref}) with the average of the outputs of the amplifier, calculated thanks to the resistors (R_{av}). A feedback network is formed by the mirrors ($M_{10(d)} - M_{5(d)}$), hence the CMFB error amplifier must have a bias current equal to the bias current of the input pair plus the current flowing through the cascode loads. The capacitors (C_{av}) in parallel with R_{av} allow compensating for the effect of the pole introduced by the parasitic capacitance of R_{av}. It needs to be taken into account that CMFB unity gain frequency must be two times higher than the amplifier one, this is achieved by having a higher transconductance on the error amplifier (R_{Ecm} value must be about half of the value of R_E). Note that since the bias current for the pair is fixed by a previous constraint, the emitter degeneration provides an additional degree of freedom needed to adjust the circuit.

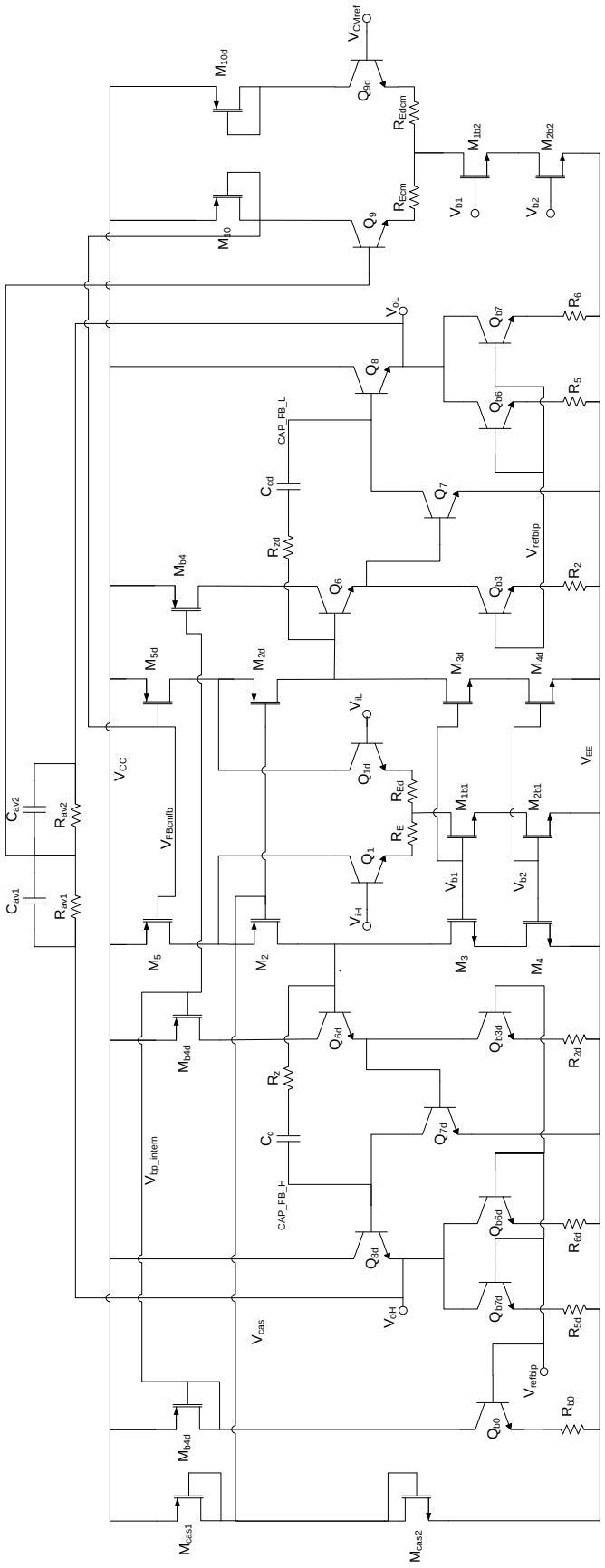

Figure 4-27. Schematics of the FDOA

4.2.2.2.1 Biasing and operating points

A high-swing cascode current source [167] is used to bias the input differential pair (Q_1-Q_{1d}), the differential pair of the CMFB error amplifier and the cascode loads M_3-M_4. It is shown in Figure 4-28. The gate voltages (V_{b1} and V_{b2}) for the cascode transistors are generated from an input reference current injected to the node "i_ref_bip". This current is generated using a band-gap current source (see section 4.5.1). Bypass capacitors are used to keep the V_{gs} voltages constant at high frequency.

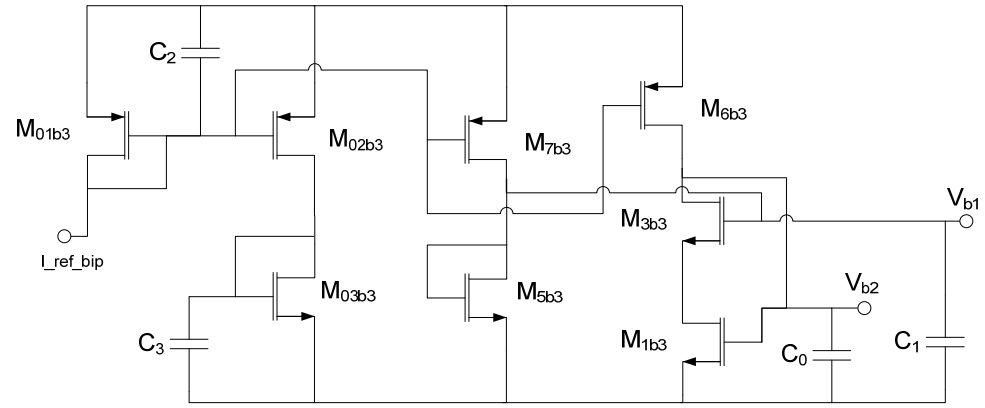

Figure 4-28. High-swing cascode current source.

Figure 4-29 shows the result of a DC simulation of the input CM range. Lower limit is fixed by the minimum output voltage required at the output of the cascode current sources. Upper limit is given by the saturation of the transistors of the input differential pair. Similar results are obtained for the differential pair of the error amplifier, then the V_{CMref} range is -0.5 V < V_{CMref} <1 V.

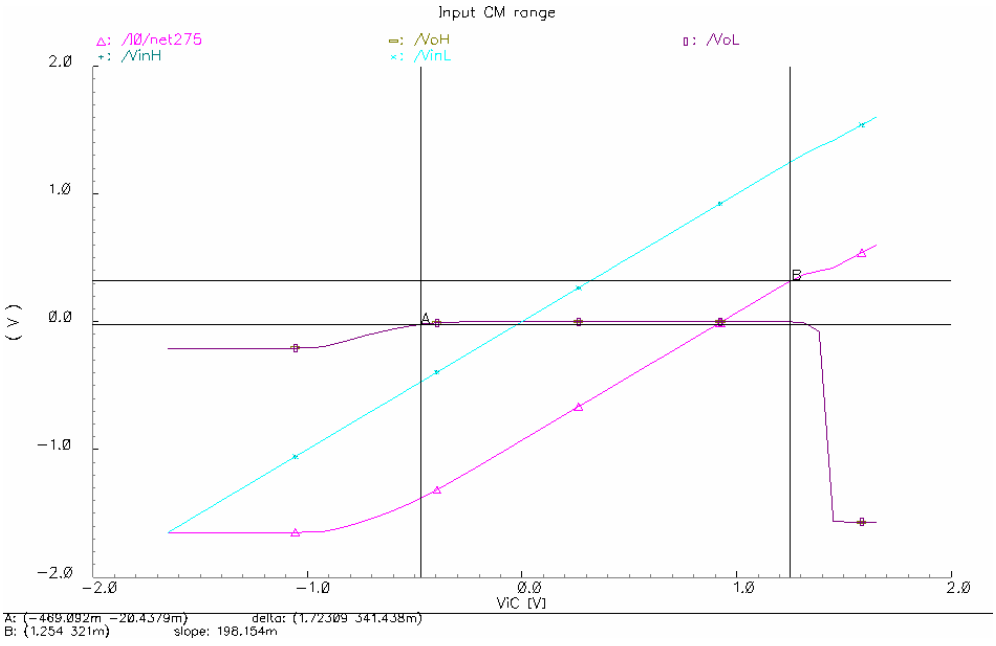

Figure 4-29. Input CM range.

The common-base transistor M_2 is biased through the voltage V_{CAS}, which is obtained through a voltage divide made of MOS transistors in saturation region. The value of V_{CAS} must be such that the transistors $Q_{1(d)}$ and $M_{5(d)}$ are in forward active (saturation for MOS) region. It is important also to

obtain the maximum signal excursion at the drain of $M_{2(d)}$; assuring that $M_{2(d)}$ operates in saturation region. A value of $V_{CAS} \approx$-0.5V is chosen.

Figure 4-30 shows the output DM range as a function of V_{iD}. It is obtained simulating the operation of the FDOA in a close-loop gain of 1. It is apparent that $|V_{oD}|$<1.5 V. The range is limited by the minimum drain to source voltage required to operate in saturation region by the bias current source M_{b4} at the Darlington stage.

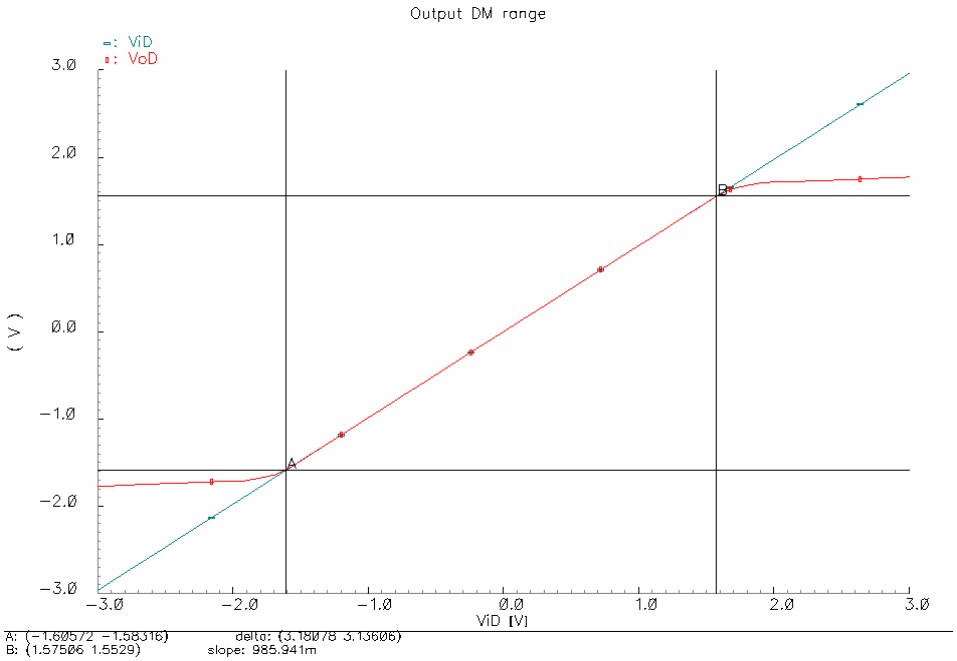

Figure 4-30. Output DM range as function of input DM voltage.

4.2.2.2.2 Frequency compensation

There are five key points to consider in the design of the FDOA for a closed loop operation:

1. *Low frequency differential gain (G_{DM0}).* The G_{DM0} must be high enough to:
   - Reduce the effects of the gain variations of the FDOA in the closed loop operation.
   - Minimize the non-linearity error.
   - Maximize the integration bandwidth at the low frequency (see section 4.2.2.3).

   Most of these errors are inversely proportional to G_{DM0}, to achieve a 0.1% precision G_{DM0} must be higher than 60 dB. The FDOA is made of two stages (plus an output emitter follower) to achieve this gain.

   The first stage is a folded cascode one ($Q_{1(d)}$ to $M_{5(d)}$), and its gain (G_{DM01}) is determined by the effective transconductance ($G_{MQ1} \simeq g_{mQ1} \Big/ \left(1 + g_{mQ1} R_E\right)$) of the input differential pair with emitter degeneration and the parallel combination of the output resistance of the cascode load ($R_{oM2} \simeq \left(g_{m2}\left(r_{oM5} \,/\!/\, r_{oQ1}\right)\right) r_{oM2}$, see section 6.6 in [66]), of the output resistance of the current source ($R_{oM3} \simeq \left(g_{m3} r_{oM4}\right) r_{oM3}$) and the input impedance of the Darlington stage ($R_{iDAR} \simeq r_{\pi Q6} + \left(\beta_{0Q6} + 1\right) r_{\pi Q7}$):

$$G_{DM01} = G_{MQ1} R_X \qquad (4.98)$$

where $R_X = R_{oM2} // R_{oM3} // R_{iDAR}$. Using small-signal parameters derived in A.3.1, $G_{MQ1} \approx 0.7$ mA/V and the impedance at the output of the cascade stage R_X is about 1MΩ. However, the first order model to compute the output resistance of MOS transistors is very imprecise and simulations shows that the impedance at this node is about 500 kΩ. Thus, the gain of the first stage is $G_{DM01} \approx 300$.

The gain (G_{DM02}) of the second stage, a Darlington CC-CE stage compose by $Q_{6(d)}$ and $Q_{7(d)}$, is given by its effective transconductance $G_{MDAR} \simeq \dfrac{g_{mQ7}}{1+\dfrac{r_{\pi Q6}}{\left(\beta_{0Q6}+1\right)r_{\pi Q7}}}$ and by its effective output impedance $R_{oDAR} \simeq r_{oQ7}$ in parallel with input impedance of the output buffer $R_{iQ8} \simeq r_{\pi Q8} + \left(\beta_{0Q8}+1\right)\left(r_{oQ8} // R_L\right)$, where R_L is the load resistance (or input impedance of the next stage, the Track and Hold):

$$G_{DM02} = G_{MDAR}\left(R_{oDAR} // R_{iQ8}\right) \qquad (4.99)$$

The gain of the Darlington stage (G_{DM02}) is given by its effective transconductance $G_{MDAR} \simeq \dfrac{g_{mQ7}}{1+\dfrac{r_{\pi Q6}}{\left(\beta_{0Q6}+1\right)r_{\pi Q7}}}$ and by its effective output impedance $R_{oDAR} \simeq r_{oQ7}$ in parallel with the output impedance of bias transistor M_{b4} and with the input impedance of the output buffer $R_{iQ8} \simeq r_{\pi Q8} + \left(\beta_{0Q8}+1\right)\left(r_{oQ8} // R_L\right)$, where R_L is the load resistance (or input impedance of the next stage, the Track and Hold):

$$G_{DM02} = G_{MDAR}\left(R_{oDAR} // r_{oMb4} // R_{iQ8}\right) \qquad (4.100)$$

According to the value of small signal parameters computed in appendix A.3.1, $r_{oMb4} \ll R_{oDAR}$ and $r_{oMb4} \ll R_{iQ8}$ for $R_L \gg 1$ kΩ. Thus, $G_{DM02} \simeq g_{mQ7} r_{oMb4}$. Again, the output impedance of the PMOS M_{b4} is only roughly estimated by the first order model and computer simulations shows that $r_{oMb4} \approx 22$ kΩ, then $G_{DM02} \approx 100$ and the low frequency gain of the amplifier is $G_{DM0} \approx 30000$ or about 90 dB.

2. *Gain Bandwidth Product (GBW)*. The product $G_{DM0} \cdot f_a$ is defined as the Gain Bandwidth Product, where f_a is the corner frequency where the gain is 3*dB* smaller than G_{DM0}. As studied in section 4.2.2.3, the integrator bandwidth is given by GBW and thus a GBW of about 200 MHz is required.
3. *Phase Margin (PM)*. The phase margin of the loop gain (T) must be at least of 60º to avoid ringing in the step transient response. It will be shown that when the integrator is in the integration state, the FDOA must be internally compensated as a general purpose amplifier (see section 9.4.1. in [66]) for the most difficult configuration (using resistive feedback): unity gain closed-loop situation.
4. *Settling time (t_s)*. The requirement on settling time is given by the maximum time to reset the integrator: < 10 ns. Assuming operation in the linear regime, for a first order system (PM > 75º) it can found that the settling time ([66],[67]) can be approximated by:

$$t_s(\varepsilon) \approx \frac{G_f}{2\pi GBW}\ln\left(\frac{1}{\varepsilon}\right) \qquad (4.101)$$

where G_f is the closed-loop gain and ε is the error when settling occurs. In the reset state G_f is about unity and the error will be required to be less than 1%. To have t_s<10ns, the GBW must be higher than 70 MHz.

5. *Slew rate (SR)*. In OpAmps, the SR is typically given by the non-linear operation of the input differential pair which is loaded by the compensation capacitor (C_C), in this the SR is ([66],[67]):

$$SR = \frac{dV}{dt} = \frac{I_{bias}}{C_f} \tag{4.102}$$

where I_{bias} is the bias current of the input differential pair (about 150μA). In the following discussion it will be show that C_C must be around 600 fF, the SR is 193 V/μs, i.e. for a maximum signal of 1V the reset time will be around 5 ns. The emitter degeneration in the input differential pair helps to increase the slewing capabilities: using the emitter degeneration, the bias current must be higher to achieve the same transconductance.

In the following paragraphs we will discuss the compensation of the FDOA which will determine the value of some important parameters: GBW, PM, t_s and SR. A classical approach for compensation using Miller multiplication of small internal feedback capacitance C_C is used to create a dominant pole situation. As well as allowing use of small capacitor that can be integrated on the monolithic chip, this type of compensation has another significant advantage. This is due to the phenomenon of pole splitting. Although it is a complex process involving a number of high frequency poles in Darlington stage, an approximate analysis [66] can be done replacing this stage by a single equivalent transistor Q_{DAR} as depicted in Figure 4-31 for the small signal differential half circuit, neglecting for the moment the resistor R_Z.

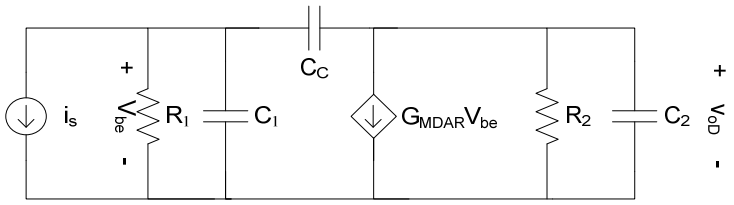

Figure 4-31. Small signal DM half circuit for the analysis of the compensation of the FDOA.

Some of the small signal parameters of the circuit of Figure 4-31 have been already discussed:

$$G_{MDAR} \simeq \frac{g_{mQ7}}{1+\dfrac{r_{\pi Q6}}{\left(\beta_{0Q6}+1\right)r_{\pi Q7}}} \simeq g_{mQ7} \simeq 4{,}45 \text{ mA/V} \tag{4.103}$$

$$R_1 = R_X = R_{oM2} \,//\, R_{oM3} \,//\, R_{iDAR} \simeq 500 \text{ k}\Omega \tag{4.104}$$

$$R_2 \simeq r_{oMb4} \simeq 22 \text{ k}\Omega \tag{4.105}$$

The stage i_s feed from a current is out of the cascode stage:

$$i_s = G_{MQ1} v_{iD} \simeq \frac{g_{mQ1}}{1+g_{mQ1}R_E} v_{iD} \tag{4.106}$$

where v_{iD} is the DM input voltage of the FDOA.

The C_1 capacitor is mainly the result parallel combination (sum) of the drain to bulk capacitance C_{sbM2} of $M_{2(d)}$, the drain to bulk capacitance C_{sbM3} of $M_{3(d)}$, the gate to drain capacitance C_{gdM2} of $M_{2(d)}$, the gate to drain capacitance of C_{gdM3} $M_{3(d)}$ and the input capacitance $C_{\pi Q6}$of $Q_{6(d)}$, thus:

$$C_1 = C_{gdM2} + C_{dbM2} + C_{gdM3} + C_{dbM3} + C_{\pi Q6} = 21 + 60 + 14 + 15 + 40 \simeq 150 \text{ fF} \tag{4.107}$$

Those capacitances are computed in appendix A.3. In the same way for C_2:

$$C_2 = C_{gdMb4} + C_{dbMb4} + C_{jsQ6} + C_{jsQ7} + C_{\pi Q8} = 42 + 90 + 55 + 55 + 100 \simeq 350\ fF \qquad (4.108)$$

Capacitor C_C represents compensation capacitance but also includes the effect of collector-base capacitance of transistors of the Darlington stage.

By simple circuit analysis (see section 9.4.2 in [66]) the transfer function of the circuit of Figure 4-31 can be found:

$$\frac{v_{oD}}{i_s}(s) = \frac{R_1 R_2 C_C (z - s)}{\left(1 - \frac{s}{p_1}\right)\left(1 - \frac{s}{p_2}\right)} \qquad (4.109)$$

Transfer function of equation (4.109) has two poles in left (negative) half plane and a zero in the positive half plane (RHP zero). The RHP zero is,

$$z = \frac{G_{MDAR}}{C_C} \qquad (4.110)$$

This RHP zero usually has such a large magnitude in bipolar transistors that it can be neglected, in our case $z \approx 2\pi \cdot 1.2$ GHz for a $C_C = 600$fF and $z \approx 2\pi \cdot 25$ GHz for a $C_C = 30$ fF (only the base collector capacitance of Darlington transistors). This is often not the case in MOS circuits because their have lower g_m and the RHP zero can affect the PM.

The dominant pole p_1 or p_d can be approximated (see section 9.4.2 in [66]):

$$p_1 = p_d \simeq -\frac{1}{G_{MDAR} R_2 R_1 C_C} = \frac{1}{G_{DM02} R_1 C_C} \qquad (4.111)$$

being G_{DM02} the voltage gain of the Darlington stage it is apparent the Miller effect on (4.111), and $p_d \approx 2\pi 5$ kHz for a $C_C = 600$fF and $p_d \approx 2\pi \cdot 100$ kHz for a $C_C = 30$ fF. Even with only the parasitic capacitance a dominant pole situation is created thanks to the Miller effect. The GBW of the circuit can now be estimated,

$$GBW \equiv G_{DM0} \frac{p_d}{2\pi} \simeq \frac{G_{MQ1}}{2\pi C_C} \qquad (4.112)$$

Thus the GBW is about 185 MHz for $C_C = 600$fF (3.7 GHz for $C_C = 30$fF), as required. Note that $1/G_{MQ1}$ is approximately R_E, so $GBW \simeq 1/2\pi R_E C_C$ depends on accurate components (typical matching about 1%). The second pole p_2 is

$$p_2 \simeq -\frac{G_{MDAR} C_C}{C_2 C_1 + C_C (C_2 + C_1)} \qquad (4.113)$$

$p_2 \approx 2\pi \cdot 1.2$ GHz for a $C_C = 600$fF and $p_2 \approx 2\pi \cdot 315$ MHz for a $C_C = 30$fF. Equation indicates that the dominant-pole magnitude p_d decrease as C_C increases, whereas shows that p_2 increases as C_C increases. Thus, increasing C_C causes the poles to split apart. This pole splitting technique is very useful and helps a lot to achieve a high PM. Unfortunately, the FDOA is a multi-stage circuit and the most significant non-dominant pole is not p_2.

Although the association of poles with nodes is only an approximation ([169]), it provides an intuitive approach to estimating the transfer function. We simply multiply the total equivalent capacitance by the total incremental resistance (both from the node of interest to ground), thus obtaining an equivalent time constant and hence a pole frequency. Doing this for the node corresponding to the collector of Q1 the approximated value of the most significant non-dominant pole p_{nd} can be found. The incremental resistance of the node (R_{nd}) is given by the input resistance of

the cascode transistor M_2, as it is in the common-gate configuration it can be approximated[r] by $R_{nd} \simeq 1/g_{mM2} \simeq 0.3\ mA/V$ (see section 3.4.2.2 in [66]). The equivalent capacitance at this node is,

$$C_{nd} \simeq \left(C_{gsM2} // \left(C_{gsMcas1} + C_{gsMcas2}\right)\right) + C_{sbM2} + C_{gdM5} + C_{dbM5} + C_{jcQ1} = 135 + 0 + 14 + 40 + 55 \simeq 250\ fF \quad (4.114)$$

and the approximated value of the non-dominant pole p_{nd} is,

$$p_{nd} \simeq \frac{g_{mM2}}{C_{nd}} \simeq 2\pi 200\ MHz \quad (4.115)$$

Figure 4-32 shows the results of a pole zero plot, generate with the Spectre simulator, for $C_C = 30fF$ and $C_C = 600fF$, and $R_Z = 0$ in both cases. Values of the first obtained by hand calculations are good approximations. The RHP zero appears for $C_C = 600fF$, as expected. The pole splitting effect in p_2 is also apparent.

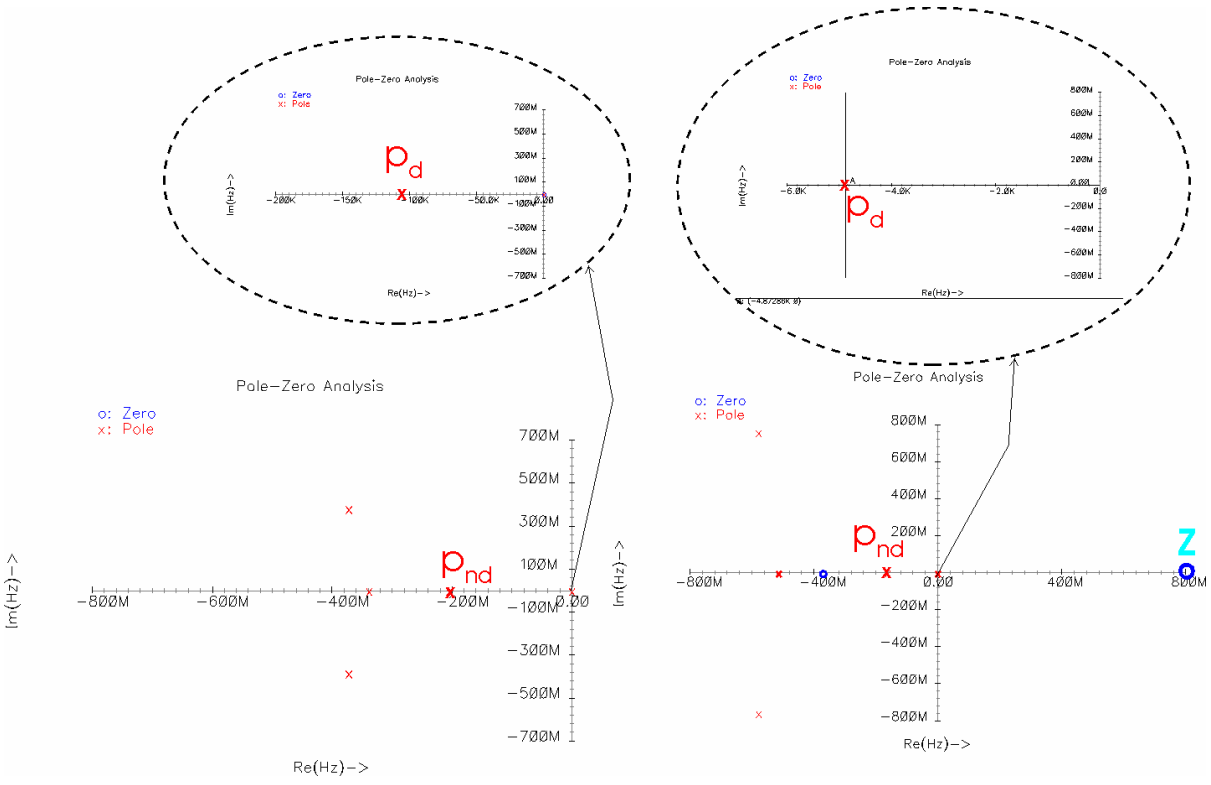

Figure 4-32. Pole zero diagram with $C_C = 30fF$ (left) and $C_C = 600fF$ (right).

Knowing the values for the dominant pole and zeros it is possible to compute the PM (only taking into account p_d and p_{nd}),

$$PM \equiv \varphi\left(T\left(j\omega_T\right)\right) + 180° \simeq \Big|_{\omega_T \simeq 2\pi GBW} - \arctan\left(\frac{2\pi GBW}{p_d}\right) - \arctan\left(\frac{2\pi GBW}{p_{nd}}\right) + 180° \quad (4.116)$$

The unity gain frequency ($f_T = \omega_T / 2\pi$) can be approximated by the GBW when there is only one dominant pole for $|T(j\omega)|>1$. This condition holds for a properly compensated amplifier, in our case for C_C=600fF, and then PM≈45º. Results of Spectre simulations shown in Figure 4-33 confirm these estimations, the FDOA would become unstable in close loop operation if no additional compensation

[r] Source terminal of all PMOS transistors is connected to the substrate (N-well) to avoid the body effect.

is added (C_C=30 fF). Increasing C_C to 600 fF makes the PM positive, however, as said above, a PM of 45º is not sufficient and additional compensation is needed.

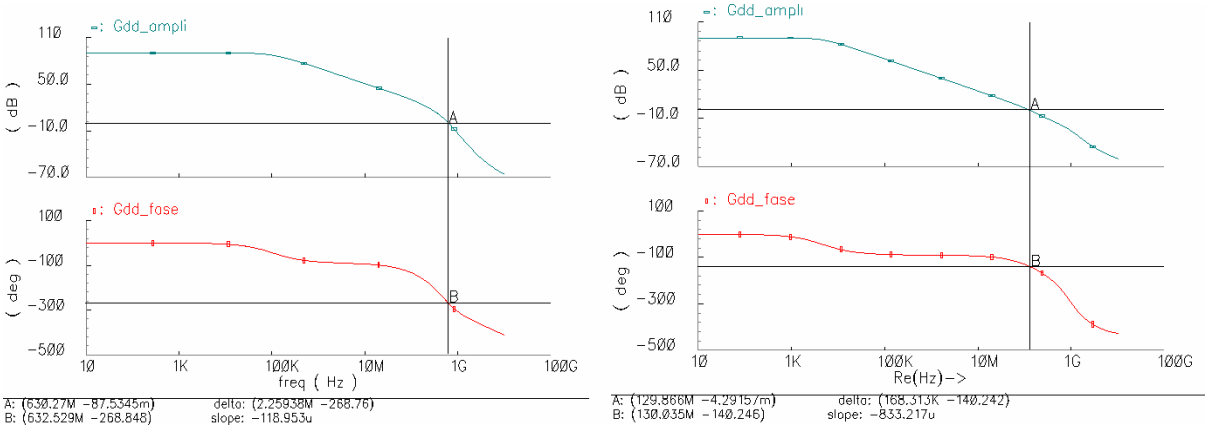

Figure 4-33. Gain (top) and phase (bottom) plots with C_C=30fF (left) and C_C=600fF (right)

A common way ([66] [67] and [169]) to deal with the RHP zero in circuits where it introduces a negative phase at relevant frequencies (reducing the PM) is to insert a resistor (R_Z) in series with the compensation capacitor. The resistor modifies the feedforward current introduced by C_C and allows to cancel the zero or even to move the zero to the LHP, which can be used to provide positive shift at high frequencies and improve the PM. It can be shown (see section 9.4.3 in [66]) that introducing R_Z does not affect poles p_1 and p_2 of the circuit of Figure 4-31, and that the new zero value is,

$$z = \frac{1}{\left(\frac{1}{G_{MDAR}} - R_Z\right)C_C} \qquad (4.117)$$

To compensate the effect of the first non-dominant pole, the zero frequency should be around 150 MHz, i.e. $R_Z \approx 2\ k\Omega$. The new PM is,

$$PM \simeq -\arctan\left(\frac{2\pi GBW}{p_d}\right) - \arctan\left(\frac{2\pi GBW}{p_{nd}}\right) + \arctan\left(\frac{2\pi GBW}{z}\right) + 180º \simeq \Big|_{p_{nd}\simeq z} 90º \qquad (4.118)$$

Figure 4-34 shows that according to Spectre simulations the PM is about 80º, this is due probably to the effect of the complex pole with real component of about 200 MHz shown in the pole zero plot.

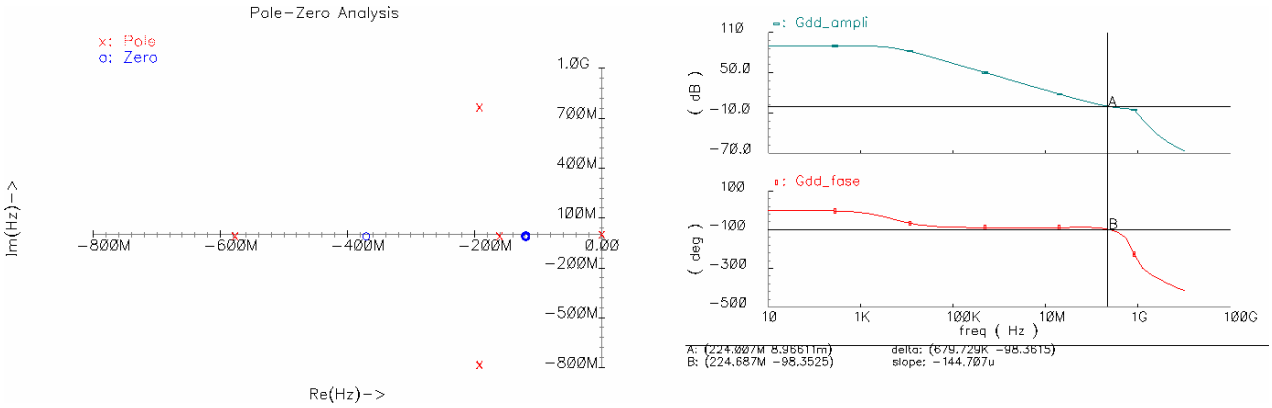

Figure 4-34. Pole zero diagram (left) and bode plot of magnitude and phase (right) of the FDOA with $R_Z \approx 2\ k\Omega$ and C_C=600fF.

The LHP zero also affects the unity gain frequency that is about 220 MHz, and the GBW is about 160 MHz. Although the PM (and unity gain frequency) might seem overcompensated, it is the result

of a "fine tuning" taking into account the parasitic capacitances and as will be shown later when this parasitics are taken into account the PM decreases.

Pole-zero pairs (doublets), as the p_{nd}-z pair, producing only minor changes in circuit frequency response can produce major changes in settling time. In [170] it is shown that a doublet introduces an exponential decay term in the step response (unity gain configuration), $k\,e^{t/\tau}$ with amplitude $k \simeq \frac{z - p_{nd}}{\omega_T}$ and with decay time-constant $\tau \simeq 1/z$. In our case, the zero frequency is about the GBW and the GBW is twice the required to achieve a settling time of 10 ns (to the 1%), therefore one could expect that the effect of the doublet can be compensated thanks to the extra GBW. According to Spectre simulations (see Figure 4-35) the settling time to the 1% is 9 ns in the linear regime. Figure 4-35 also shows the non-linear operation of the FDOA in unity gain closed loop configuration the SR is 172 V/µs close to expected value (193 V/µs). No overshoot is observed in the linear regime thanks to high PM.

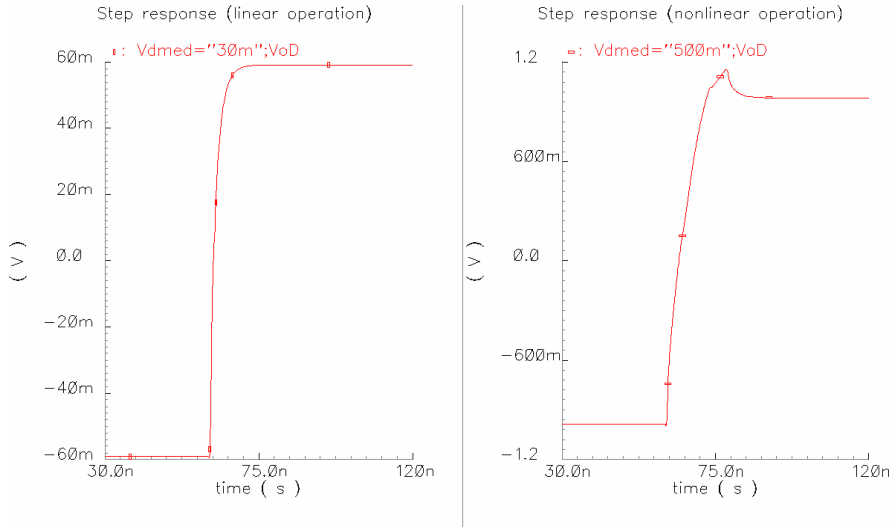

Figure 4-35. Step response (unity gain closed loop). Linear (left) vs non-linear regime (right).

Indeed, in [67] (see appendix A.6-1) it is shown that mismatch between circuit components creates also doublets. In that case the frequency of the zero of the doublet is a fraction (inversely proportional to the mismatch) of the pole associated with the component, thus it can be significant (large time constant). For instance the mismatch in C_C would generate a doublet with zero frequency $2\pi f_z = \frac{p_d}{1 + \Delta C_C / 2C_C}$. However, amplitude of the term in the step response is $k \simeq \frac{\Delta f_{pz}}{GBW} \simeq\Big|_{\Delta C_C \ll 1} \frac{p_d \, \Delta C_C / 2C_C}{GBW} \simeq \frac{\Delta C_C / 2C_C}{G_{DM0}}$, for typical mismatch on the order of 1% (for poly resistors and capacitors) and with a large low frequency open loop gain the effect of the mismatch should be negligible. Figure 4-36 confirms that the effect of mismatch on the settling time and on the SR is negligible.

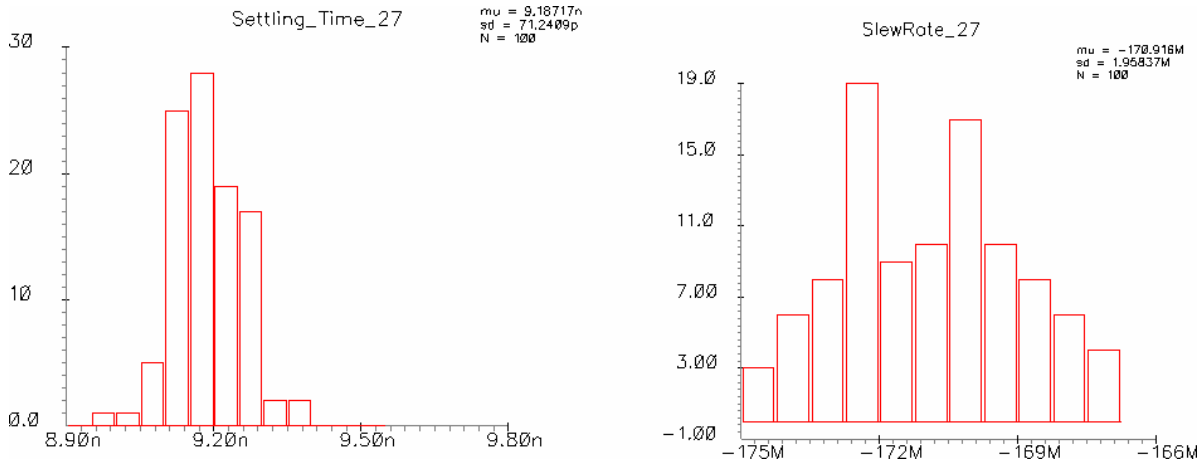

Figure 4-36. Results of Monte Carlo simulation (mismatch) for the settling time (left) and the slew rate (right) of the FDOA in unity gain closed loop operation.

Although the load of the FDOA is fixed (the input stage of the track and hold block) it is interesting to check the sensitivity of relevant parameters such GBW, PM, BW and low frequency gain to different load capacitances. According to the results of Spectre simulation shown in Figure 4-37, the effect is negligible in almost all parameters thanks to the emitter follower output stage, which provides low output impedance and high bandwidth. The most significant effects are in PM, although for a typical load capacitance of few hundreds of fF the PM exceeds the 75º.

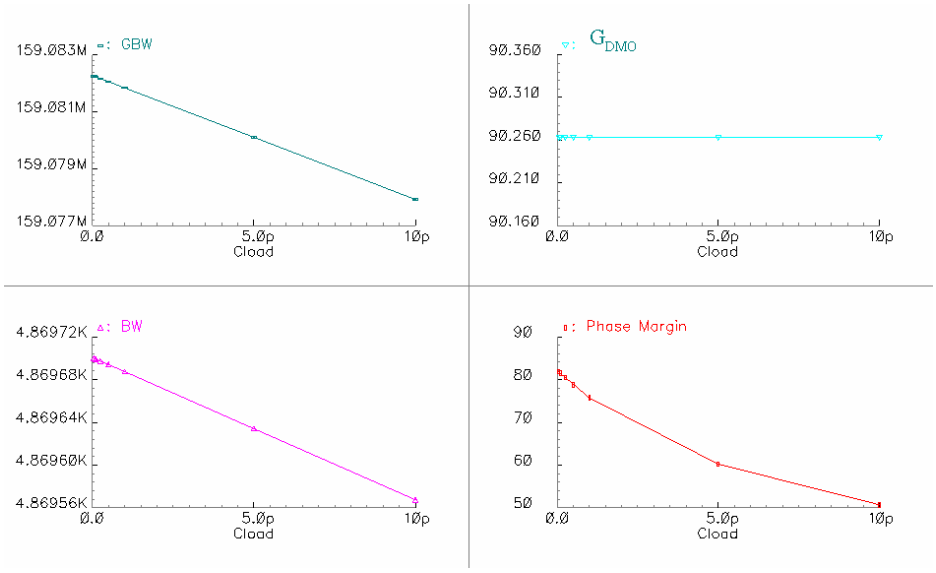

Figure 4-37. Effect of variation of load capacitance of the FDOA on main parameters.

Post layout simulations (Figure 4-38) have been performed to obtain the correct unity gain frequency (about 180 MHz) and PM (70º), taking into account the effect of the parasitic stray capacitances.

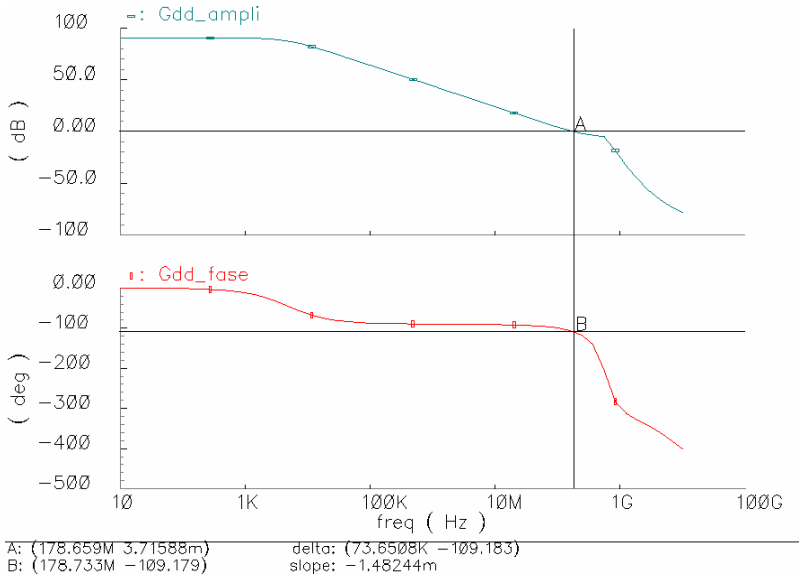

Figure 4-38. Bode plot of magnitude (top) and phase (bottom) of the FDOA from post-layout simulations.

4.2.2.2.3 Common mode feedback (CMFB)

All the transistors ($Q_{1(d)}$ to $Q_{8(d)}$) of the differential path should operate in the forward-active region (or saturation for MOS), as usual for high impedance nodes. Three different branches are connected to the node corresponding to the collector of $Q_{1(d)}$, and each branch has a different bias current source associated. Therefore the total bias (quiescent) current must be balanced,

$$I_{CQ1(d)} + I_{DM2(d)} = I_{DM5(d)} = I_{CQ9(d)} \qquad (4.119)$$

However, condition (4.119) is impossible to fulfill with complete precision due to the mismatch. Any difference in the currents caused by the mismatch will flow through the intrinsic impedance of the amplifier (which is very high to achieve high gain), creating and output voltage error that could be large enough to drive current sources to the triode region. In high gain amplifiers the output CM level is quite sensitive to device properties and mismatches and it can not be stabilized by means of differential feedback. Thus, a common-mode feedback network (CMFB) must be added to sense the CM level of the two outputs and accordingly adjust one of the bias currents of the amplifier ([66], [67] and [161]). The former function is done by the resistors R_{av1} and R_{av2} in Figure 4-27. The later is done by an error amplifier, the differential pair composed by Q_9 and Q_{9d}.

It is important to note that the use of CMFB circuit does not avoid the necessity to balance the bias DC currents on average, because the negative feedback loop is "small-signal" loop that must operate around a correct bias state having all transistors in active region.

There are many different proposals for CMFB circuits ([66], [67], [161]), both with continuous and switched capacitor circuits. The CMFB circuit proposed in [168] is taken, because it attains accurate output balancing, controlling precisely the value of the output common-mode through an error amplifier. The CM summation point (V_{cm_av}) is at the middle point between R_{av1} and R_{av2}. This point is fed to a differential pair with transistors Q_9 and Q_{9d}. The other input of this pair is connected to a reference input (V_{CMref}) that sets the FDOA output CM (V_{oC}). The common-mode feedback loop is closed through current mirrors M_{10}-$M_{5(d)}$.

Before doing a small-signal analysis, it is interesting to study how CMFB works. Let us suppose that the difference between output CM and its reference value (v_{cm_av}-v_{CMref}) increases, i_{ICQ9}=i_{DM10}=i_{DM5} also increase. Then, the voltage at the input of the Darlington stage also increases by $\Delta i_{DM5} R_1$ (R_1 is the incremental impedance at the base of Q_6 to ground). As the Darlington is an inverting stage the output tends to decrease, and v_{cm_av}- v_{CMref} decreases, counteracting the initial supposition.

Figure 4-39 shows transient simulation results of output CM control through variation of the reference of the CMFB error amplifier ($V_{cm\_in\_ref}$). The output CM (V_{cm_av}) ofollows $V_{cm\_in\_ref}$. V_{oH} and V_{oL} also follow $V_{cm\_in\_ref}$ because V_{iD}=0. Concerning, quiescent currents it is shown that condition (4.119) holds.

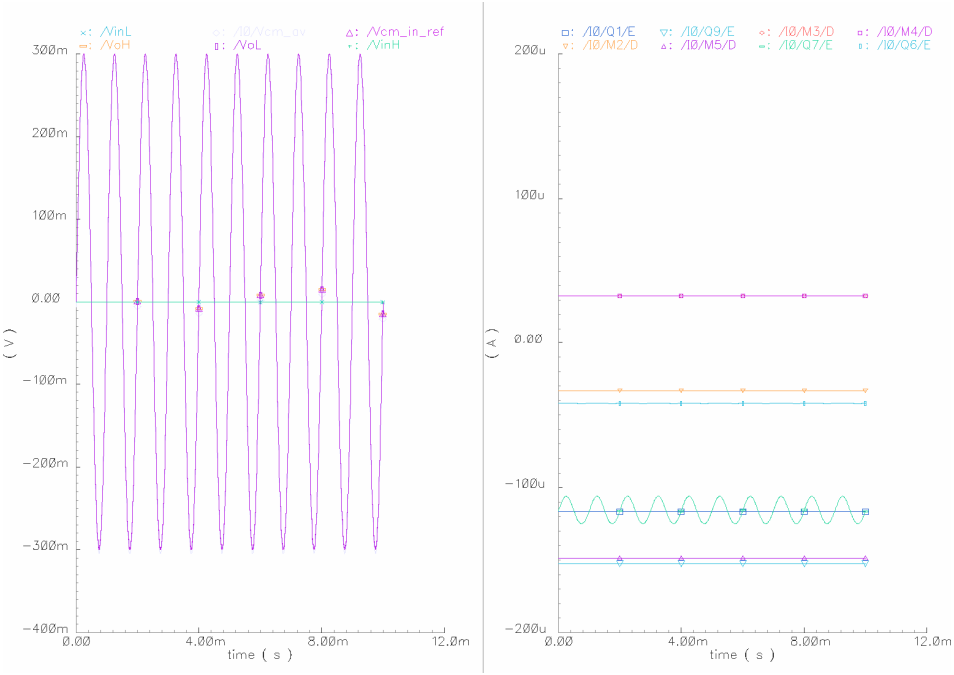

Figure 4-39. Transient simulation results of output CM control through variation of the reference of the CMFB error amplifier. Voltage (left) and currents (right).

The amplifier should inherently have as much CM open-loop gain as possible (similar to the differential-mode gain). The bandwidth of the CM loop has to be at least as large as the highest frequency at which output balancing is desired. In many applications this bandwidth should be the same as the differential-mode bandwidth of the amplifier. Therefore the GBW_{CM} of the CM amplifier must be equal or large than the GBW of the differential amplifier. In order to ensure CM stability, CM loop compensation is necessary. If the CM and DM signal path are merged at the very front end of the amplifier and their remaining separate parts are identical these objectives can be achieved automatically by the regular design of the differential amplifier. This strategy is followed: the differential pair of the error amplifier circuit is equivalent to input differential pair, because the output current of both pairs is connected to the source of cascode transistor M_2 (in the case of the error amplifier through a current mirror). Nevertheless, the error amplifier will always add some nodes, and therefore some non-dominant poles.

To analyze the CMFB feedback open-loop gain (T_{CMFB}) we will use return ratio analysis techniques [172], which for some situations are easier than two-port analysis where correct input and output variables and the type of feedback must be identified. In this technique, the closed-loop properties of a feedback circuit are described in terms of the return ratio (T_{CMFB}), which is the open loop gain, for a dependent source in the small-signal model of an active device. The return ratio for a dependent source in a feedback loop is found by the following procedure:

1. Set all independent sources to zero.
2. Disconnect the dependent source from the rest of the circuit, which introduces a break in the feedback loop.
3. Replace the dependent source by an independent source of value s_t of the same type and sign.
4. Find the return signal s_r generated by the independent source (at the controlling signal of the disconnected dependent source). The return ratio will be the negative of s_r, T=- s_r.

A simplified small-signal half circuit for the analysis of the CMFB loop is depicted in Figure 4-40. It is important to take into account the following remarks:

- The half-circuit of the differential pair of the error amplifier is the DM half-circuit. The DM input voltage is $v_{iD\_ER}=v_{cm\_avg}-v_{CMref}$. R_{IER} is the input resistance of the error amplifier and the effective transconductance (G_{MER}) of the differential pair Q9(d) is,

$$G_{MER}=\frac{g_{mQ9(d)}}{1+g_{mQ9(d)}R_{ECm}} \qquad (4.120)$$

- A factor ½ scales the transconductance G_{MER} to take into account that only half of the small signal current of the differential of the error amplifier is mirrored to input stage.
- For the return ratio calculation v_{CMref} must be set to 0, and then it is ignored.
- For the main differential amplifier the small signal representation of one signal path is taken.
- The collector current i_{cQ9} is ideally copied transmitted to the source of transistors M_2 and M_{2d} thanks to the current mirrors M_{10}-$M_{5(d)}$.
- The small-signal current gain of common-gate transistors $M_{2(d)}$ is unitary ($G_{MCAS}=g_{mM2(d)}\approx 1/R_{nd}$).
- The voltage gain of emitter follower $Q_{8(d)}$ is approximately one ($G_{Q8(d)}=1$) and its output impedance is $R_{oQ8}<<R_{av}$.
- C_{PAR} represents the parasitic capacitance at node v_{cm_avg}, including input capacitance of the error amplifier and poly2 to substrate capacitance of resistor R_{av}.
- Other circuit parameters have been defined in the previous section (4.2.2.2.2).

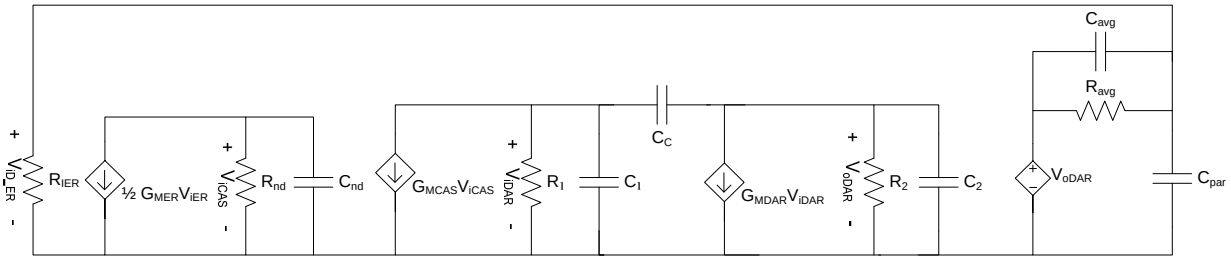

Figure 4-40. Small-signal half circuit for the analysis of the return ratio CMFB circuit.

From Figure 4-40 it is clear how DM and CMFB circuits share most of the small-signal path. To analyze the return ratio V_{oDAR} is chosen as s_r and the corresponding voltage controlled voltage source as s_t. By simple circuit analysis (see previous section), one can find the low frequency value for the return ratio of the CMFB circuit,

$$T_{CMFB}(0)=\frac{1}{2}G_{MER}R_1G_{DAR}R_2 \qquad (4.121)$$

and the GBW of the CMFB circuit,

$$GBW_{CMFB}\simeq\frac{1}{2}\frac{G_{MER}}{2\pi C_C} \qquad (4.122)$$

Comparing (4.112) and (4.122) it is clear that to have $GBW\approx GBW_{CMFB}$, the condition $G_{MER}=2G_{MQ1}$ arises, this is accomplished by making $R_E\approx 2R_{ECM}$. Doing this the low frequency return ratio of the CMFB circuit will be approximately equal to the low frequency differential gain: $T_{CMFB}(0)\approx G_{DM0}$. Concerning the PM, the non-dominant poles related to elements depicted in Figure 4-40 are the same that have been studied in previous section with one exception, the pole related to C_{PAR}. Indeed, capacitor C_{avg} is included to provide a high-frequency bypass of C_{PAR}. It can be shown that C_{avg} performs a pole zero cancellation in the return ratio transfer function provided that $C_{avg}>>C_{PAR}$,

$$\frac{C_{avg}}{C_{avg}+C_{PAR}}\frac{s+\dfrac{1}{C_{avg}R_{avg}}}{s+\dfrac{1}{\left(C_{avg}+C_{PAR}\right)R_{avg}}}\simeq\Big|_{C_{avg}\gg C_{PAR}}1 \qquad (4.123)$$

In [172] some techniques to break the feedback loop in order to measure the return ratio are presented. The most straightforward way, is just to break the loop (c-c'), then to inject a signal at point (c) and to measure the return signal at the other side of the break (c'). Incremental impedance seen at node c' must be the same seen before breaking the loop. Unfortunately, there cases where the loop can not be cut because the amplifier's DC-biasing scheme depends on keeping the loop intact for DC signals. As the CMFB is precisely dedicated to set the DC operating point, this is one of these situations. To get around this problem we cut the loop at c-c' in Figure 4-41, and terminate the right-hand of the cut in R_{I_ER}. We also introduce a large inductor between terminals c and c', as shown in Figure 4-41. If the inductor's reactance is large enough in the frequency range of interest to prevent AC-signal propagation around the loop, then the loop is effectively cut at c-c'. We are now in a position to measure the loop gain by adding a voltage source Voc, then $T=-v_{oc}/v_{ocp}$, where v_{ocp} is the voltage at c'.

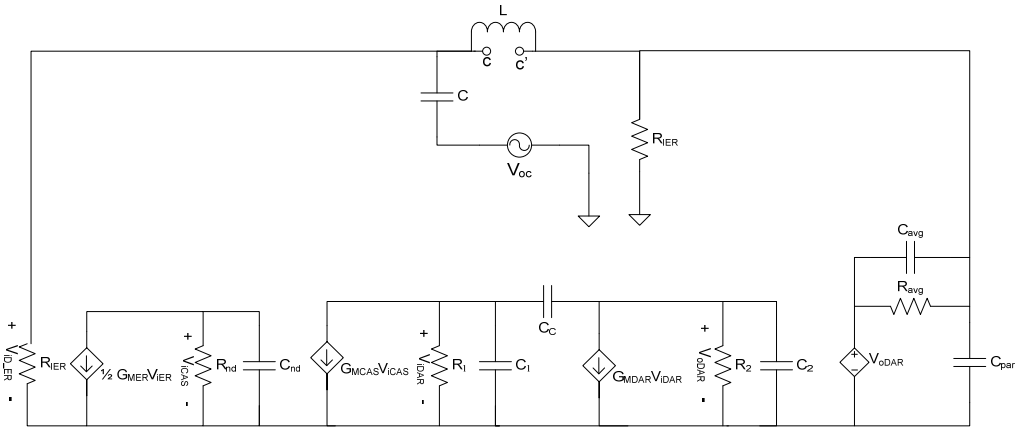

Figure 4-41. Circuit for measure the return ratio of the CMFB circuit.

This technique allows to perform transient and small signal simulations to study the open loop gain, see Figure 4-42.

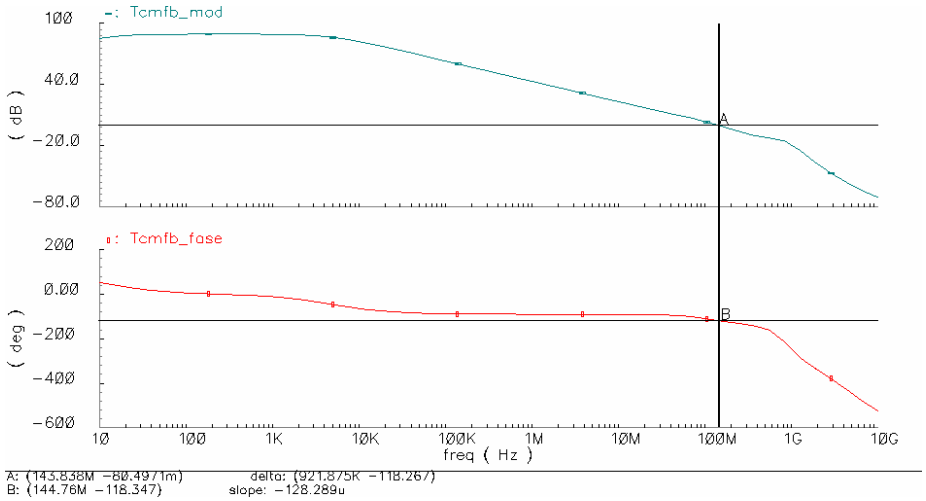

Figure 4-42. Small signal AC simulation of CMFB loop gain.

In the band of interest (from 500 Hz, 1 decade below the expected value for the dominant pole) $Z_L>>R_{I\_ER}$, as the value of R_{I_ER} is of the order of tens of kΩ an inductor of 50 H is used for the

simulation. According to the results shown in Figure 4-42 the low frequency gain is 89.5 dB and unit gain frequency is about 150 MHz, approximately equal to the GBW_{CMFB}. As expected, these figures of merit are close to the ones of the differential gain. The PM of the CMFB loop is about 60 º, smaller than the one of the DM loop. This was not unexpected, as the CMFB has more nodes than the DM loop, for example non-dominant poles of transistors M_2 and M_5 of the current mirror are contributing to the PM value. It is important to note that if the pole-zero cancellation capacitor C_{av} is not included in the circuit the PM of the CMFB loop is only 45º. The effect of the blocking inductor is visible at frequencies below 100Hz.

4.2.2.3 Integrator transfer function and MIP pulse response

In order to carry out a first order small signal analysis of the integrator circuit in the frequency domain using Laplace transform, we assume a dominant pole model for the Op Amp differential gain (G_{DM}), as shown in (4.124), where G_{DM0} is the low frequency differential gain and $f_a = 1/2\pi\omega_a$ the corner frequency where the gain is $3dB$ smaller than G_{DM0}. The product $G_{DM0} \cdot f_a$ is defined as the Gain Bandwidth Product (GBW), and it is often approximated for a dominant-pole response by the unity gain frequency ($f_T = 1/2\pi\omega_T$) of the Op Amp.

$$G_{DM}(s) = G_{DM0}\frac{\omega_a}{s+\omega_a} = \frac{2\pi GBW}{s+\omega_a} \qquad (4.124)$$

Figure 4-43 shows the differential-mode half circuit of the integrator. The input and output resistances are considered infinity and zero respectively, and the parasitic small-gains of the Op Amp are neglected. Signal $V_{yD}/2$ is the differential input voltage and the differential output voltage is $V_{oD}/2 = -G_{DM}(s)V_{yD}/2$, where the minus indicates the inverting configuration of the Op Amp feedback.

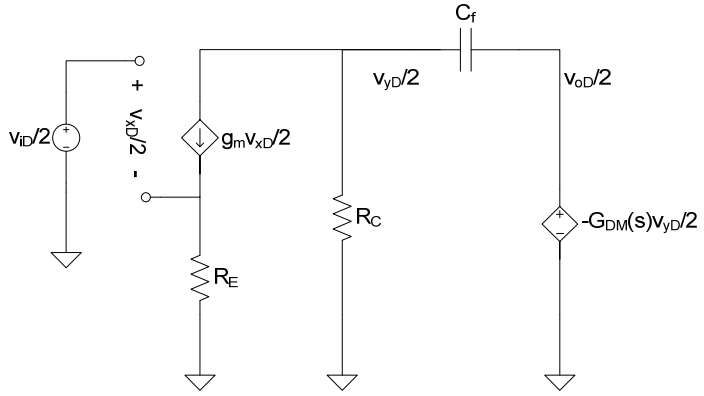

Figure 4-43. Differential-mode half circuit of the integrator

Through simple circuit analysis and taking (4.124) the integrator transfer function *I(s)* is derived,

$$I(s) = \frac{v_{oD}(s)}{v_{iD}(s)} = \frac{\omega_T \dfrac{1}{R_E C_f}}{s^2 + s\left(\omega_T + \dfrac{1}{R_C C_f}\right) + \dfrac{\omega_a}{R_C C_f}} \qquad (4.125)$$

The denominator of I(s) is a second order expression indicating that the system presents two poles

$$(s+p_1)(s+p_s) = s^2 + s(p_1+p_2) + p_1 p_2 \qquad (4.126)$$

The poles can be easily found if they are widely spaced in frequency, i. e. if $p_1 >> p_2$

$$s^2 + s(p_1+p_2) + p_1 p_2 \simeq s^2 + s p_1 + p_1 p_2 \qquad (4.127)$$

Then, the highest frequency pole p_1 is:

$$p_1 \simeq \omega_T + \frac{1}{R_C C_f} \simeq \omega_T \quad for \quad \omega_T \gg \frac{1}{R_C C_f} \tag{4.128}$$

For the low frequency pole p_2 we have

$$p_2 \simeq \frac{1}{G_{DM0}} \left(\omega_T \,||\, \frac{1}{R_C C_f} \right) \simeq \frac{1}{G_{DM0} R_C C_f} \quad for \quad \omega_T \gg \frac{1}{R_C C_f} \tag{4.129}$$

Figure 4-44 shows simulation results for the integrator frequency response.

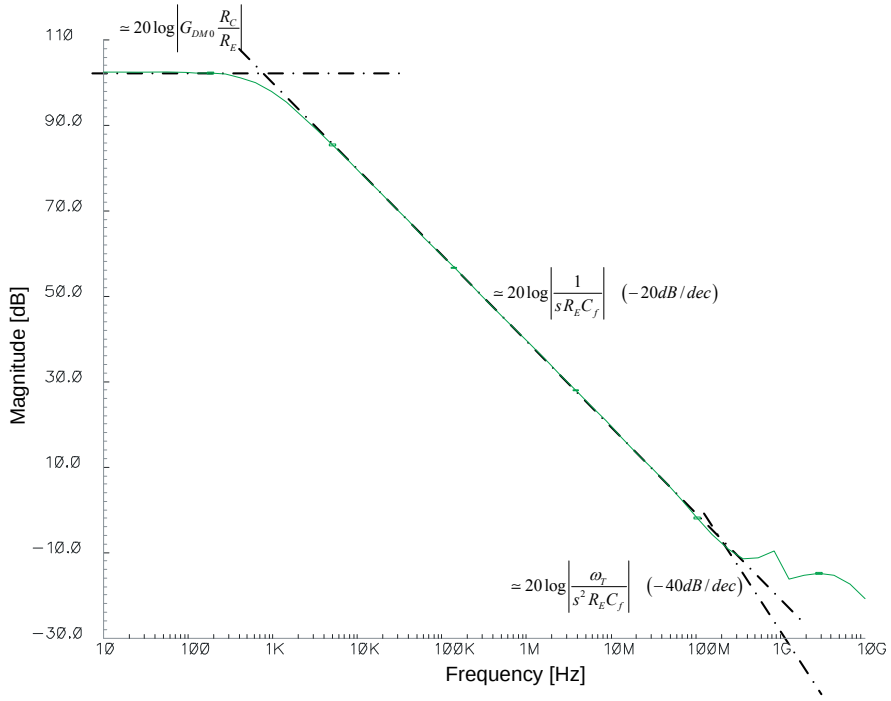

Figure 4-44. Simulation of the integrator frequency response with gain asymptotes.

Three different regions can be distinguished:

a) Low frequency region: $\omega \ll \frac{1}{G_{DM0} R_C C_f}$,

$$\left| I(s) \right|_{LF} \Big| \simeq \left| G_{DM0} \frac{R_C}{R_E} \right| \tag{4.130}$$

b) Mid frequency or integration band: $\frac{1}{G_{DM0} R_C C_f} \ll \omega \ll \omega_T$,

$$\left| I(s) \right|_{INT} \Big| \simeq \left| \frac{\omega_T \frac{1}{R_E C_f}}{s\left(s + \omega_T + \frac{1}{R_C C_f} \right)} \right| \simeq \left| \frac{\omega_i'}{s} \right| \tag{4.131}$$

where $\omega_i' = \frac{1}{R_E C_f} \left(\frac{1}{1 + \frac{1/R_C C_f}{\omega_T}} \right) \simeq \Big|_{1/R_C C_f \ll \omega_T} \frac{1}{R_E C_f}$

c) High frequency region: $\omega \gg \omega_T$,

$$\left|I(s)\right|_{HF}\left| \simeq \right|\frac{\omega_T}{s^2 R_E C_f}\Bigg| \tag{4.132}$$

The circuit behaves as an integrator in the mid band, therefore it is important to assure that this band covers the PMT signal bandwidth. The PMT signal bandwidth is from DC to about 100 MHz for the single photoelectron response in the worst case (no effect of stray capacitance at the PMT anode). In order to have some margin the goal has been to achieve $f_T \approx 200$ MHz. The low frequency pole can not be moved to DC because of the effect of R_C, at low frequency its impedance is smaller than the input impedance of the circuit composed by the FDOA and the feedback capacitor and the small signal current flows through R_C. Nevertheless, thanks to the feedback (Miller effect) the input capacitance much higher than C_C, it is $C_C G_{DM0}$. A low frequency gain of at least 60 dB has been required. The low frequency gain of the FDOA G_{DM0} is about 90 dB, then using expression (4.129) the expected value of p_2 is about 900 Hz, fitting well with simulation results shown in Figure 4-44, where p_2 is about 700 Hz. Simulations fit very well with hand calculations for low and mid frequencies (up to the unity gain frequency of the FDOA) at high frequency the non-dominant poles and zeros of the FDOA introduce discrepancies.

Once the integrator transfer function has been determined, it is possible to study the response to a typical MIP pulse. For an ideal preamplifier of gain A_{DM} (constant in the band of interest), and using (4.3) the integrator input signal is:

$$v_{iD}(t) \simeq \Big|_{\tau_C \ll \tau} A_{DM} \frac{Q_{MIP}}{\tau} R_{PMT} \left(e^{-\frac{t}{\tau_C}} - e^{-\frac{t}{\tau}} \right) u(t) \tag{4.133}$$

Neglecting the effect of R_C, the integrator response is

$$I(s) \simeq \frac{\omega_T \omega_i^{'}}{s(s+\omega_T)} \tag{4.134}$$

The Laplace transform of the integrator's output is

$$V_{oD}(s) = I(s) V_{iD}(s) = \left(\frac{\omega_T \omega_i^{'}}{s(s+\omega_T)} \right) \left(A_{DM} \frac{Q_{MIP}}{\tau} R_{PMT} \left(\frac{1}{s+\frac{1}{\tau_C}} - \frac{1}{s+\frac{1}{\tau}} \right) \right) = \tag{4.135}$$

$$-\omega_T \omega_i^{'} A_{DM} \frac{Q_{MIP} R_{PMT}}{\tau \tau_C} \left(\frac{1}{s(s+\omega_T)\left(s+\frac{1}{\tau_C}\right)\left(s+\frac{1}{\tau}\right)} \right)$$

where $V_{iD}(s)$ is the Laplace transform of $v_{iD}(t)$. Using Heaviside's partial fraction expansion:

$$V_{oD}(s) = -\omega_T \omega_i^{'} A_{DM} \frac{Q_{MIP} R_{PMT}}{\tau \tau_C} \left(\frac{k_1}{s} + \frac{k_2}{s+\omega_T} + \frac{k_3}{s+\frac{1}{\tau_C}} + \frac{k_4}{s+\frac{1}{\tau}} \right) \tag{4.136}$$

The coefficients k_i, also called residues, are computed as

$$k_i \equiv \left(\left(s+p_i\right) \left(\frac{1}{s\left(s+\omega_T\right)\left(s+\frac{1}{\tau_C}\right)\left(s+\frac{1}{\tau}\right)} \right) \right)_{s=-p_i} \qquad (4.137)$$

where p_i is the pole of the fraction corresponding to k_i. Assuming that the dominating time constant is the signal (Scintillator, fiber, etc) time constant τ,

$$V_{oD}\left(s\right) \simeq \Big|_{\substack{\tau \gg \tau_C \\ \tau \gg 1/\omega_T}} -\omega_T \omega_i^{'} A_{DM} \frac{Q_{MIP} R_{PMT}}{\tau \tau_C} \left(\frac{\tau \tau_C}{\omega_T} \frac{1}{s} - \frac{\tau \tau_C}{\omega_T} \frac{1}{s+\frac{1}{\tau}} \right) \qquad (4.138)$$

We have seen that $\tau \gg \tau_C$ means that the voltage at the PMT anode follows the current shape, i.e. the PMT is operated in pulsed current mode. On the other hand, condition $\tau \gg 1/\omega_T$ is equivalent to say that the integration band of the integrator is much higher than the bandwidth of the input signal, as discussed above. From (4.138) it is straightforward to compute the inverse Laplace transform and of to compute the integrator's output $v_{oD}(t)$:

$$v_{oD}\left(t\right) = -A_{DM} \omega_i^{'} R_{PMT} Q_{MIP} \left(1 - e^{-\frac{t}{\tau}} \right) \qquad (4.139)$$

For $t \gg \tau$ expression (4.139) shows that the integrator's output is just proportional to the total charge generated by a MIP signal at the PMT output ($\int_0^\infty i_{PMT}\left(t\right) \equiv -Q_{MIP}$), i.e. the preamplifier and the integrator work as a charge sensitive preamplifier since at the end, the voltage at the PMT anode, which in current pulsed mode is proportional to pulse current, is integrated. Although the measurement time in the LHCb experiment is 25 ns (about 2τ) the integrators output is still proportional to the collected charge, and we are able to define a charge "gain" G_Q for the ASD:

$$G_Q \equiv \frac{v_{oD}\left(t=T_m\right)}{-Q_{MIP}} \simeq A_{DM} \omega_i^{'} R_{PMT} \left(1 - e^{-\frac{T_m}{\tau}} \right)_{T_m=25ns} \qquad (4.140)$$

The term of (4.140) corresponding to integrator's gain is

$$G_{Q\_Int} \equiv \frac{v_{oD}}{v_{iD}} \simeq \omega_i^{'} \left(1 - e^{-\frac{T_m}{\tau}} \right)_{T_m=25ns} \simeq \frac{1}{R_E C_f} \left(1 - e^{-\frac{T_m}{\tau}} \right)_{T_m=25ns} \qquad (4.141)$$

Figure 4-45 shows the response of the integrator (V_{oD}) to a typical MIP pulse (V_{iD}) with statiscal fluctuations due to small number of photoelectrons. The simulated output signal is V_{oD} for the first clock cycle and V_{oD2} for the next cycle. It fits quite well with the ideal integral of V_{iD}, the waveform V_{oD_teo}. V_{oD_teo} is the integral of V_{iD} times the charge gain G_Q: $V_{oD\_teo} = G_Q \int V_{iD}$.

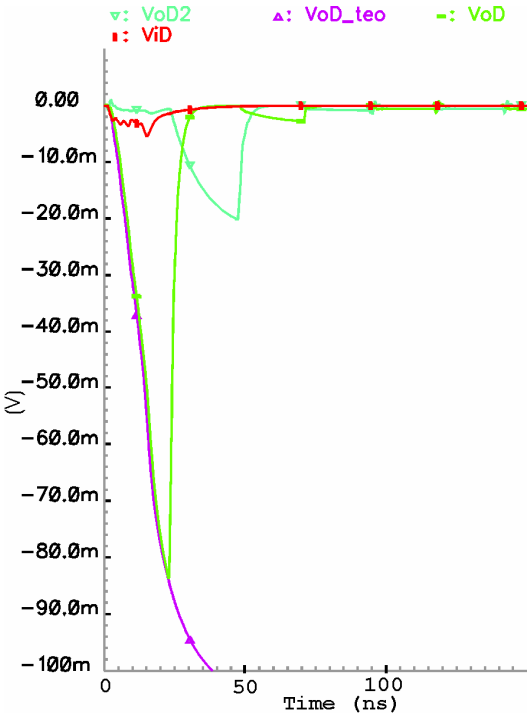

Figure 4-45. Integrator response to a typical MIP pulse. V_{iD} is the DM input, V_{oD} is the DM output in the period of the input pulse arrival, V_{oD2} is the DM output in the next clock cycle and V_{oD_teo} is the integral of V_{iD} times G_Q.

4.2.2.4 Integrator linearity

The linearity error is required to be below 5 % (3.3.6). Although it can be corrected through calibration, it is important to specify an upper limit in order to maintain the dynamic range for the tail correction system and to make easier this calibration. The linearity of the integration depends on the input transconductor and on the closed-loop current integration stage. As the open loop gain of the FDOA is high enough, the later depends mainly on the linearity of the feedback capacitors (C_1-C_2), which are poly1 to poly2 capacitors and according to [73] the variation of such capacitance as a function of voltage is

$$\frac{\partial C}{\partial V}\frac{1}{C\big|_{V=0}} < 0.032\,\% \qquad (4.142)$$

The former has been studied in section 0, being better than 0.02 % of signal range. According to Spectre simulations the linearity error of the integrator is below 0.1 %.

4.2.2.5 Reset state of the integrator

The integrator is a time-varying network with two states: integration and reset. So far, the integration state has been analyzed. Concerning the reset, the key point is the design of the reset switches in Figure 4-21. To minimize the clock feed-through a CMOS switch is implemented. The nMOS and the pMOS transistors have the same size to introduce the same parasitic capacitance and they are driven by two complementary clocks. The clock controlling the switches is a differential one, working between 0 and -1.65 V for pMOS transistors and between 0 and +1.65 V for nMOS transistors. The feedthrough caused by the rising edge of the nMOS clock tends to cancel out with the feedthrough caused by the simultaneous falling edge of the pMOS clock. The use of complementary clocks between 0 V and ±1.65 V also allows reducing the excursion and minimising the interference generation of the clock distribution lines. For 0 V all switch transistors are off, provided that input and

output nodes of the integrator are between about +1V and -1V (i.e. 2V of differential range). If during the integration period the differential output amplitude gets bigger than ±2 V, the switches enter in conduction, acting as an output voltage limiter.

Of course, the conduction resistance of the reset switches has to be designed to optimise the discharge of the feedback capacitors. However, this is not an issue because a minimum size transistor would be enough to discharge an 1 pF capacitor in less than 10 ns.

The conduction resistance (r_{ON}) of the MOS transistors of the switches introduces some residual amplification in the reset state. It can be found the transfer function of the integrator in the reset state is, within the bandwidth f_T:

$$\frac{v_{oD}}{v_{iD}} \simeq \frac{1}{2}\frac{r_{ON}}{R_E} \tag{4.143}$$

Requirement of having a residual output at the end of reset state lower than the 5 % of the integral of the tail of the signal between 25 and 50 ns, leads to a r_{ON} of about 200 Ω, and thus the size of MOS switch transistors is fixed: W=20 μ and L=0.8 μ.

4.2.2.6 Integrator stability

The return ratio or open loop gain of the DM feedback loop of the integrator must be analyzed to assure the stability. As the integrator is a time variant circuit the two states must be analyzed.

4.2.2.6.1 Integration state

If the FDOA is modelled as a voltage controlled voltage source of gain $G_{DM}(s)$, with infinity input impedance and zero output impedance the DM half circuit for the integration state can be drawn as shown in Figure 4-46.

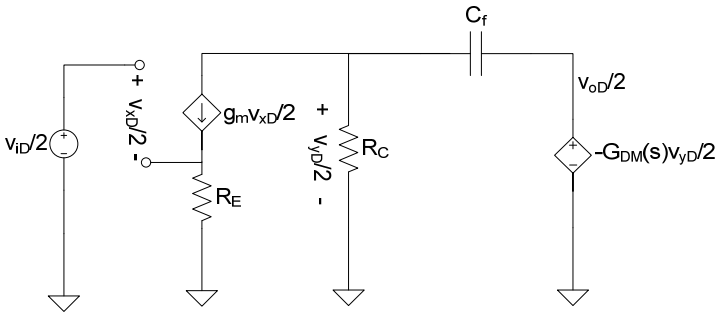

Figure 4-46. DM half circuit for the integration state of the integrator.

In terms of two-port representations it is a shunt-shunt feedback and it can be readily shown [66] that the amplifier's gain is,

$$a(s) \simeq -G_{DM}(s)\left(R_C \,//\, Z_f\right) \tag{4.144}$$

with $Z_f = 1/sC_f$ and the gain of the feedback network is,

$$\beta(s) \simeq -\frac{1}{Z_f} \tag{4.145}$$

Thus the feedback loop gain is,

$$T(s) = a(s)\beta(s) \simeq G_{DM}(s)\frac{Z_f}{Z_f + R_C} \tag{4.146}$$

Expression (4.146) can also be derived using the return ratio technique, changing the dependent source that models the FDOA gain by an independent source of value $-G_{DM}(s)$ and finding the voltage signal generated across R_C with v_{iD} set to zero.

The FDOA can be approximated by a two-pole and one zero transfer function,

$$G_{DM}(s) = G_{DM0}\frac{p_d p_{nd}}{z}\frac{(s+z)}{(s+p_d)(s+p_{nd})} \qquad (4.147)$$

where dominant pole is $p_d \simeq \frac{GBW}{G_{DM0}} \simeq -\frac{G_{MQ1}}{G_{DM0}C_C}$, non-dominant pole is $p_{nd} \simeq -\frac{g_{mM2}}{C_{nd}}$ and zero is $z^{-1} = \left(\frac{1}{G_{MDAR}} - R_Z\right)C_C$ (see section 4.2.2.2.2). Combining expression (4.146) and (4.147) we obtain,

$$T(s) = \frac{G_{MQ1}}{C_C}\frac{g_{mM2}}{C_{nd}}\left(\frac{1}{G_{MDAR}} - R_Z\right)C_C \frac{s\left(s + \frac{1}{\left(\frac{1}{G_{MDAR}} - R_Z\right)C_C}\right)}{\left(s + \frac{G_{MQ1}}{G_{DM0}C_C}\right)\left(s + \frac{g_{mM2}}{C_{nd}}\right)\left(s + \frac{1}{R_C C_f}\right)} \qquad (4.148)$$

The DM loop gain T(s) has a zero at the origin due to the capacitive feedback, the LHP introduced for the frequency compensation of the FDOA and three poles. Two of the poles are just the most significant poles of the FDOA, $p_d \approx 2\pi 5$ kHz and $p_{nd} \approx 2\pi 200$ MHz. The other one is $1/R_C C_f \simeq 2\pi 26\,MHz$, with R_C=4k6 Ω and C_f=1.32 pF. To compute the PM the unity gain frequency must be derived, from expression (4.148) it can be shown that it is approximately the GBW of the FDOA,

$$s\big|_{|T(s)|=1} = \frac{G_{MQ1}}{C_C} \simeq GBW_{FDOA} \qquad (4.149)$$

Considering that the phase shift of the p_{nd} and the one of the z cancel out, the PM is given by,

$$PM \equiv \varphi\left(T\left(j\omega_T\right)\right) + 180^\circ \simeq\big|_{\omega_T \simeq 2\pi GBW} 90 - \arctan\left(\frac{2\pi GBW}{p_d}\right) - \arctan\left(\frac{2\pi GBW}{1/R_C C_f}\right) + 180^\circ \qquad (4.150)$$

A PM margin of 100º is obtained for a GBW of about 150 MHz. The PM is about the same of the FDOA in unity gain closed loop operation, main difference is due to the difference between the positive phase shift introduced by the zero at the origin and the negative one introduce by the pole $1/R_C C_f$.

The return ratio can be studied through AC simulations; in that case it is not necessary to maintain the loop for DC as it was for the CMFB circuit because the operating point of the amplifier is independent of the DM feedback. The loop is broken at the FDOA differential outputs: a signal is injected to the feedback capacitor and the differential output is studied. The FDOA outputs must be terminated with the same impedance seen before breaking the loop, the easiest solution is to connect the feedback network and R_C as shown in Figure 4-47.

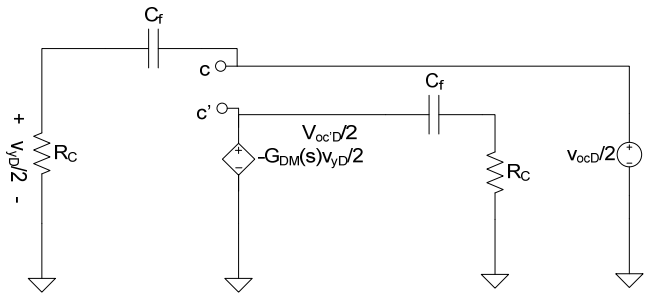

Figure 4-47. DM half circuit for measuring the return ratio of the DM feedback.

Simulation results for the return ratio $T(s)=v_{oc'D}/v_{ocD}$ are shown in Figure 4-48, together with the asymptotes derived of expression (4.148). Results are in good agreement with hand calculations, and the PM is about 100º as expected.

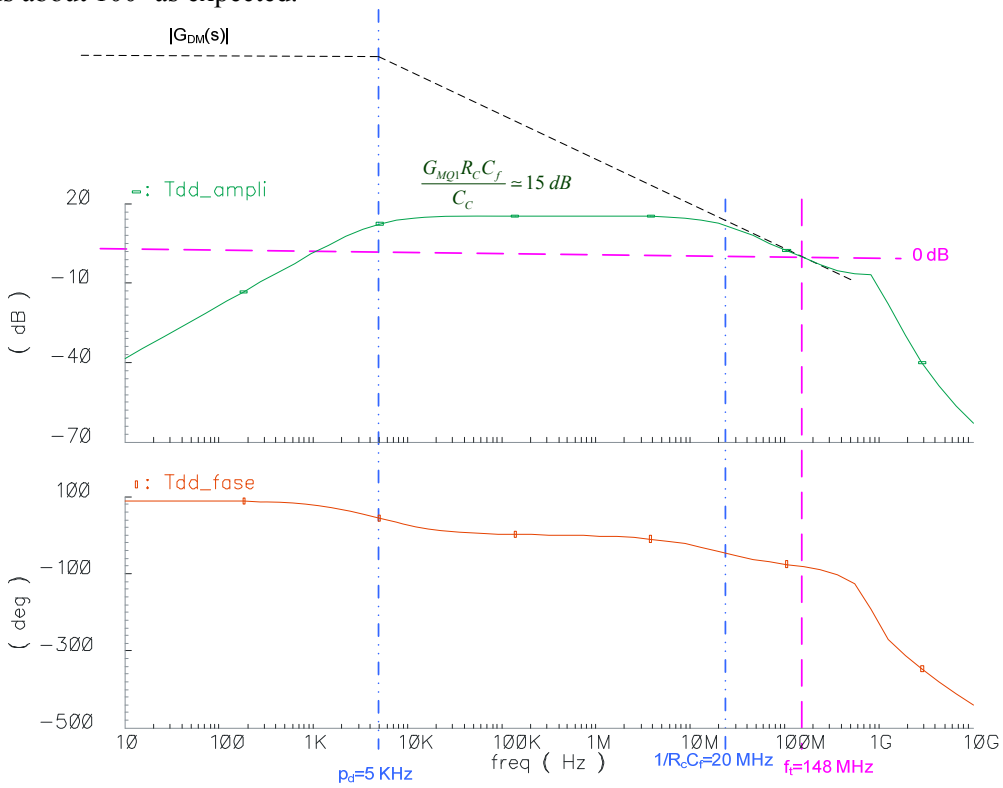

Figure 4-48. AC simulation results for the loop gain of the DM feedback (integration).

4.2.2.6.2 Reset state

Following the same procedure the DM half circuit for the reset state can be drawn as shown in Figure 4-49. R_{ONE} and R_{ONF} are the on resistance of the reset switches.

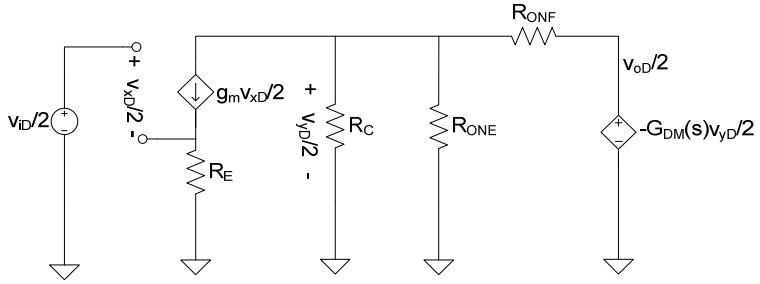

Figure 4-49. DM half circuit for the reset state of the integrator.

The feedback can be regarded either as a shunt-shunt configuration as in previous section or a series-shunt configuration, if the transconductance of the input stage is neglected and the "input" signal of the reset state is considered to be the ground where R_C and R_{ONE} are connected. In any case if $R_C//R_{ONE} \approx R_{ONE}$ the feedback gain is,

$$\beta = \frac{R_{ONE}}{R_{ONE} + R_{ONF}} \tag{4.151}$$

And the loop gain is,

$$T(s) = \frac{1}{2}\frac{G_{MQ1}}{C_C}\frac{g_{mM2}}{C_{nd}}\left(\frac{1}{G_{MDAR}} - R_Z\right)C_C \frac{\left(s + \frac{1}{\left(\frac{1}{G_{MDAR}} - R_Z\right)C_C}\right)}{\left(s + \frac{G_{MQ1}}{G_{DM0}C_C}\right)\left(s + \frac{g_{mM2}}{C_{nd}}\right)} \tag{4.152}$$

It can be easily shown that the GBW of the loop gain with a feedback gain of 1/2 is half of the GBW of the FDOA,

$$s\Big|_{|T(s)|=1} = \frac{1}{2}\frac{G_{MQ1}}{C_C} \simeq \frac{1}{2}GBW_{FDOA} \tag{4.153}$$

Considering that the phase shift of the p_{nd} and the one of the z cancel out, the PM is given by,

$$PM \equiv \varphi\left(T\left(j\omega_T\right)\right) + 180^\circ \simeq \Big|_{\omega_T = 2\pi \frac{1}{2} GBW_{FDOA}} - \arctan\left(\frac{2\pi \frac{1}{2} GBW_{FDOA}}{p_d}\right) + 180^\circ \tag{4.154}$$

A PM margin of 90º is obtained for a unity gain frequency of the feedback loop of about 75 MHz. The PM is a bit higher than the one of the FDOA in unity gain closed loop operation.

The return ratio can be studied breaking the loop in the same way presented for the integration state. Simulation results for the return ratio T(s) are shown in Figure 4-48. Results are in good agreement with hand calculations, the PM is about 95º, the unity gain frequency is 75 MHz, half of the GBW of the FDOA, and the low frequency gain is 81.75 dB ($1/2G_{DM0}$=83.5 dB).

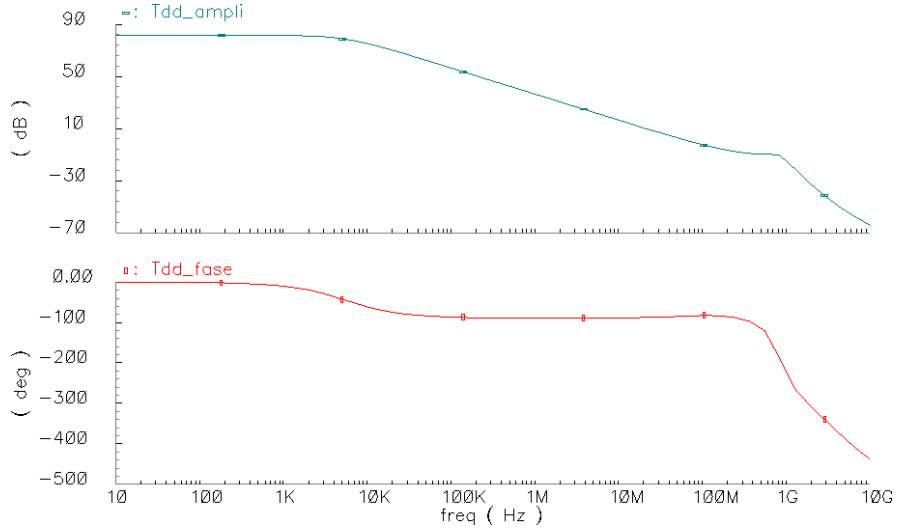

Figure 4-50. AC simulation results for the loop gain of the DM feedback (reset).

4.2.2.7 Temperature coefficient of integrator's "gain"

The pseudo-gain of the integrator for a MIP pulse is defined in (4.141), to compute the temperature dependence we can neglect the exponential term but the dependence of the input stage on the transconductance of the differential pair has to be taken into account. The "gain" of the integrator is then,

$$G_{Q\_Int} \equiv \frac{g_m}{\left(1+g_m R_E\right) C_f} \tag{4.155}$$

The temperature dependence $\frac{\partial G_{Q\_Int}}{\partial T}$ is

$$\frac{\partial G_{Q\_Int}}{\partial T} = \frac{\partial G_{Q\_Int}}{\partial C_f}\frac{\partial C_f}{\partial T} + \frac{\partial G_{Q\_Int}}{\partial R_E}\frac{\partial R_E}{\partial T} + \frac{\partial G_{Q\_Int}}{\partial g_m}\frac{\partial g_m}{\partial T} \tag{4.156}$$

Using (4.155),

$$\begin{aligned}
\frac{\partial G_{Q_Int}}{\partial C_f} &= -\frac{g_m}{1+g_m R_E}\frac{1}{C_f^2} \simeq\Big|_{g_m R_E \gg 1} -\frac{1}{R_E C_f^2} \\
\frac{\partial G_{Q_Int}}{\partial R_E} &= \frac{-g_m^2}{\left(1+g_m R_E\right)^2 C_f} \simeq\Big|_{g_m R_E \gg 1} -\frac{1}{R_E^2 C_f} \\
\frac{\partial G_{Q_Int}}{\partial g_m} &= \frac{1}{\left(1+g_m R_E\right)^2 C_f} \simeq\Big|_{g_m R_E \gg 1} \frac{1}{g_m^2 R_E^2 C_f}
\end{aligned} \tag{4.157}$$

The effective temperature coefficient for the poly 2 resistors is, according to [73],

$$TC_{RPOLY2} \equiv \frac{1}{R_{T0}}\frac{R_T - R_{T0}}{T - T0} = -0.3\cdot 10^{-3}\left[\frac{1}{\Omega}\right] \tag{4.158}$$

and the temperature coefficient of the poly 1 to poly2 capacitors

$$TC_{CPOLY1\text{–}2} \equiv \frac{1}{C_{T0}}\frac{C_T - C_{T0}}{T - T0} = 0.076\cdot 10^{-3}\left[\frac{1}{F}\right] \tag{4.159}$$

Taking the effective temperature coefficient as nominal temperature coefficient, we obtain

$$\begin{aligned}
\frac{\partial C_f}{\partial T} &= C_f TC_{CPOLY1\text{–}2} \\
\frac{\partial R_E}{\partial T} &= R_E TC_{RPOLY2}
\end{aligned} \tag{4.160}$$

The temperature coefficient for the transconductance is,

$$\frac{\partial g_m}{\partial T} = \frac{\partial g_m}{\partial I_C}\frac{\partial I_C}{\partial T} + \frac{\partial g_m}{\partial V_T}\frac{\partial V_T}{\partial T} = \frac{1}{V_T}\frac{\partial I_C}{\partial T} - \frac{I_C}{V_T^2}\frac{k}{q} \tag{4.161}$$

and using previous expressions,

$$\frac{\partial G_{Q\_Int}}{\partial T} \simeq \frac{1}{R_E C_f}\left(-TC_{RPOLY2} - TC_{CPOLY1\text{–}2} + \frac{1}{g_m^2 R_E}\left(\frac{1}{V_T}\frac{\partial I_C}{\partial T} - \frac{I_C}{V_T^2}\frac{k}{q}\right)\right) \tag{4.162}$$

As $G_{Q\_Int} \simeq\Big|_{g_m R_E \gg 1} \frac{1}{R_E C_f}$ the temperature coefficient for integrator's "gain" is

$$TC_{G_{Q\_Int}} \equiv \frac{1}{G_{Q\_Int}} \frac{G_{Q\_Int}}{\partial T} \simeq -TC_{RPOLY2} - TC_{CPOLY1-2} + \frac{1}{g_m^2 R_E}\left(\frac{1}{V_T}\frac{\partial I_C}{\partial T} - \frac{I_C}{V_T^2}\frac{k}{q}\right) \quad (4.163)$$

The current source is a based on band-gap reference, being the $\frac{\partial I_C}{\partial T} \simeq 200 \ \frac{\text{nA}}{\text{K}}$. V_T is 26 mV at 300 K, the collector current I_C is $I_{bias}/2$=360 µA, q is the electron charge $q=1.6\cdot10^{-19}$ C and $k=1.38\cdot10^{-23}$ J/K is the Boltzmann's constant. Then, $TC_{G_{Q\_Int}} \simeq -122 \ \frac{\text{ppm}}{\text{K}}$. According to Spectre simulations the temperature coefficient of the integrator: $TC_{G_{Q\_Int}} \simeq -150 \ \frac{\text{ppm}}{\text{K}}$.

4.2.2.8 Layout

Figure 4-51 shows the layout of the integrator, cell size is 500 µm x 290 µm. Same layout techniques described for the preamplifier are used in order to improve device matching.

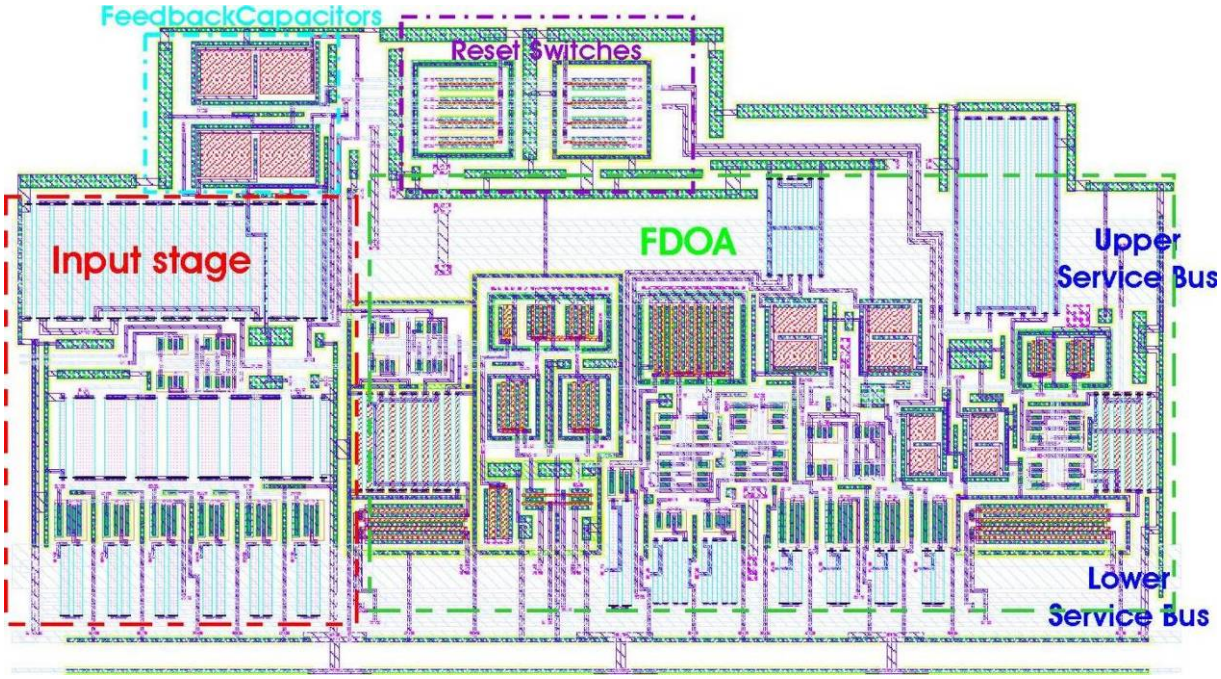

Figure 4-51. Layout of the integrator.

All the cells which are duplicated in each channel (the integrator, the track and hold, the adder and the comparator) include a service bus in the same position to be easily assembled to systematically build a channel. The service bus is split into two parts. Most of the active devices are placed between both buses, although sometimes a few elements are placed over the upper one. The buses include:

- Three independent bipolar supply lines to minimize the common mode interference:
  - Analogue supply (*Veea, Vcca)* and reference (*gnda*).
  - Digital supply (*Vdd,Vss*).
  - Clock distribution and generation system supply (*VccC, VeeC*) and reference *gndC*
- Clock lines, between supply (substrate) lines to obtain some shielding.
- Reference signals for the bias sources.

4.2.3 Track and hold for tunable tail correction

The pile-up compensation or tail correction system takes a fraction of the integrator output at this time (ideally the fraction that would appear in the next period) and stores it on a track and hold circuit. The fraction to subtract is tunable through an analogue control signal, called V_{subD}. The resulting block diagram of the pile-up compensation stage is shown in Figure 4-52. Open loop bipolar voltage buffers are used to duplicate the input signal introducing a common-mode shift between the two replicas. Then, a MOS cross-coupled stage whose transconductance is function of this common-mode shift, serves to adjust the fraction of the signal which is stored in the next stage, a differential track and hold circuit. The MOS transconductor works as input stage of the track and hold circuit. The total current consumption of the stage is 1.5 mA.

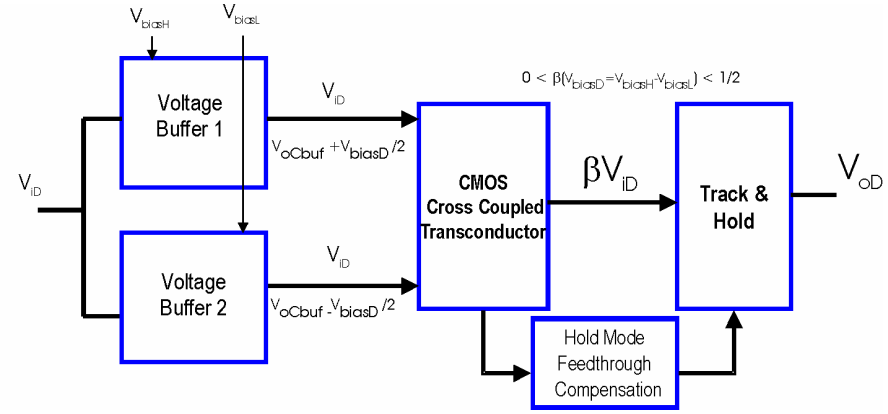

Figure 4-52. Block diagram of the pile-up compensation circuit.

The tunable element is a voltage-controllable linear MOS transconductor based on the bias offset technique [153]. To perform an efficient tracking of the integrator's output the bandwidth of the stage should be higher than 100 MHz. The bias solution proposed in [153] is useful to design an MOS transconductor where a perfectly linear transfer characteristic is obtained from two cross-coupled differential transistor pairs operating in saturation. However, it can be shown that the two voltage shifters in [153] introduce two additional internal nodes resulting in bandwidth limitation. There are several additional proposals to implement the scheme with two cross-coupled pairs (see for example [154] and [155]), but the problem of introducing an offset between the pairs without degrading the bandwidth is always an issue. Here it is adopted a solution, not reported in the literature as far as we are aware, employing an open-loop voltage buffer based on a classical differential stage using linearity compensation.

4.2.3.1 Open loop voltage buffer

The buffer with linearity compensation is shown in Figure 4-53. Its emitter and current source configuration improves the CM input signal range (see Appendix B). The linearization technique is based on a diode connected BJT (D_{1buf}- D_{2buf}). Using KVL on the integrator input an approximating the emitter current by the collector current ($\alpha \approx 1$),

$$V_{iH} - V_{be_{Q1buf}} - \left(I_{c_{Q1buf}} - I_{bias1buf}/2\right)R_{E1buf} + \left(I_{c_{Q2buf}} - I_{bias2buf}/2\right)R_{E2buf} + V_{be_{Q2buf}} - V_{iL} = 0 \qquad (4.164)$$

with $V_{be} = V_T \ln\left(I_C / I_S\right)$. Using the circuit symmetry ($I_{bias1buf} = I_{bias2buf}$ and $R_{E1buf} = R_{E2buf} = R_E$) and defining $\Delta I = I_{c_{Q1buf}} - I_{c_{Q2buf}}$,

$$V_{iD} = R_E \Delta I + V_T \ln\left(\frac{I_{c_{Q1buf}}}{I_{c_{Q2buf}}}\right) \qquad (4.165)$$

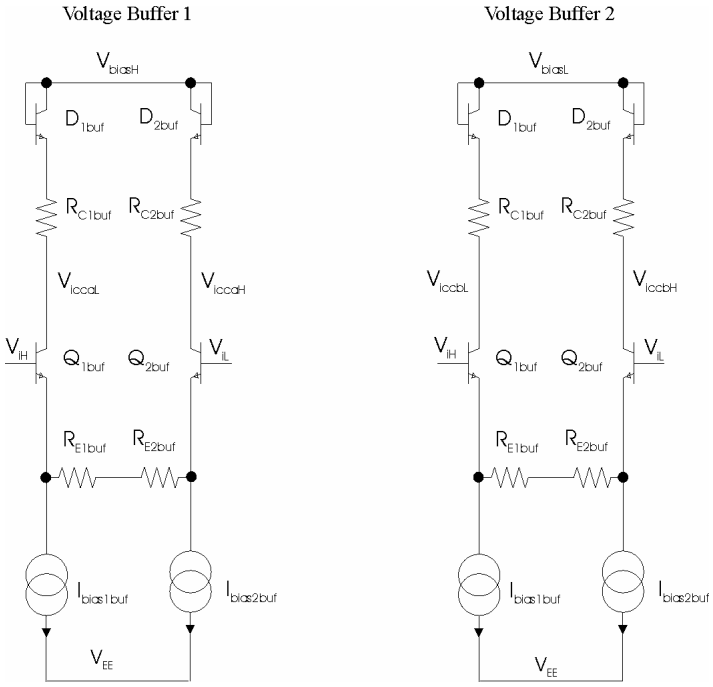

Figure 4-53. Schematic of voltage buffers.

The outputs of the buffer are V_{iccaH} (or V_{iccbH})

$$V_{iccaH} = V_{CC} - V_{be_{D2buf}} - I_{c_{Q2buf}} R_{C2buf} \tag{4.166}$$

and V_{iccaL} (or V_{iccbL})

$$V_{iccaL} = V_{CC} - V_{be_{D1buf}} - I_{c_{Q1buf}} R_{C1buf} \tag{4.167}$$

Using $V_{be} = V_T \ln\left(\frac{I_C}{I_S}\right)$, the differential output V_{iccaD}= V_{iccaH} - V_{iccaL} is,

$$V_{iccaD} = R_C \Delta I_1 - V_T \ln\left(\frac{I_{c_{Q2buf}}}{I_{c_{Q1buf}}}\right) \tag{4.168}$$

Combining (4.165) and (4.168) we found that the transfer function is linear as long as R_C and R_E are approximately equal.

$$V_{iccaD} = \frac{R_C}{R_E} V_{iD} - V_T \ln\left(\frac{I_{c_{Q2buf}}}{I_{c_{Q1buf}}}\right) + \frac{R_C}{R_E} V_T \ln\left(\frac{I_{c_{Q2buf}}}{I_{c_{Q1buf}}}\right) \simeq \Big|_{R_C = R_E} \frac{R_C}{R_E} V_{iD} \tag{4.169}$$

In this design other constraints make this condition impossible, however as long as $I_{bias1buf} \gg \Delta I$ the linearity error will be small (see 4.2.1.1), this will be achieved using a high R_E.

The common mode shift is created just introducing some offset (V_{biasD}=V_{biasH}-V_{biasL}) between the positive rails of the voltage buffers. From Figure 4-53 the common mode voltage at the output of each voltage buffer is,

$$\begin{aligned} V_{oC\_buf1} &\equiv \frac{V_{iccaH} + V_{iccaL}}{2} = V_{biasH} - V_{be\_Dbuf(ON)} - \frac{I_{biasbuf}}{2} R_{Cbuf} \\ V_{oC\_buf2} &\equiv \frac{V_{iccbH} + V_{iccbL}}{2} = V_{biasL} - V_{be\_Dbuf(ON)} - \frac{I_{biasbuf}}{2} R_{Cbuf} \end{aligned} \tag{4.170}$$

Where $V_{be\_Dbuf(ON)}$ is the base to emitter conduction voltage of the diode connected transistor, $I_{biasbuf}$ is the bias current of the stage and R_{Cbuf} is the resistor between the collector of the transistor (Q_{1buf}-Q_{2buf}) of differential pair and the diode connect one. Then the difference of the CM voltage is just V_{biasD} as long as all the components are properly matched.

The most relevant design parameters of this kind of voltage buffers are the emitter resistor R_{Ebuf}, the collector resistor R_{Cbuf} and the DC bias current $I_{biasbuf}$. There several design constraints for these parameters. First, for a DC coupled system, such the ASD, defining the input/output DM and CM signal range of every block is crucial. The upper limit for any input signal is given by the condition of operating the BJTs of the differential pair in the forward-active region

$$V_{iC} + \frac{V_{iD(MAX)}}{2} \le V_{biasX} - I_{biasbuf} R_{Cbuf} - V_{be\_Dbuf(ON)} + V_{be\_Q1buf(ON)} - V_{ce\_Q1buf(SAT)} \quad (4.171)$$

where $V_{be\_Q1buf(ON)}$ and $V_{ce\_Q1buf(SAT)}$ are the base to emitter conduction voltage and the collector to emitter saturation voltage of Q_{1buf} respectively. The lower limit for the input voltage is given by the minimum voltage drop required by the bias current source $V_{Ibias\_buf(MIN)}$

$$V_{iC} - \frac{V_{iD(MAX)}}{2} \ge V_{be\_Q1buf(ON)} - V_{Ibias\_buf(MIN)} + V_{EE} \quad (4.172)$$

The input differential range $V_{iD(MAX)}$ should be ±1V, the differential output range of the integrator. It can be shown that,

$$V_{iD(MAX)} \le 2 I_{biasbuf} R_{Ebuf} \quad (4.173)$$

and the differential voltage gain of the stage is,

$$G_{buf1} \equiv \frac{V_{iccaH} - V_{iccaL}}{V_{iD}} \simeq \Big|_{g_{mQ1buf} R_{Ebuf} \gg 1} \frac{R_{Cbuf}}{R_{Ebuf}} \quad (4.174)$$

The pile-up compensation attenuates the signal to store it in the track and hold part (the gain ranges from 0 to 0.5); part of the attenuation can be introduced in the voltage buffer. This is useful to minimize the excursion of the signal at the input of the cross-coupled transconductor; thus minimizing the linearity error as will be seen later.

Considering all the constraints and trying to minimize the power consumption, the values of the components are chosen R_{Ebuf}= 4k5 Ω, R_{Cbuf}= 1k6 Ω and $I_{biasbuf}$ = 120 μA.Using this values we obtain,

$$-0.1 \le V_{iC} \le 0.2 \quad (4.175)$$

This is compatible with the CM of the integrators output voltage, which is set to 0 through the reference input of the CMFB of the FDOA.

The bandwidth of this kind stage easily reaches few hundreds of MHz, which is more than enough, as can be seen from direct extrapolation of the small-signal analysis of the preamplifier. The only high impedance node is the collector of (Q_{1buf}-Q_{2buf}). The capacitance in such node is of the order of hundreds of fF, with an R_{Cbuf} of 4k5 Ω, the time constant is a few nanoseconds and the bandwidth of hundreds of MHz.

4.2.3.2 Cross-coupled transconductor

Now we will analyze the operation of the cross-coupled transconductor shown in Figure 4-54. First, all MOSFETs are assumed to operate in their saturation region and have their bulks connected to their sources. Thus, their drain currents I_D can be characterized to first order by

$$I_D = k_n \left(V_{gs} - V_t \right)^2 \quad (4.176)$$

where V_{gs} is the gate to source voltage, V_t is the threshold voltage, $k_n = k_{0n} W/L = 0.5 \mu_n C_{ox} W/L$ is the transconductance parameter of a MOS, and μ_n, C_{ox}, W, L are the n region mobility, the oxide

capacitance per unit area, the channel width and the channel length, respectively. The body effect, the effect of channel length modulation and other second-order effects are neglected in this analysis. The influence of these effects on the OTAs transfer characteristics are shown via Spectre simulation.

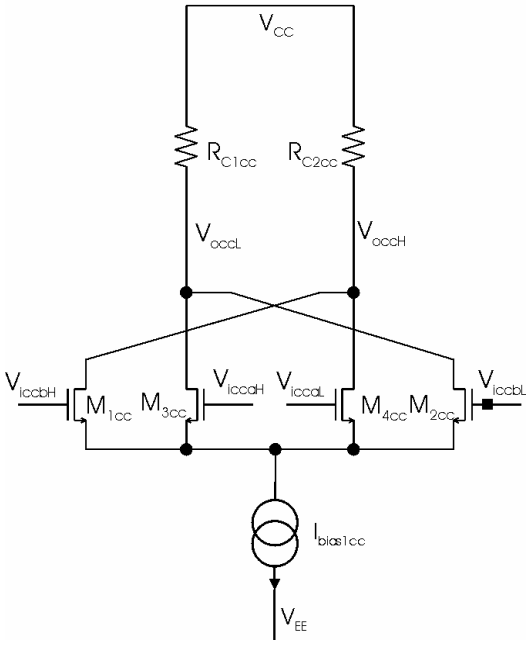

Figure 4-54. Schematic of the cross-coupled transconductor.

The DM voltage at the output of the transconductor is,

$$V_{occD} = V_{occH} - V_{occL} = I_{R_{C2cc}} R_{C2cc} - I_{R_{C1cc}} R_{C1cc} = \Big|_{R_{C1cc}=R_{C1cc}=R_{Ccc}} R_{Ccc}\left(I_{R_{C2cc}} - I_{R_{C1cc}}\right) \quad (4.177)$$

and the currents across collector resistors are

$$\begin{aligned} I_{R_{C1cc}} &= I_{DM3} + I_{DM2} = k_n\left(V_{gsM3} - V_t\right)^2 + k_n\left(V_{gsM2} - V_t\right)^2 \\ I_{R_{C2cc}} &= I_{DM1} + I_{DM4} = k_n\left(V_{gsM1} - V_t\right)^2 + k_n\left(V_{gsM4} - V_t\right)^2 \end{aligned} \quad (4.178)$$

with

$$\begin{aligned} V_{gsM1} &= V_{iccbH} - V_s \\ V_{gsM2} &= V_{iccbL} - V_s \\ V_{gsM3} &= V_{iccaH} - V_s \\ V_{gsM4} &= V_{iccaL} - V_s \end{aligned} \quad (4.179)$$

Taking into account that the DM at both input pairs is the same and equal to DM input of the voltage buffers $V_{iccaD} = V_{iccbD} = V_{iD}$ and that the CM difference of both input pairs is $V_{iccaC} - V_{iccbC} = V_{biasD}$.Then the quadratic terms are cancelled and linear relation between the DM input of the pile-up compensation stage and the output of the cross-coupled transconductor is obtained

$$V_{occD} = 2R_{Ccc}k_n V_{biasD} V_{iD} \quad (4.180)$$

Furthermore, the gain is linearly controlled through the differential voltage V_{biasD}:

$$G_{cc}\left(V_{biasD}\right) = \frac{V_{occD}\left(V_{biasD}\right)}{V_{iD}} = 2k_n R_{Ccc} V_{biasD} \quad (4.181)$$

As said before the whole gain range of the pile-up compensation system must be:

$$0 \le G_{buf} G_{cc}\left(V_{biasD}\right) \le 0.5 \quad (4.182)$$

Expression (4.180) is valid provided that all MOS transistors are in the forward active region. The limit case is for the transistor with a gate voltage equal to the threshold voltage. As the cross-coupled transconductor is fully symmetrical, i. e. all the MOS transistors do have the same channel width (W) and length (L), if we suppose that any transistor, for instance M_{1CC}, is in this situation ($V_{gs_{M1CC}} = V_t$ and by definition $I_{ds_{M1CC}} = 0$), the conclusions of the analysis will be valid for any situation. Gate voltage of transistor M_{1CC} is V_{biasD} higher[s] than gate voltage of M_{3CC} ($V_{gs_{M3CC}} = V_t + V_{biasD}$). In the same way, gate voltage of transistor M_{2CC} is V_{biasD} higher than gate voltage of M_{4CC}. Thus, using KCL in the node corresponding to the source of MOS transistors,

$$\begin{aligned} I_{bias1CC} &= I_{dsM1CC} + I_{dsM2CC} + I_{dsM3CC} + I_{dsM4CC} \\ I_{bias1CC} &= 0 + k_n\left(V_{gsM2CC} - V_t\right)^2 + k_n\left(V_{biasD}\right)^2 + k_n\left(V_{gsM2CC} + V_{biasD} - V_t\right)^2 \end{aligned} \quad (4.183)$$

The cross-coupled transconductor input DM voltage is by definition: $V_{iccD} = V_{gsM1CC} - V_{gsM2CC} = V_{gsM3CC} - V_{gsM4CC}$. In the case of study the DM input voltage, which is the modulus of the maximum input DM voltage $|V_{iccDmax}|$ is, taking into account that $V_{gs_{M1CC}} < V_{gs_{M2CC}}$

$$\left|V_{iccD\max}\right| = V_{gs_{M2CC}} - V_{gs_{M1CC}} = V_{gs_{M2CC}} - V_t \quad (4.184)$$

Using this result in (4.183), a second order expression function of $|V_{iccDmax}|$ is obtained,

$$0 = \left|V_{iccD\max}\right|^2 + V_{biasD}\left|V_{iccD\max}\right| + V_{biasD}^2 - \frac{I_{bias1cc}}{2k_n} \quad (4.185)$$

Equation (4.185) has two solutions,

$$\left|V_{iccD\max}\right| = -\frac{V_{biasD}}{2} \pm \sqrt{\frac{I_{bias1cc}}{2k_n} - \frac{3}{4}V_{biasD}^2} \quad (4.186)$$

By definition $|V_{iccDmax}|$ is a positive value, therefore a fundamental design equation, in agreement with literature [154], is obtained for the input DM range in which the stage works linearly:

$$V_{iccD} < \sqrt{\frac{I_{bias1cc}}{2k_n} - \frac{3}{4}V_{biasD}^2} - \frac{V_{biasD}}{2} \quad (4.187)$$

Temperature derives of feedback circuits or stages such the open-loop voltage buffer are usually controlled through the ratio of two components with similar temperature coefficient (if possible same type device, e.g. resistors made of the same polysilicon type) which tend to cancel one to the other. Conversely, from (4.181) it becomes clear that the TC of the gain of this stage, provided that the controlling signal V_{biasD} is stable with temperature, depends on the TC of the transconductance parameter and on the TC of the poly resistor R_{Ccc}. The former depends on the TC of the n region mobility; according to [161] some empirical equations are used in MOS models to describe the dependence of the mobility on the temperature:

$$\mu_n = \mu\left(T = 300\ K\right)\left(\frac{300}{T}\right)^{3/2} \quad (4.188)$$

Using (4.188) an approximated value for the TC of the transconductance parameter is -3000 ppm/K. We chose to implement R_{Ccc} as a poly1 resistor, because it has a positive TC (+1000 ppm/K) that will partially cancel the variation of the k_n parameter. According to Spectre simulations the TC of the gain stage is – 0.15%/K using a poly1 resistor for R_{Ccc} whereas it would be -0.4%/K using a poly 2 resistor.

[s] V_{biasD} shifth can be positive or negative. However, in in this case we suppose that M_{1CC} is in the limit of the cut-off region and that other transistors are in saturation region, therefore the value of V_{gsM1CC} must be the minimum gate voltage.

Some dependence of the TC on the W/L ratio of the MOS transistors has been observed through simulations and minimizing the TC of the stage has been an additional design constraint. However, many parameters of MOS transistors, such as the threshold voltage, vary with temperature, making difficult to maintain a reasonable fit between measured and simulated data across a wide temperature range. Taking into account these uncertainties and the relatively high TC of the stage, it will be very important to measure accurately its temperature dependence.

Another design constraint of the transconductor V_{occC} is to provide an output CM compatible with the input CM of the track and hold stage:

$$V_{oCC} = V_{CC} - I_{biascc} R_{Ccc} \qquad (4.189)$$

Last design consideration is to achieve a gain bandwidth higher than 100 MHz. As in the case of the voltage buffer there is only one high impedance node, and with R_{Ccc} of a few kΩ it can be easily achieved (for the W and L required).

Taking into account all these considerations the values for design parameters are shown in Table 4-5. The channel length L of the MOS devices is not minimal in order to increase output resistance.

	Value
$I_{bias1cc}$	240 µA
W	40 µm
L	2.6 µm
$R_{C1(2)cc}$	3 kΩ

Table 4-5. Values for the design parameters of the cross coupled transconductor.

4.2.3.3 Differential open loop track and hold stage

The circuit used to store the value that will be subtracted to the next event is an adaptation of a well known fully differential track and hold (T&H) [156], see Figure 4-55.

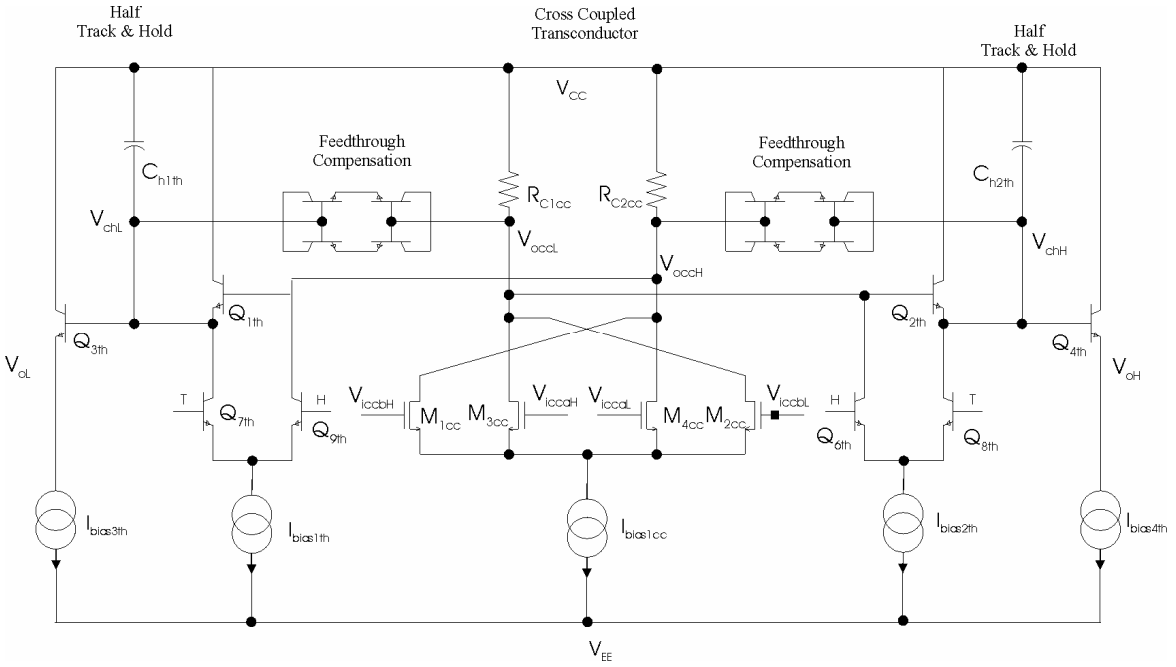

Figure 4-55. Schematic of the track and hold (with the cross-coupled transconductor).

Nevertheless, several adjustments of the classical design are needed. First of all, it is not possible to use the classical input stage [156] (very similar to the bipolar voltage buffer described above) with a supply voltage of 3.3 V due to the voltage drop in diodes for linearity compensation. Although there

are some proposals to overcome this problem using bipolar [157] or CMOS [158] technology, in our design the MOS cross coupled transconductor plays the role of the input stage, providing at the same time a tunable gain and a linear response at 3.3V supply voltage.

The following stage of the T&H is a follower that drives the hold capacitor and that is biased through a fast bipolar current switch controlled by a differential clock (T and H signals) which is derived from the 40 MHz clock (see section 4.5.2). The status of the switch defines the two possible states of the circuit:

a) Track mode. If the voltage in the switch input T is higher than the voltage in the switch input H by at least about $3 \cdot V_T$, i.e. $T\text{-}H > 3 \cdot V_T$ where $V_T = kq/T$, the transistor Q_{6th} (and Q_{9th}) turns off and the bias current $I_{bias2th}$ (and $I_{bias1th}$) flows through the other transistor of the pair Q_{8th} (Q_{7th}). In this situation Q_{2th} and Q_{1th} are properly biased with a current $I_{bias2th}$ and $I_{bias1th}$ respectively, working as emitter followers, and the voltage in the hold nodes (V_{chH} and V_{chL}) and in the differential outputs follow the differential input voltage.

b) Hold mode. If $H\text{-}T > 3V_T$ transistors Q_{2th} and Q_{1th} turn off and the output of the input stage is disconnected from the hold node, where the capacitor voltage before the change in the switch is stored.

In the hold operation mode the bias currents $I_{bias2th}$ and $I_{bias1th}$ flow through the collector resistors R_{C1cc} and R_{C2cc} and there is a limit for these bias current in order to assure that the MOS transistors are not entering in the ohmic region, to work in saturation $V_{gs} - V_t < V_{ds}$ and then $V_t > V_g - V_d$. In the worst case, the maximal input gate voltage is V_{CC}-$V_{be\_Dbuf(ON)}$ and the minimal drain voltage is $V_{CC} - \left(I_{bias1cc} + I_{bias1(2)th}\right) R_{C1(2)cc}$, thus

$$I_{bias1(2)th} < \frac{V_t + V_{be\_Dbuf(ON)} - I_{bias1cc} R_{C1(2)cc}}{R_{C1(2)cc}} \tag{4.190}$$

In the hold operation the base to emitter diodes of the transistors Q_{2th} and Q_{1th} must never enter in conduction. Then, the maximum voltage at the base to emitter junction of Q_{2th} and Q_{1th} in hold operation $V_{CC} - I_{bias1(2)th} R_{C1(2)cc}$ must be smaller than the minimum voltage at the hold nodes (V_{chH} and V_{chL}) $V_{CC} - I_{bias1(2)th} R_{C1(2)cc} - V_{beQ1(2)th(ON)}$. Then a condition that imposes a lower limit for this bias current is obtained

$$I_{bias1(2)th} > \frac{I_{bias1cc} R_{C1(2)cc} + V_{beQ1(2)th(ON)}}{R_{C1(2)cc}} \tag{4.191}$$

Choosing $I_{bias2th}$ and $I_{bias1th}$ 240 μA fulfills conditions (4.190) and (4.191).

The correct operation of the circuit also imposes some constraints in the level of T and H signals that must be taken into account in the design of the clocking modules:

1) The base to emitter voltage of the active transistors in the switch, Q_{8th} (Q_{7th}) in track operation and Q_{6th} (and Q_{9th}) in hold operation, must be higher than $V_{be(ON)}$ with minimum voltage drop in the current sources $I_{bias2th}$ and $I_{bias1th}$:

$$\begin{aligned} T &> V_{be(ON)} + V_{Ibias1(2)th(MIN)} + V_{EE} \\ H &> V_{be(ON)} + V_{Ibias1(2)th(MIN)} + V_{EE} \end{aligned} \tag{4.192}$$

2) Transistors Q_{8th} and Q_{7th} must not saturate in track operation

$$T < V_{CC} - I_{bias1CC} R_{C1(2)cc} - V_{ce(SAT)} \tag{4.193}$$

3) Transistors Q_{6th} (and Q_{9th}) must no saturate in hold operation

$$H < V_{CC} - \left(I_{bias1cc} + I_{bias1(2)th}\right) R_{C1(2)cc} - V_{ce(SAT)} \tag{4.194}$$

Using typical values we found,

$$-0.5\,V \le T(H) \le 0.6\,V \qquad (4.195)$$

Emitter followers Q_{2th} and Q_{1th} provide high impedance at the hold node and low output impedance. In the original design [156] there is an additional emitter follower between the hold node and the emitter follower working as output buffer, which is controlled through another branch of the differential switch. During the hold mode the tail current of the additional emitter follower is switched off. The common-mode drop of the T&H reduces by a factor 1/β and the usable range of the sample rate improves by this same factor. In track mode the tail current of these emitter followers is switched on in order to secure the settling performance of the output buffer. To operate at a 3.3 V, the additional follower is removed and the tail current of the output buffers ($I_{bias3th}$ and $I_{bias4th}$) is set to 120 μA, as a compromise between the drop rate of the hold signal and settling capabilities in track mode. Indeed, the DM drop rate is determined by the degree of mismatch of the base currents of the output buffers.

This architecture suffers from hold-mode feedthrough. This is feedthrough of the input signal to the hold capacitor during the hold state, caused by a parasitic stray capacitor from the input node to the output node of the switch (the base to emitter parasitic capacitance, C_{be}, of Q_{1th} and Q_{2th}). A compensation circuit, whose capacitance must be equal to the C_{be} of Q_{1th} and Q_{2th} [156], connects an output of the MOS transconductor with the hold node that corresponds to the complementary output; the hold-mode feedthrough is approximately canceled out thanks to the differential architecture.

4.2.3.4 Simulation results

Figure 4-56 shows the DM signals at the relevant points of the circuit when a sinusoidal signal of 3 MHz is applied at the input. The controlling signal V_{subD} of the gain of the circuit is set to 300 mV, i.e. a gain of about 0.25. The T&H is clocked at the standard frequency of 20 MHz. The track and hold phases are clearly visible in the output signal V_{oD}, in the track phase it follows the output of the tunable cross-coupled transconductor (V_{oCCD}) and in the hold phase keeps the last value.

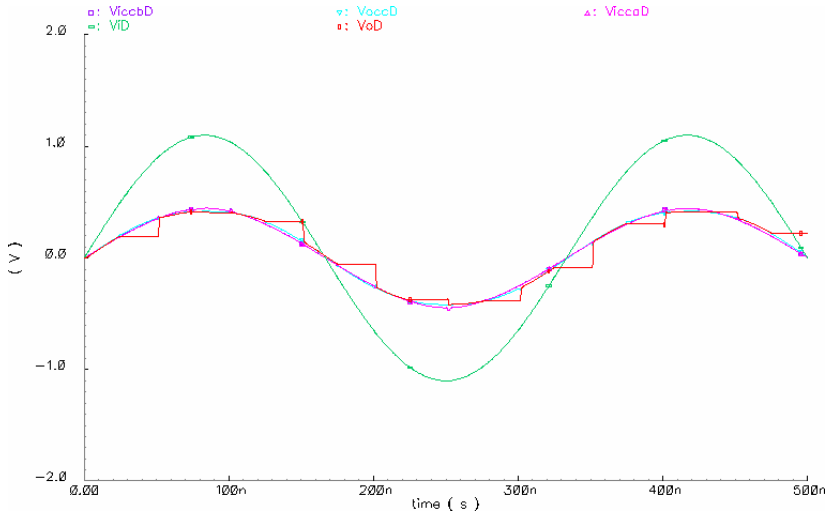

Figure 4-56. Results of transient simulation for a sinusoidal input of 3 MHz with V_{subD} = 300 mV.

Figure 4-57 shows the output of the tunable cross-coupled transconductor (V_{oCCD}) and the output of the whole circuit (V_{oD}) for different values of the gain controlling signal V_{subD}, ranging between -500 mV and + 500 mV (gain between -0.5 V and 0.5 V). The linearity error of the T&H is below 1%. The drop rate in the hold phase is 0.07 mV/ns, i.e. less than 2 mV in 25 ns.

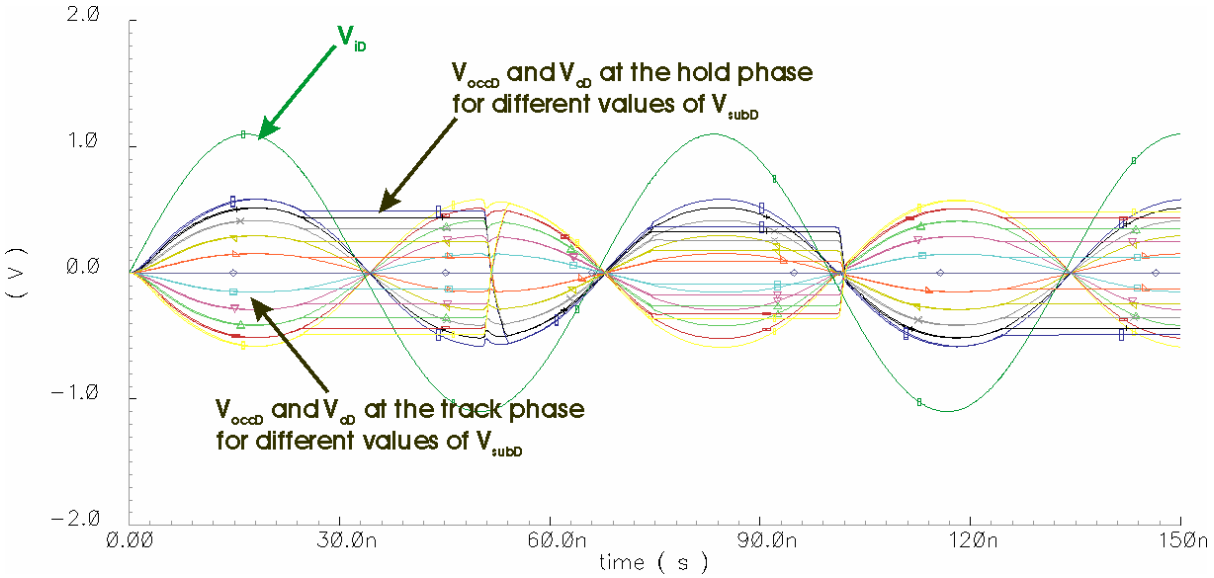

Figure 4-57. Results of transient simulation for a sinusoidal input of 15 MHz with V_{subD} varying between - 500 mV and + 500 mV.

Figure 4-58 shows the frequency response of the cross-coupled transconductor for values of the gain controlling signal V_{subD}, ranging between - 500 mV and + 500 mV. Not only the phase depends on V_{subD}, the signal is inverted (phase is 180º) for negative values of V_{subD} as can be seen also in Figure 4-57. The bandwidth of the stage is 170 MHz (for a typical capacitive load of few hundreds of fF).

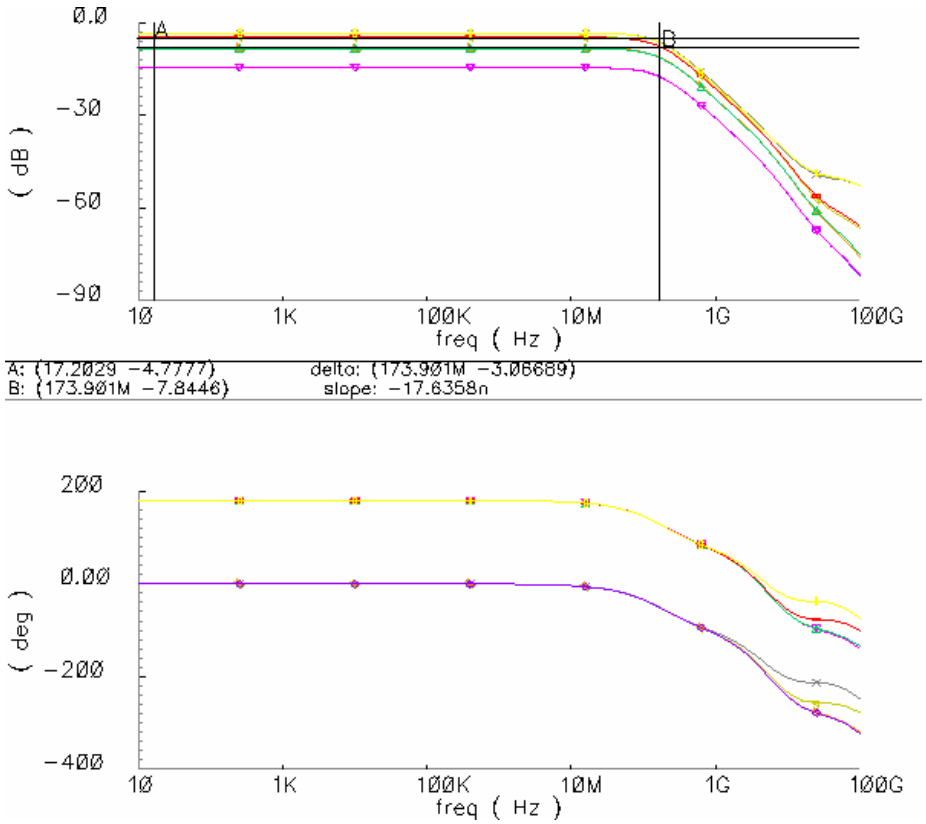

Figure 4-58. Results of the simulation of the frequency response of the cross-coupled transconductor for V_{subD} varying between - 500 mV and + 500 mV. Top: magnitude . Bottom: phase.

4.2.3.5 Layout

Figure 4-59 shows the layout of track and hold circuit, cell size is 260 µm x 230 µm. Same layout techniques described for the preamplifier are used in order to improve device matching. In the case of the cross-coupled transconductor, transistors M_{1cc}, M_{2cc}, M_{3cc} and M_{4cc} must be matched. This is achieved dividing each transistor in four fingers, and arranging the 16 resulting fingers using a common centroid lay out structure. The service bus lines described in the previous sub-sections are also included in this cell.

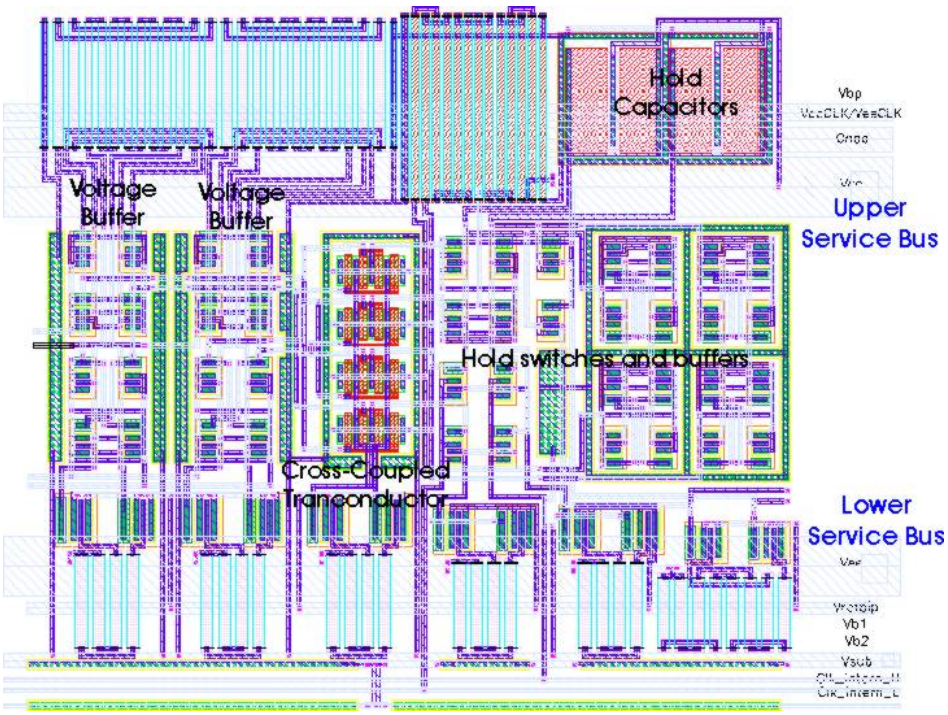

Figure 4-59. Layout of the track and hold circuit.

4.2.4 Open loop addition

The open loop addition is the first step of the comparison. It consist on subtracting the tail correction signal and the threshold from the integrator's output, so that the sign of the output indicates whether the integrated charge, taking into account pile-up compensation, is above threshold or not. Three bipolar differential pairs with emitter degeneration are used to convert the outputs of the integrator, of the DAC and of the pile-up compensation stage to a differential current (see Figure 4-60). Once this is done it is easy to subtract the pile up compensation signal (V_h) and the threshold (V_{th}) to the integrator signal (V_t), just using an inverting configuration for the formers and a non-inverting configuration for the later. The result is converted into a voltage signal using a common collector resistor and linearity compensation (D_{1a}-D_{1b}). The comparator connected at the output of this block evaluates the sign of the result of the addition; after the addition the linearity of the circuit is not important any more. The block also includes an output stage to adjust the output common mode to the comparator requirement (pair Q_{4a}-Q_{4b}) and output buffer (emitter followers Q_{5a} and Q_{5b}). The total current consumption of the stage is 1.2 mA.

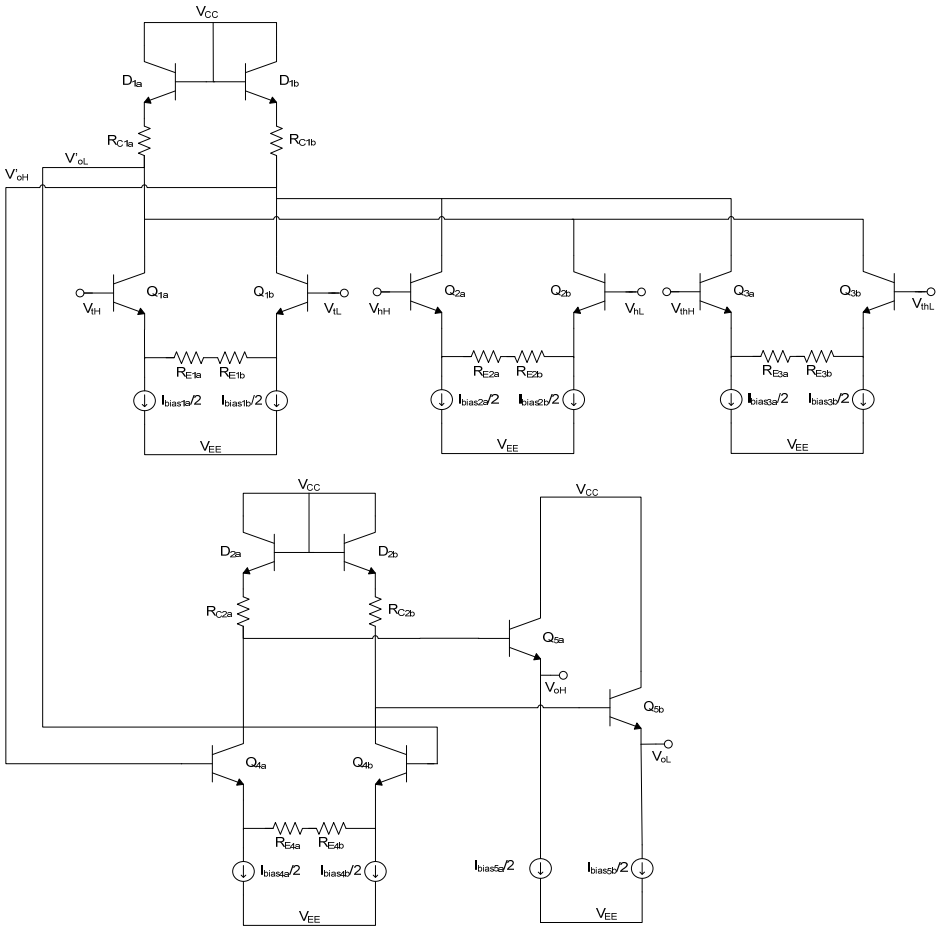

Figure 4-60. Schematic of the open loop addition stage. Addition of input signals at the top and output stage at the bottom.

The open loop addition easily provides high bandwidth (about 300 MHz according to Spectre simulations) but the linearity must be carefully analyzed. Using KVL on the integrator input and approximating the emitter current by the collector current ($\alpha \approx 1$),

$$V_{tH} - V_{be_{Q1a}} - \left(I_{c_{Q1a}} - I_{bias1a}/2\right)R_{E1a} + \left(I_{c_{Q1b}} - I_{bias1b}/2\right)R_{E1b} + V_{be_{Q1b}} - V_{tL} = 0 \quad (4.196)$$

with $V_{be} = V_T \ln\left(I_C / I_S\right)$. Using circuit symmetry ($I_{bias1a} = I_{bias1b}$ and $R_{E1a} = R_{E1a} = R_{E1}$) and defining $\Delta I_1 = I_{c_{Q1a}} - I_{c_{Q1b}}$,

$$V_{tD} = R_{E1}\Delta I_1 + V_T \ln\left(\frac{I_{c_{Q1a}}}{I_{c_{Q1b}}}\right) \quad (4.197)$$

In the same way we obtain for V_h,

$$V_{hD} = R_{E2}\Delta I_2 + V_T \ln\left(\frac{I_{c_{Q2a}}}{I_{c_{Q2b}}}\right) \quad (4.198)$$

and for V_{th},

$$V_{thD} = R_{E3}\Delta I_3 + V_T \ln\left(\frac{I_{c_{Q3a}}}{I_{c_{Q3b}}}\right) \quad (4.199)$$

The outputs of the addition stage are V'_{oH}

$$V'_{oH} = V_{CC} - V_{be_{D1b}} - (I_{c_{Q1b}} + I_{c_{Q2a}} + I_{c_{Q3a}})R_{C1b} \qquad (4.200)$$

and V'$_{oL}$

$$V'_{oL} = V_{CC} - V_{be_{D1a}} - (I_{c_{Q1a}} + I_{c_{Q2b}} + I_{c_{Q3b}})R_{C1a} \qquad (4.201)$$

Using $V_{be} = V_T \ln\left(I_C / I_S\right)$ the differential output V'$_{oD}$= V'$_{oH}$- V'$_{oL}$ is,

$$V'_{oD} = R_{C1}\left(\Delta I_1 - \Delta I_2 - \Delta I_3\right) - V_T \ln\left(\frac{I_{c_{Q1b}} + I_{c_{Q2a}} + I_{c_{Q3a}}}{I_{c_{Q1a}} + I_{c_{Q2b}} + I_{c_{Q3b}}}\right) \qquad (4.202)$$

Last term in (4.202) corresponds to the diode connected transistors, it is the linearity compensation term. Combining equations (4.197), (4.198), (4.199) and (4.202),

$$\frac{V'_{oD}}{R_{C1}} = \frac{V_{tD}}{R_{E1}} - \frac{V_{hD}}{R_{E1}} - \frac{V_{thD}}{R_{E1}} - \frac{V_T}{R_{E1}} \ln\left(\frac{I_{c_{Q1a}}}{I_{c_{Q1b}}}\right) + \frac{V_T}{R_{E1}} \ln\left(\frac{I_{c_{Q2a}}}{I_{c_{Q2b}}}\right) + \frac{V_T}{R_{E1}} \ln\left(\frac{I_{c_{Q2a}}}{I_{c_{Q2b}}}\right) - \frac{V_T}{R_{C1}} \ln\left(\frac{I_{c_{Q1b}} + I_{c_{Q2a}} + I_{c_{Q3a}}}{I_{c_{Q1a}} + I_{c_{Q2b}} + I_{c_{Q3b}}}\right) \qquad (4.203)$$

Defining the common mode in each pair as $I_i = \frac{I_{c_{Qia}} + I_{c_{Qib}}}{2}$ the collector current in each branch of the pair is $I_{c_{Qia}} = I_i + \frac{\Delta I_i}{2}$ and $I_{c_{Qib}} = I_i - \frac{\Delta I_i}{2}$. Using this notation the logarithmic terms of (4.203) corresponding to the transistors of the pairs can be rewritten as $\ln\left(\frac{I_{c_{Qia}}}{I_{c_{Qib}}}\right) = \ln\left(\frac{1 + \frac{\Delta I_i}{2I_i}}{1 - \frac{\Delta I_i}{2I_i}}\right) \simeq\big|_{\frac{\Delta I_i}{2I_i} \ll 1} \frac{\Delta I_i}{I_i}$.

This simplification is based on Taylor series expansion $\ln\left(\frac{1+x}{1-x}\right) = 2\left(x + \frac{x^3}{3!} + \frac{x^5}{5!} + \ldots\right) \simeq\big|_{x \ll 1} 2x$. In the same way: $\ln\left(\frac{I_{c_{Q1b}} + I_{c_{Q2a}} + I_{c_{Q3a}}}{I_{c_{Q1a}} + I_{c_{Q2b}} + I_{c_{Q3b}}}\right) = \ln\left(\frac{1 + \frac{\left(-\Delta I_1 + \Delta I_2 + \Delta I_3\right)}{2\left(I_1 + I_2 + I_3\right)}}{1 - \frac{\left(-\Delta I_1 + \Delta I_2 + \Delta I_3\right)}{2\left(I_1 + I_2 + I_3\right)}}\right) \simeq \frac{-\Delta I_1 + \Delta I_2 + \Delta I_3}{I_1 + I_2 + I_3}$, for the compensation term. Then, (4.203) can be expressed as a linear input-output relationship plus a linearity error term called *LE*:

$$\frac{V'_{oD}}{R_{C1}} = \frac{V_{tD}}{R_{E1}} - \frac{V_{hD}}{R_{E1}} - \frac{V_{thD}}{R_{E1}} + LE \qquad (4.204)$$

where the linearity error is

$$LE = -\frac{V_T}{R_{E1}} \frac{\Delta I_1}{I_1} + \frac{V_T}{R_{E1}} \frac{\Delta I_2}{I_2} + \frac{V_T}{R_{E1}} \frac{\Delta I_3}{I_3} - \frac{V_T}{R_{C1}} \frac{-\Delta I_1 + \Delta I_2 + \Delta I_3}{I_1 + I_2 + I_3} \qquad (4.205)$$

Imposing that linearity error depending on each differential current ΔI_i with ΔI_j=0 ($i \neq j$) is cancelled

$$LE\big|_i = \frac{V_T}{R_{Ei}} \frac{\Delta I_i}{I_i} - \frac{V_T}{R_{C1}} \frac{\Delta I_i}{I_1 + I_2 + I_3} = 0 \qquad (4.206)$$

this leads to the condition

$$\frac{R_{Ei}}{R_{C1}} = \frac{I_1 + I_2 + I_3}{I_i} \qquad (4.207)$$

All the inputs must have the same gain $R_{E1}=R_{E2}=R_{E3}$ and the same DM signal range $V_{iDMAX}= \pm 1V$, the DM signal excursion is limited by the product of emitter resistor and the bias current, thus $V_{iDMAX} \leq R_E I_{biasi}$. As the common mode current I_i is equal to I_{biasi}, according to (4.207), $R_{E1}=R_{E2}=R_{E3}=3R_{C1}$.

In order to operate all the transistors of the input pairs in its forward active region, it is critical to control the input signal range. Transistor Q_i will be in the limit of saturation when the input reaches its maximum level V_{iMAX}:

$$V_{iMAX} = V_{iCMAX} + \frac{V_{iDMAX}}{2} \leq V_{CC} - V_{be\_D1(ON)} - 3I_{bias} - V_{ce\_Qi(SAT)} + V_{be\_Qi(ON)} \quad (4.208)$$

As said before, the input DM signal range is fixed to $V_{iDMAX}= \pm 1V$, therefore constraints will apply on the input CM range, which is improved thanks to a special configuration (see Appendix B). Then the maximum input CM for any input (V_{iCMAX}) is

$$V_{iCMAX} \leq V_{CC} - V_{be\_D1(ON)} - 3I_{bias} - V_{ce\_Qi(SAT)} + V_{be\_Qi(ON)} - \frac{V_{iDMAX}}{2} \quad (4.209)$$

On a similar way the minimum level of an input signal is given by the minimum voltage drop required by the bias current source $V_{Ibias(MIN)}$,

$$V_{iMIN} = V_{iCMIN} - \frac{V_{iDMAX}}{2} \geq V_{be\_Qi(ON)} + V_{Ibias(MIN)} + V_{EE} \quad (4.210)$$

Thus

$$V_{iCMIN} \geq V_{be\_Qi(ON)} + V_{Ibias(MIN)} + V_{EE} + \frac{V_{iDMAX}}{2} \quad (4.211)$$

V_t and V_h inputs are internal; therefore the signal excursion is fixed by design. V_{th} is connected to the internal DAC, whose output range depends on V_{refH} and V_{refL} inputs of the ASIC.

Figure 4-61 shows the result of a transient simulation of the open-loop addition stage. The ideal output follows quite well the ideal response, the discrepancy is due to the phase delay introduced by the first order response of the stage; the dominant pole is at ≈300 MHz and it corresponds to 7º for 30 MHz sine input signal (V_t). Simulations at low frequency show that the linearity error is about 1%.

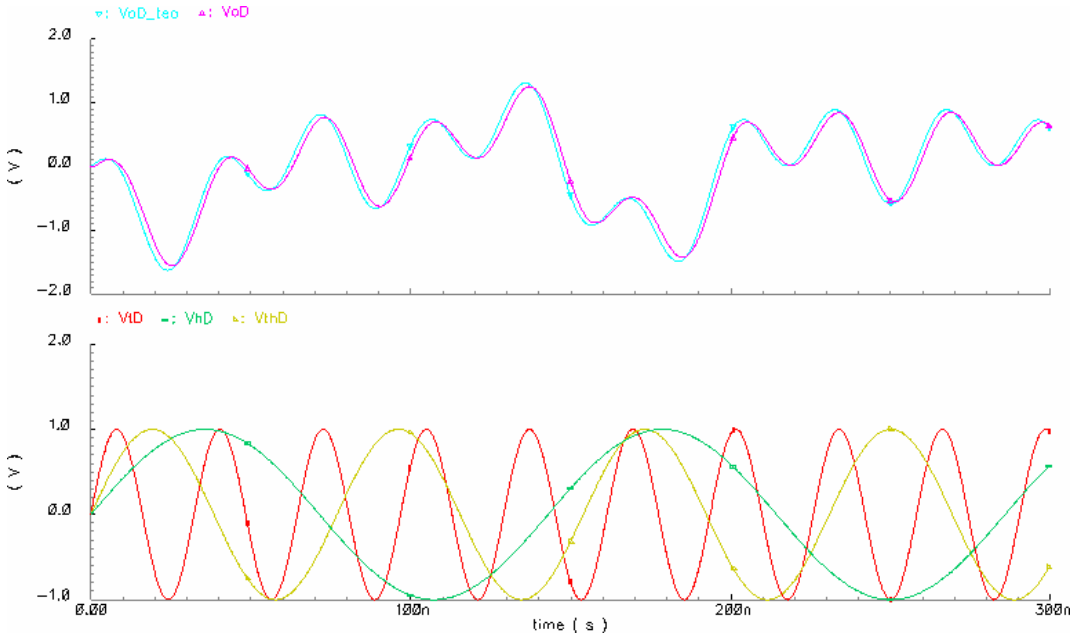

Figure 4-61. Results of the simulation of the triple addition stage. Bottom: input signals. Top: ideal output (V_{oD_teo}) and simulated output (V_{oD})

The ideal output follows quite well the ideal response, the discrepancy is due to the phase delay introduced by the first order response of the stage; the dominant pole is at ≈300 MHz and it corresponds to 7º for 30 MHz sine input signal (V_t). Simulations at low frequency show that the linearity error is about 1%.

As said before, this kind of stage is very robust to temperature variations, according to Spectre simulations the TC of the stage is about 100 ppm/K.

4.2.5 Differential comparator

A latched comparator [159] evaluates the sign of the result of the previous operation. The comparator, shown in Figure 4-62, has two operation modes according to the clock level. In the acquisition phase it amplifies the input signal while in the latch state it exploits positive feedback to reach the desired output levels.

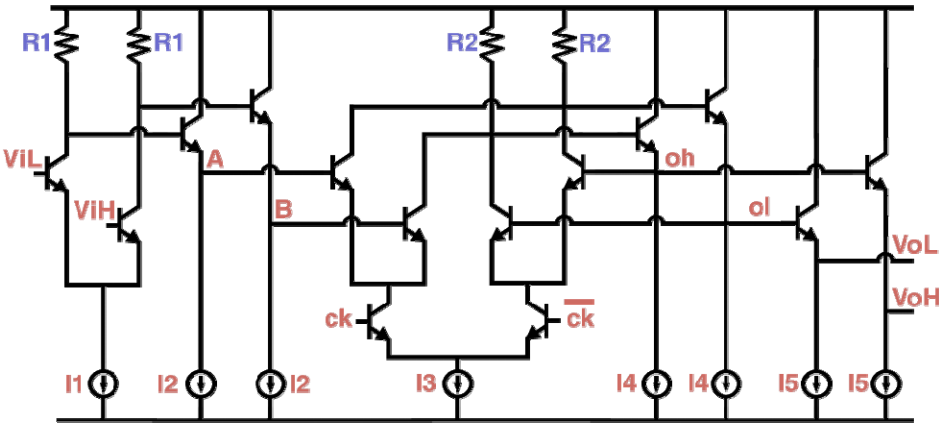

Figure 4-62. Schematic of the latched comparator.

The requirements for the comparator are a fully differential structure, resolution about 1mV or less and valid operation at the frequency of 20MHz. The input signal is fully differential with maximum range about ± 500 mV. The output is a pseudo-ECL differential signal of ±350 mV. The comparator is controlled by a clock signal of amplitude ±250 mV.

The comparator is basically formed by:

- A pre-amplification stage that allows better resolution and reduces power consumption. This amplification stage is a differential pair formed by two npn bipolar transistors and load resistors.
- A buffer formed by two emitter followers.
- The amplification and latch stage, formed by two crossed differential pairs controlled by another differential pair clocked. The operation consists in two phases, an evaluation phase (ck high, nck low) where the left differential pair of the amplification stage actuates and the store phase (ck low, nck high) where the right pair of the amplification stage in figure actuates. In the storing phase further amplification occurs.
- An output buffer (emitter follower).

The complete comparator consumes 750 µA.

Figure 4-63 a) presents a simulation of the comparator in which the input signal V_{iD} varies between 100 µV and -100 µV, it corresponds to simulated output of the addition stage with V_t varying from 199.9mV and 200.1mV, with the threshold voltage V_{th} fixed at 200mV and with V_h=0.

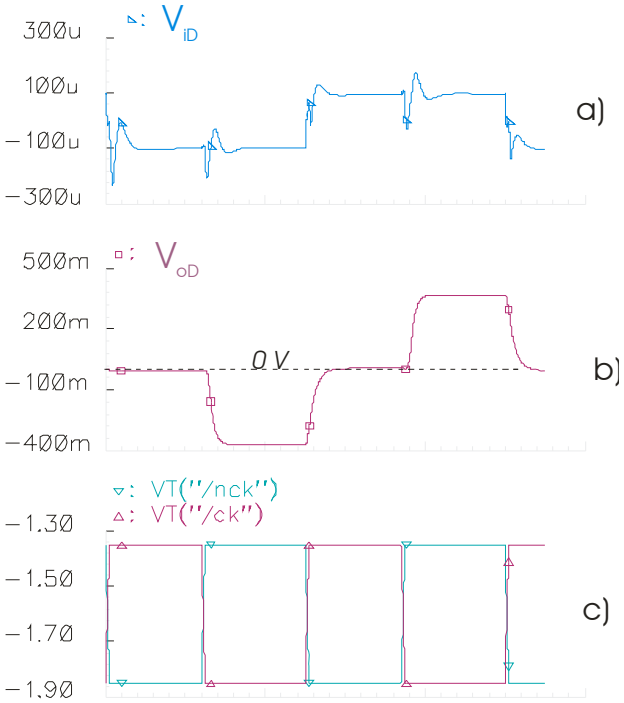

Figure 4-63. Simulation of the comparator: a) input signal (V_{iD}), b) output signal (V_{oD}) and c) controlling clock signals.

The evaluation phase and the storing phase are clearly visible in Figure 4-63 (curve b V_{oD}). In the pre-amplification phase the output signal is only of a few mV (close to the 0V level), negative in the first cycle and positive in the second one. In the hold phase there is a large amplification which gives the output at ± 350mV.

4.3 Output circuitry of the channel

The output of the comparator is a binary signal indicating whether the input charge is above programmed threshold or not. However, it is not possible to directly connect the output of the comparator to an output pad, it is needed to:

- Select the subchannel whose comparator output is in latch state. This is done using a multiplexer.
- Translate the pseudo-ECL levels at the output of the multiplexer and comparator to CMOS levels to drive a standard digital output pad.

4.3.1 Multiplexer

Figure 4-64 shows the schematic of the multiplexer. The input stages adjust the CM of the pseudo-ECL input signals coming from the comparator of each subchannel. As the circuit is operated at a relative low voltage it is very important to control the CM levels at the base of the transistors of the input differential pairs of the differential switch (I_4-I_5 and I_{10}-I_{11}). Through a careful adjustment of the operating point it is possible to use the same differential clock that drives the comparator. The output of the multiplexer is a pseudo-ECL differential signal of ±800 mV of amplitude, high level is 0.85 V and low level is 0.05 V.

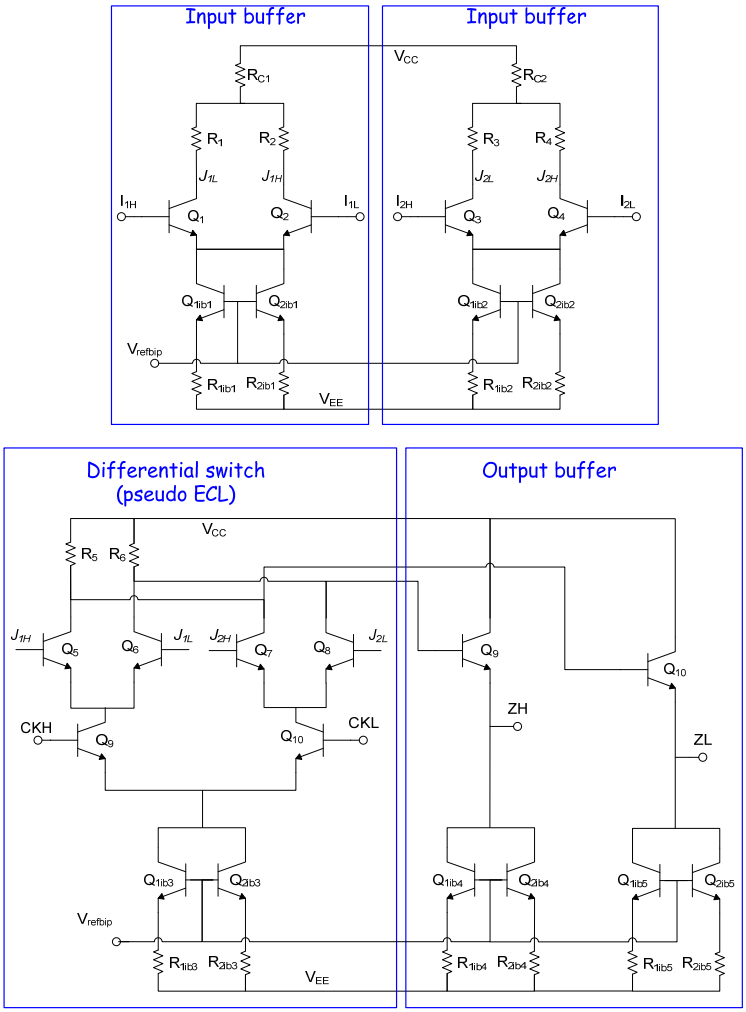

Figure 4-64. Schematic of the multiplexer.

Figure 4-65 shows the operation of the multiplexer, the propagation delay is less than 2 ns.

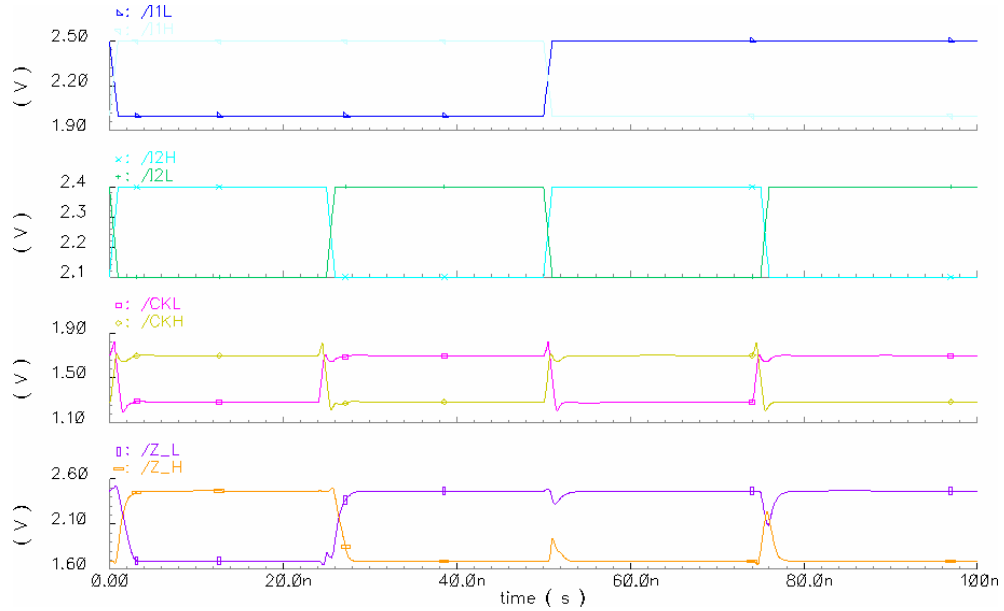

Figure 4-65. Transient simulation results of the operation of the multiplexer. Note that V_{cc}=3.3V and V_{ee}=0V for this simulation.

4.3.2 ECL to CMOS converter

The ECL to CMOS converter stage adapts the output levels of the multiplexer to CMOS levels so that standard output pads can be used. Figure 4-66 shows the schematic of the ECL to CMOS converter

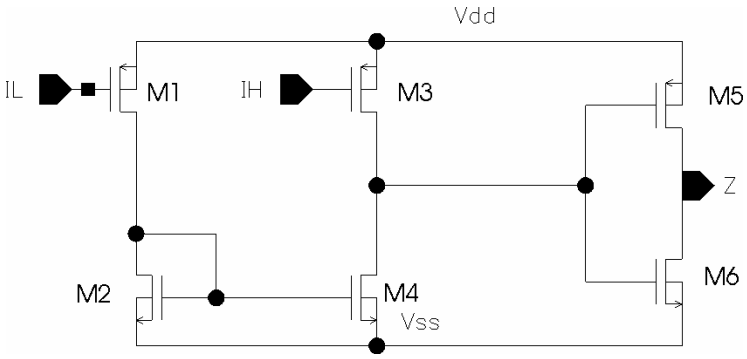

Figure 4-66. Schematic of the ECL to CMOS converter.

The operation can be understood analyzing the two possible states of the inputs:

1. I_H=0.85 and I_L=0.05. $V_{GSM1} \approx V_{TP}$, so $I_{DM1} \approx I_{DM2} \approx 0$. The current mirror M_1-M_2 force $I_{DM2} \approx I_{DM4}$, thus $I_{DM3} \approx 0$. As $V_{GSM3} \approx 1.6$ V and $I_{DM3} \approx 0$, M_3 must be in ohmic region ($V_{DSM3} \approx 0$) so the voltage at the input of the CMOS inverter (M_5-M_6) is $\approx V_{dd}$ and the output (Z) will be $\approx V_{ss}$.
2. I_H =0.05 and I_L =0.85. On the one hand $V_{GSM3} \approx V_{TP}$, so $I_{DM3} \approx 0$. On the other hand $V_{GSM1} \approx 1.6 >> V_{TP}$, M_1 operates in the ohmic region and therefore $V_{GSM2}=V_{GSM4} >> V_{TN}$. As M_4 is on and $I_{DM3} \approx I_{DM4} \approx 0$, M_4 operates in the ohmic region ($V_{DSM4} \approx 0$) so the voltage at the input of the CMOS inverter (M_5-M_6) is $\approx V_{ss}$ and the output (Z) will be $\approx V_{dd}$.

Figure 4-67 shows input and output signals of a transient simulation of the converter. The input signal is the simulated output signal of the multiplexer. Propagation delay is less than 2 ns and the rise and fall times are below the ns.

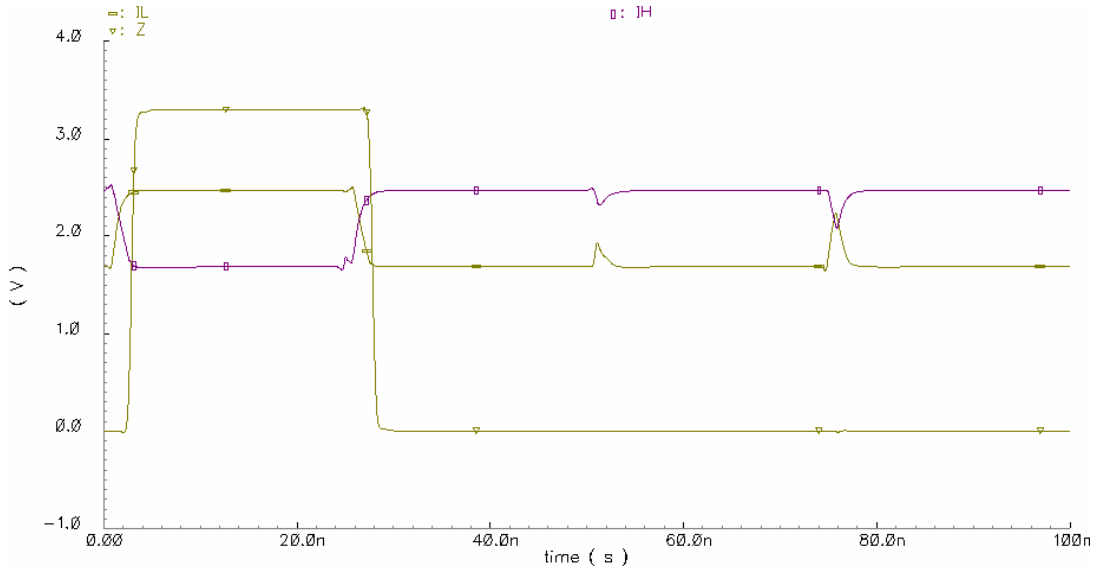

Figure 4-67. Transient simulation of the operation of the ECL to CMOS converter. Note that V_{dd}=3.3V and V_{ss}=0V for this simulation.

4.4 Threshold setting circuits

The threshold value is set by a 7 bits DAC, the range of the DAC is determined by the dispersion of the offset of the ASD, as will be shown in next chapter. The DACs are programmed through a serial interface, basically a shift register, to reduce the pin count.

4.4.1 Digital shift register

In Figure 4-68 the block diagram of the synchronous digital interface is shown. Threshold DAC register data is loaded through a serial interface to save pins and area. As long as the digital control signal "capt0_scan1"=1 the shift register shifts the input data. When data is properly placed control signal "e" must be activated to store information in the triple voting register.

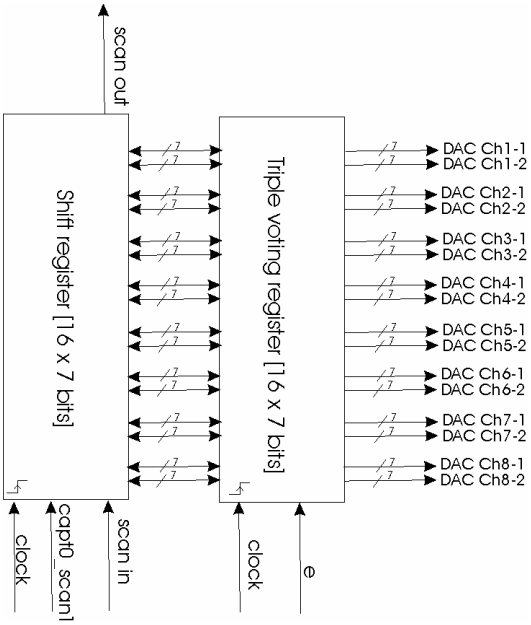

Figure 4-68. Digital interface.

According to LHCb electronics requirements any configuration register must be readable to perform systematic test and monitoring. When "capt0_scan1"=0 the threshold triple voting registers information is loaded on the serial register and can be monitored by the ECS trough the "scan_out" pin. When "e=0", at each clock cycle the content of the triple voting register is self-updated.

To prevent Single Event Upset the true memory elements of the digital part use a triple voting mechanism [30]. The shift register does not implement triple voting since its operative time is very small: digital interface can be operated up to 100MHz according to simulation and it is foreseen to work with 1MHz clock, that means that loading the complete configuration of an ASIC takes <1ms. The flip-flops have been implemented using a "master-slave" architecture. To save area only the slave implements triple voting: the duty cycle of the digital clock must be tuned to ensure that the slave will be the active memory element >99% of time.

Figure 4-69 shows the layout of 1 memory bit: including shift register and triple voting mechanism. A full custom design was done to implement the triple voting on an efficient way, that is to say, to minimize the area and the sensitive nodes.

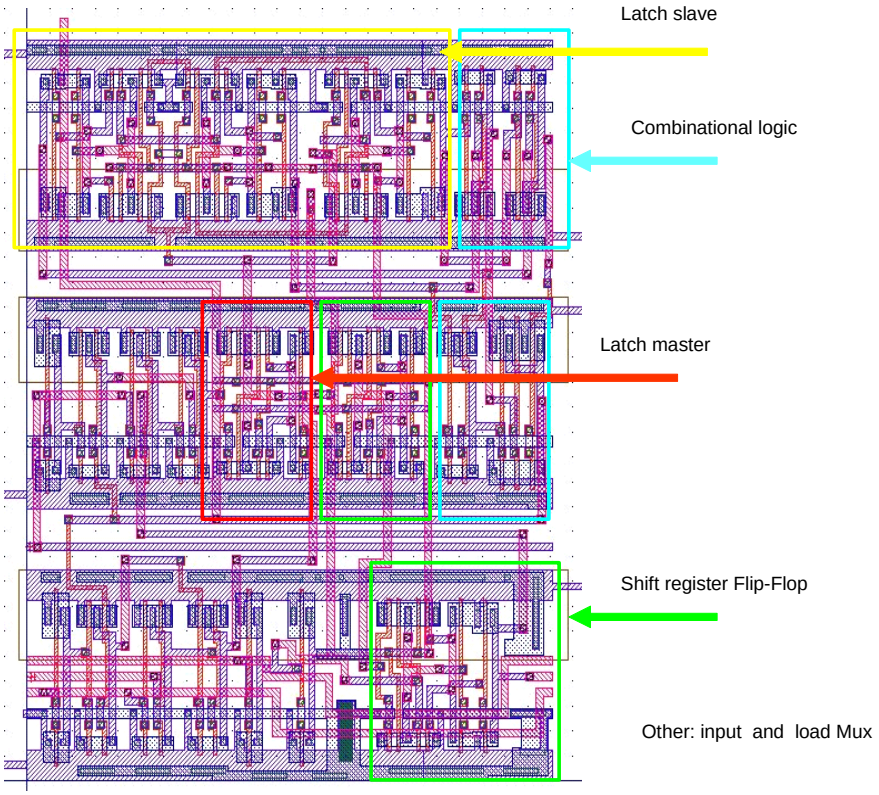

Figure 4-69. Layout of 1 memory bit: including shift register and triple voting mechanism.

4.4.2 D/A module

The DAC is an R-2R network that divides a floating reference voltage (Figure 4-70). It is a multiplying converter to have higher degree of freedom to calibrate and set the thresholds. R_{00D}, R_{01D} and R_0 to R_5 are 6 kΩ polysilicon resistors whereas R_{0H} to R_{5H} are 3 kΩ polysilicon resistors. It uses 1 bit to define the sign (DB_{6ctrl}) and 6 for the modulus (DB_{0ctrl} to DB_{5ctrl}). Each control bit drives a CMOS switch (S_x). The layout is done using dummy switches (S_{xD}) and common centroid techniques to improve the linearity. The noise bandwidth is reduced to about 2 MHz using internal capacitors connected to ground (C_{Dec1} and C_{Dec2}).

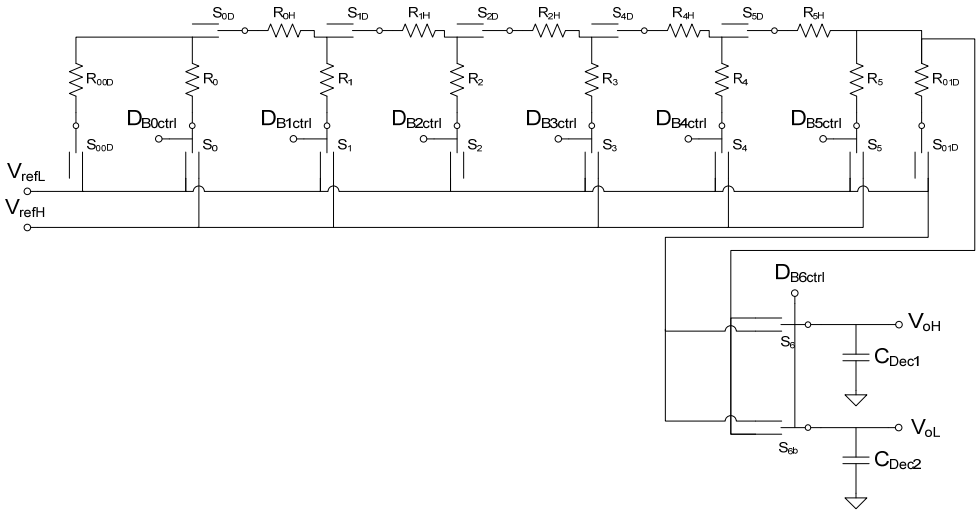

Figure 4-70. Schematic of the DAC.

4.5 Global circuitry

4.5.1 Bias current master

All the analogue blocks of the chip obtain its bias current from a reference current generated by a master current source. Figure 4-71 shows the schematic of this current master, which is a supply-independent band gap referenced current source. The idea behind this kind of bias circuits is to combine the current of a bias source referenced to $V_{BE(ON)}$ and the current of bias source referenced to V_T. Both bias sources, are supply independent and have opposite temperature coefficient (TC), thus, it is possible to think on referencing the output current to a weighting sum of both currents in such a way that the combined current has zero TC ([66],[161]).

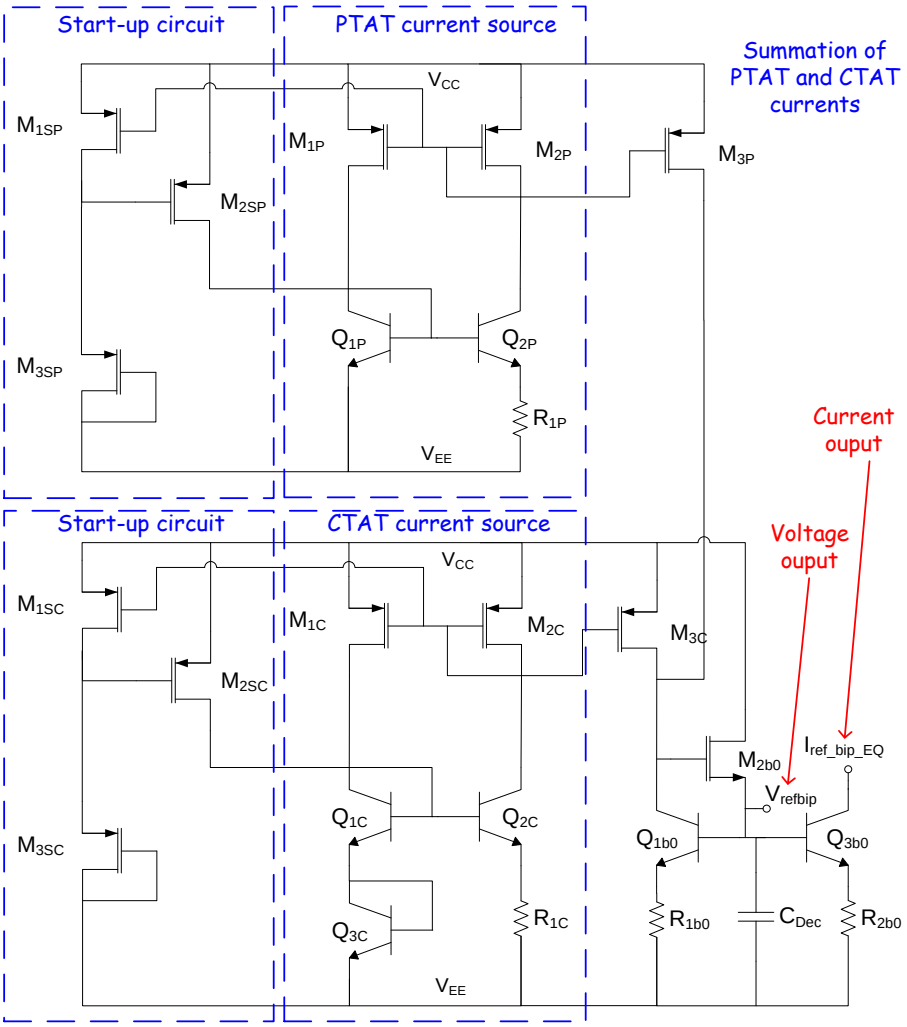

Figure 4-71. Schematic of the band gap current source.

The current source based on V_T has a positive TC, and it is also referred as proportional to absolute temperature (PTAT). For the PTAT circuit of Figure 4-71 and considering $-I_{E\_Q2P} \approx I_{C\_Q2P} = -I_{D\_M2P} = -I_{D\_M3P}/2 = I_{PTAT}/2$ and $-I_{E\_Q1P} \approx I_{C\_Q1P} = -I_{D\_M1P} = -I_{D\_M3P} = I_{PTAT}$,

$$V_{BE\_Q1P} = V_{BE\_Q2P} + \frac{I_{PTAT}}{2} R_{1P} \qquad (4.212)$$

Knowing that $V_{BE} = V_T \ln\left(I_C / I_S\right)$ and that I_S is proportional to the emitter area, from (4.212),

$$V_T \ln\left(\frac{I_{PTAT}}{I_{S\_Q1P}}\right) = V_T \ln\left(\frac{I_{PTAT}/2}{3I_{S\_Q1P}}\right) + \frac{I_{PTAT}}{2} R_{1P} \qquad (4.213)$$

then, the PTAT current is,

$$I_{PTAT} = \frac{2V_T \ln(6)}{R_{1P}} \qquad (4.214)$$

The current source based on V_{BE} has a negative TC, and it is also referred as complementary to absolute temperature (CTAT). For the CTAT circuit of Figure 4-71 and considering $-I_{E\_Q2C} \approx I_{C\_Q2C} = -I_{D\_M2C} = -I_{D\_M3C} = I_{CTAT}$, $-I_{E\_Q2C} \approx I_{C\_Q2C} = -I_{D\_M2C} = -I_{D\_M1C} \approx I_{C\_Q1C} \approx -I_{E\_Q1C} \approx I_{C\_I27} \approx -I_{E\_I27}$, and $V_{BE\_Q1C} \approx V_{BE\_Q2C}$,

$$I_{CTAT} = \frac{V_{BE\_Q3C}}{R_{1C}} = \frac{V_T}{R_{1C}} \ln\left(\frac{I_{CTAT}}{I_{S\_Q3C}}\right) \qquad (4.215)$$

The circuit to sum CTAT and PTAT current is a bipolar current mirror with N-MOS beta helper. Bipolar mirrors are used because they usually have better matching than MOS mirrors [173]. Emitter degeneration is used to increase the output resistance and to improve the matching [66]. The circuit provides two kinds of outputs:

- A bias current of 120 μA connecting the load at the collector Q_{3B0}. This is only used by the circuit generating the reference voltages for the FDOA (see 4.2.2.2.1).
- The possibility to connect additional transistors to the node "V_{refbip}", thus creating mirrors where needed. Each added mirror increases the error due to its base current, to avoid this effect beta helper circuits can be used [66]. MOS transistors are especially useful as beta helper because its high input impedance [173], thus M_{2b0} plays this role.

Most of the blocks of the chip use the second type of output and generate its bias current just adding the corresponding part of the bipolar mirror with emitter degeneration and replicating or scaling it to obtain the required current.

The output impedance is an important parameter of a current mirror, for example it determines the CMRR in differential pairs. The output resistance R_{olb} of a bipolar mirror with emitter degeneration (resistor R_E) can be approximated [66] by

$$R_{olb} \simeq r_o \left(1 + g_m R_E\right) \qquad (4.216)$$

The output resistance r_o in the small signal model of the bipolar transistor is defined as the ratio of the AC variation of v_{CE} to the variation of i_C. For a specific value of I_C, the output resistance is given [67] by $r_o = V_E / I_C$, where V_E is the Early voltage (named VAF in models). According to the model of the transistor (see section A)V_E is about 37 V (for an area parameter value of 12), and then the output resistance r_o is about 300 kΩ for a collector current of 120μA. The output resistance of each bipolar mirror unit will be about 1.7 MΩ, with R_E equal to 1068 Ω and g_m about 5 mS. Table 4-6 shows the current and output resistance for different multiples of the basic current mirror.

	Output current [μA]	Output resistance [kΩ]
1x	124	1700
3x	372	500
4x	495	330
8x	990	135

Table 4-6. Current and output resistance for several multiples of a single bipolar current mirror. Obtained through simulation.

In this application, it is better that the master current has a slightly positive TC. This is due to the fact that most of the analog blocks of the chip are based of bipolar differential pairs. The temperature dependence of the transconductance of a bipolar transistor is at first order given by,

$$\frac{\partial g_m}{\partial T}=\frac{\partial g_m}{\partial I_{CQ}}\frac{\partial I_{CQ}}{\partial T}+\frac{\partial g_m}{\partial V_T}\frac{\partial V_T}{\partial T}=\frac{1}{V_T}\frac{\partial I_{CQ}}{\partial T}-\frac{I_{CQ}}{V_T^2}\frac{k}{q} \qquad (4.217)$$

where I_{CQ} is the quiescent current and $V_T=kT/q$, where T is the "quiescent" temperature, q is the electron charge $q=1.6\cdot10^{-19}$ C and $k=1.38\cdot10^{-23}$ J/K is the Boltzmann's constant. In order to have a transconductance value independent of the temperature,

$$\left.\frac{\partial I_{CQ}}{\partial T}\right|_{\frac{\partial g_m}{\partial T}=0}=\frac{I_{CQ}}{T} \qquad (4.218)$$

Or in terms of TC,

$$TC_{I_{CQ}}\Big|_{\frac{\partial g_m}{\partial T}=0}=\frac{1}{I_{CQ}}\left.\frac{\partial I_{CQ}}{\partial T}\right|_{\frac{\partial g_m}{\partial T}=0}=\frac{1}{T} \qquad (4.219)$$

Then, for a typical ambient temperature (T=300K), the temperature coefficient of the quiescent current must be around 3000 ppm/K. However, other important parameters such as the quiescent or bias levels of some circuits depend on the bias current and such a large positive TC would be problematic, hence a compromise will be taken.

Using (4.214), we obtain a first order approximation of the dependence of the of bias current with the temperature,

$$\frac{\partial I_{PTAT}}{\partial T}=\frac{2\ln(6)}{R_{1P}}\frac{\partial V_T}{\partial T}-\frac{2V_T\ln(6)}{R_{1P}^2}\frac{\partial R_{1P}}{\partial T} \qquad (4.220)$$

As the last term of (4.220) is typically small, the PTAT part of the current has a positive TC as expected. In the same way for the CTAT part,

$$\frac{\partial I_{CTAT}}{\partial T}=\frac{1}{R_{1C}}\frac{\partial V_{BE\_Q3C}}{\partial T}-\frac{V_{BE\_Q3C}}{R_{1C}^2}\frac{\partial R_{1C}}{\partial T} \qquad (4.221)$$

According to [161] the temperature dependence of base to emitter conduction voltage is approximately,

$$\frac{\partial V_{BE}}{\partial T}=\frac{V_{BE}-(4+m)V_T-E_g/q}{T} \qquad (4.222)$$

where $E_g\approx1.12$ eV is the bandgap energy of silicon and the constant $m\approx-3/2$. With typical values of $V_{BE}\approx0.75$ V and T=300 K, $\partial V_{BE}/\partial T=-1{,}5$ mV/K . As last term of (4.221) is typically smaller, the TC of the CTAT part of the current is negative as expected.

The TC of the combined bias current $I_{bias}=I_{PTAT}+I_{CTAT}$ is,

$$\frac{\partial I_{bias}}{\partial T}=\frac{\partial I_{PTAT}}{\partial T}+\frac{\partial I_{CTAT}}{\partial T}=\frac{2\ln(6)}{R_{1P}}\frac{\partial V_T}{\partial T}-\frac{2V_T\ln(6)}{R_{1P}^2}\frac{\partial R_{1P}}{\partial T}+\frac{1}{R_{1C}}\frac{\partial V_{BE\_Q3C}}{\partial T}-\frac{V_{BE\_Q3C}}{R_{1C}^2}\frac{\partial R_{1C}}{\partial T} \qquad (4.223)$$

As said before terms corresponding to V_T and V_{BE} temperature coefficients are the dominating ones and have opposite TC sign, then to minimize expression (4.223) they must be equated,

$$\frac{2\ln(6)}{R_{1P}}\frac{\partial V_T}{\partial T}=-\frac{1}{R_{1C}}\frac{\partial V_{BE\_Q3C}}{\partial T} \qquad (4.224)$$

Condition (4.224) is accomplished by adjusting the value for the ratio of resistors R_{1C} and R_{1P},

$$\frac{R_{1C}}{R_{1P}} = -\frac{\dfrac{V_{BE} - (4+m)V_T - E_g/q}{T}}{2\ln(6)\,k/q} = -\frac{V_{BE} - (4+m)V_T - E_g/q}{2\ln(6)V_T} \simeq 5 \quad (4.225)$$

It is important to notice that the cancellation of CTAT and PTAT depends on the ratio of two resistors, and therefore matching will be much better than if it was function of absolute values. Then, considering that main CTAT and PTAT terms are cancelled out in (4.223) the temperature dependence of bias current is,

$$\frac{\partial I_{bias}}{\partial T} = -\frac{2V_T \ln(6)}{R_{1P}^2}\frac{\partial R_{1P}}{\partial T} - \frac{V_{BE\_Q3C}}{R_{1C}^2}\frac{\partial R_{1C}}{\partial T} \quad (4.226)$$

As R_{1C} and R_{1P} are resistors made with the second level of polysilicon, so they have the same temperature coefficient,

$$\frac{\partial I_{bias}}{\partial T} = -\left(\frac{2V_T \ln(6)}{R_{1P}} + \frac{V_{BE\_Q3C}}{R_{1C}}\right)\frac{1}{R_{Poly2}}\frac{\partial R_{Poly2}}{\partial T} \quad (4.227)$$

And the temperature coefficient of the bias current is just given by the negative of the TC of the second level of polysilicon, which is -300 ppm/K,

$$TC_{I_{bias}} = \frac{1}{I_{bias}}\frac{\partial I_{bias}}{\partial T} = -\frac{1}{R_{Poly2}}\frac{\partial R_{Poly2}}{\partial T} = -TC_{Rpoly2} = 300 \text{ ppm/K} \quad (4.228)$$

Figure 4-72 shows simulations results of the dependence on the temperature of the bias current. The slope is about 50 nA/K for a quiescent current o 120 µA, thus the approximated TC_{Ibias} is about 400 ppm/K according simulations. It is slightly positive as required.

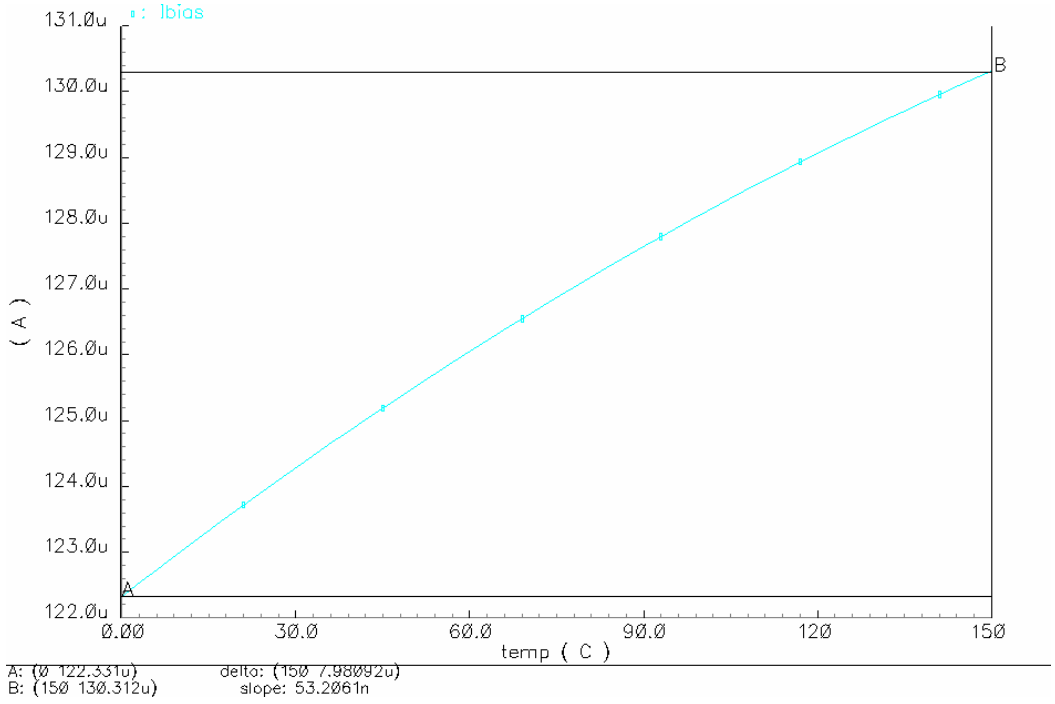

Figure 4-72. DC bias current as a function of temperature.

The bias circuitry of Figure 4-71 also includes start-up circuits. Equations (4.212)and (4.215) used to derive the quiescent currents of CTAT and PTAT circuits have a second trivial solution when I=0. To prevent the bias circuit from settling to the wrong steady-state condition, a startup circuit is

necessary in all practical applications [167]. Taking for example the PTAT start-up circuit, if $I_{PTAT}=I_{D\_M1P}=I_{D\_M1SP}= I_{D\_M3SP}=0$ then $V_{GS\_M3SP}=0$. As M_{3SP} is a diode connected PMOS, $V_{DS\_M3SP}=0$ and $V_{GS\_M2SP}=-3.3$ V, then M_{2SP} must be on and current will be injected to the collector node of Q_{1P}, forcing the circuit to move to its other equilibrium state. Figure 4-73 it is shown the start-up cycle of the bias circuit.

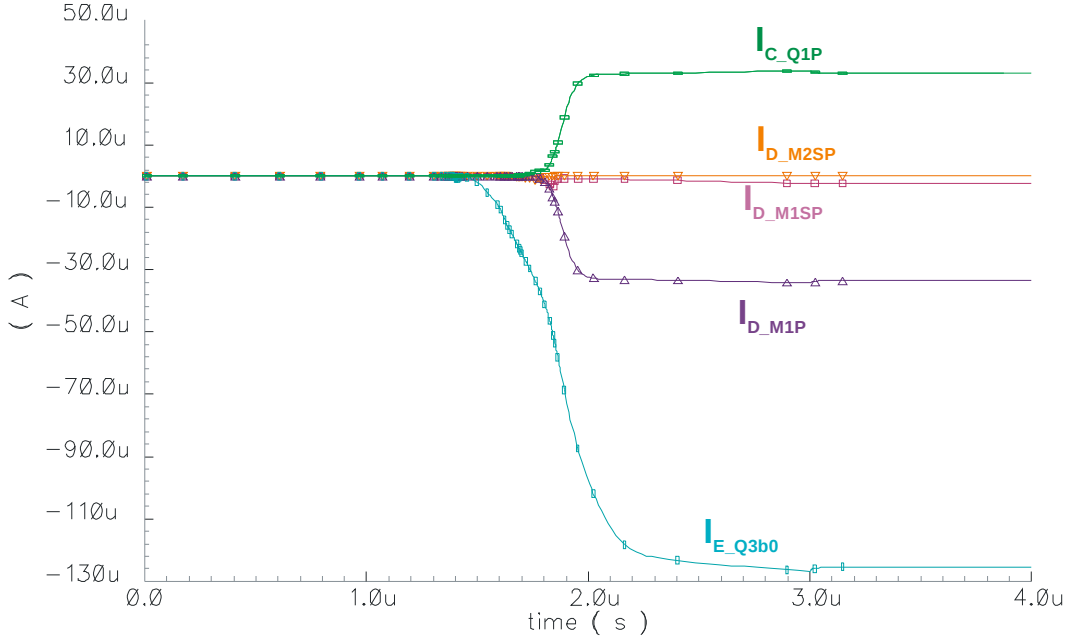

Figure 4-73. Transient simulation of the start-up circuitry operation.

Although this bias circuit can be classified as supply-independent, any transistor has finite output resistance and considering the small-signal model of the circuit it can be shown that power supply variations will be coupled to the bias current in some extend. A detailed analysis of the role of the bias circuit in the PSRR of sensitive blocks such the preamplifier or the integrator is presented in section 5.3.

4.5.2 Clocking modules

Several blocks of the discriminator channel are controlled through a 20 MHz clock. Since this clock has not the same levels and timings for all blocks a circuit to generate this phases from an input 20 MHz clock is needed. The requirements for this generator are:

- Input clock: 20 MHz differential (LVDS) with CM≈0V (V_{ss}=-1.65V).
- Generation of pseudo CMOS differential clock for the integrator:
  - From 0 to 1.65 V for nMOS switches.
  - From 0 to -1.65 V for nMOS switches.
- Two different phases of the CMOS clock are needed (will be called clk1 and clk2), each of the two interleaved subchannels.
- Generation of pseudo ECL differential clock for the track and hold, comparator and multiplexer circuits. Although two pseudo ECL clock phases are need, as it is fully balanced and symmetrical this can be obtained just connecting the clock in the opposite way in each subchannel.
- Delay of about 2 nanoseconds between CMOS and ECL phases: to sample the integrator signal before reset

Figure 4-74 shows the schematic of the pseudo ECL clock generation circuit. It consists basically on a differential pair plus emitter followers to be able to drive capacitive loads (the parasitic stray capacitances of the clock distribution lines) without degradation of signal quality.

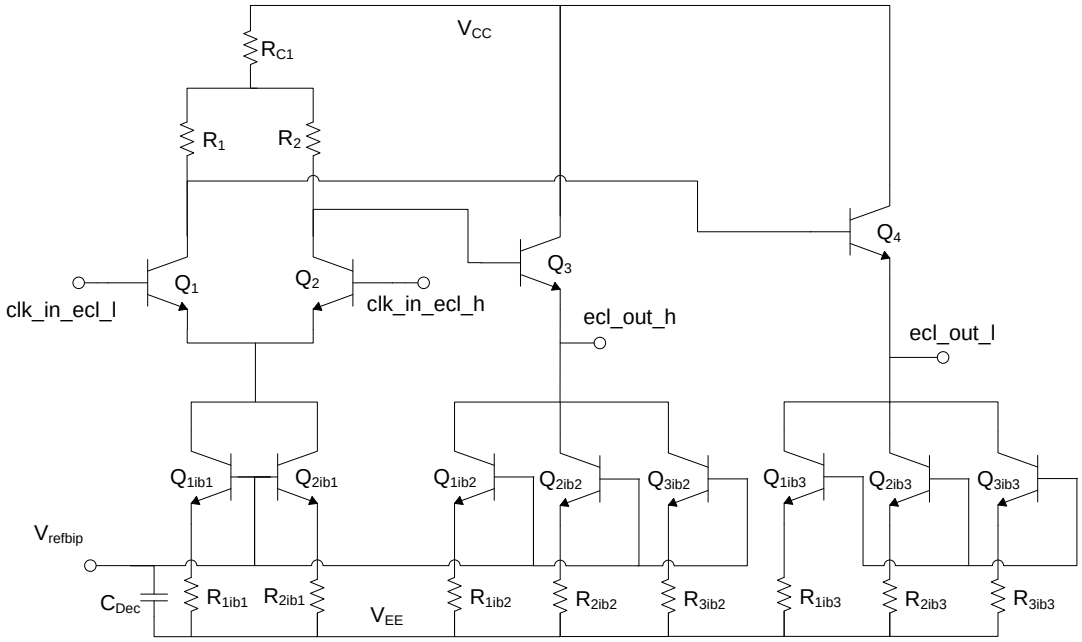

Figure 4-74. Schematic of the pseudo ECL clock generation circuit.

The output of the ECL clock generator circuit is connected to the CMOS clock circuit, shown in Figure 4-75. An input differential buffer drives two complementary differential pairs, to generate the control signals for pMOS and nMOS transistors of the integrator switches. Each branch of one of this differential pairs generates one phase (clk1 or clk2) of the CMOS clock. Finally a CMOS inverter buffers nMOS and pMOS clock signals of each phase.

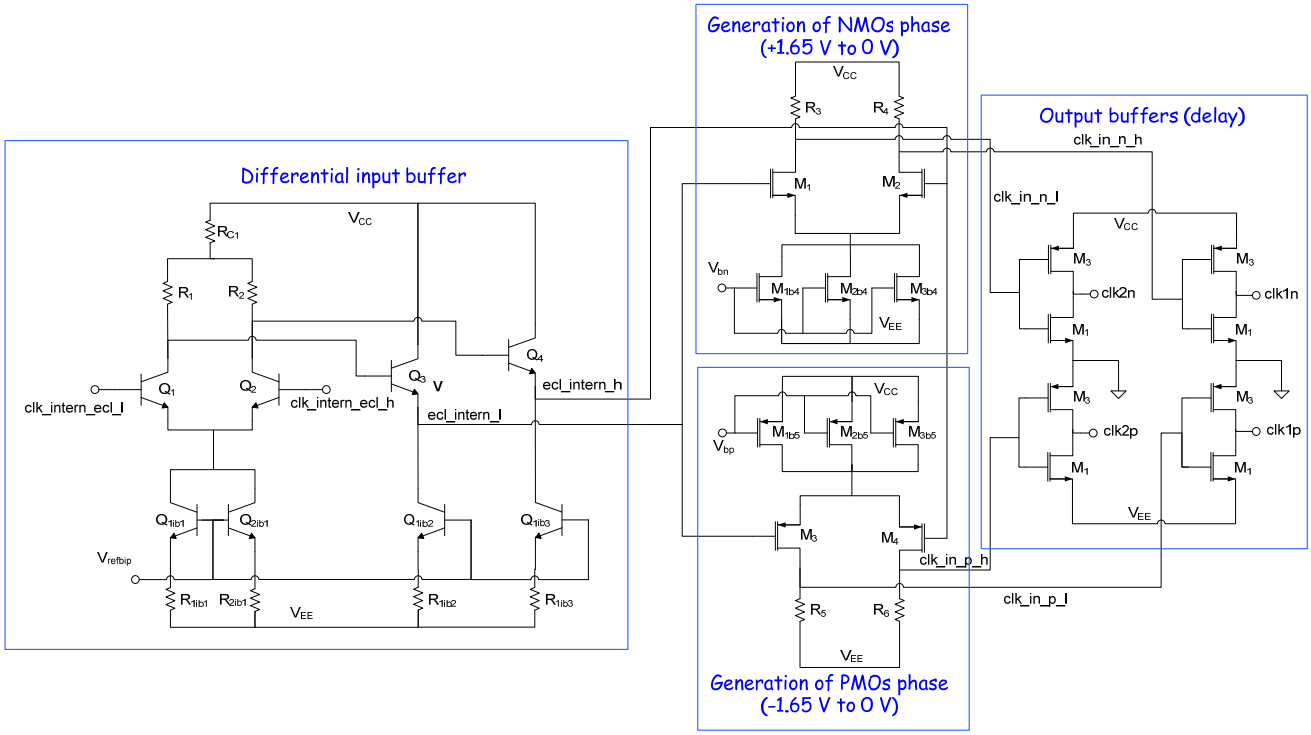

Figure 4-75. Schematic of the CMOS clock generation circuit.

Waveforms of all the clock phases are shown in Figure 4-76. The parameters of the circuit have been carefully tuned to have the minimum delay between CMOS transitions. This is very important to try to balance supply currents and to cancel the pick up noise.

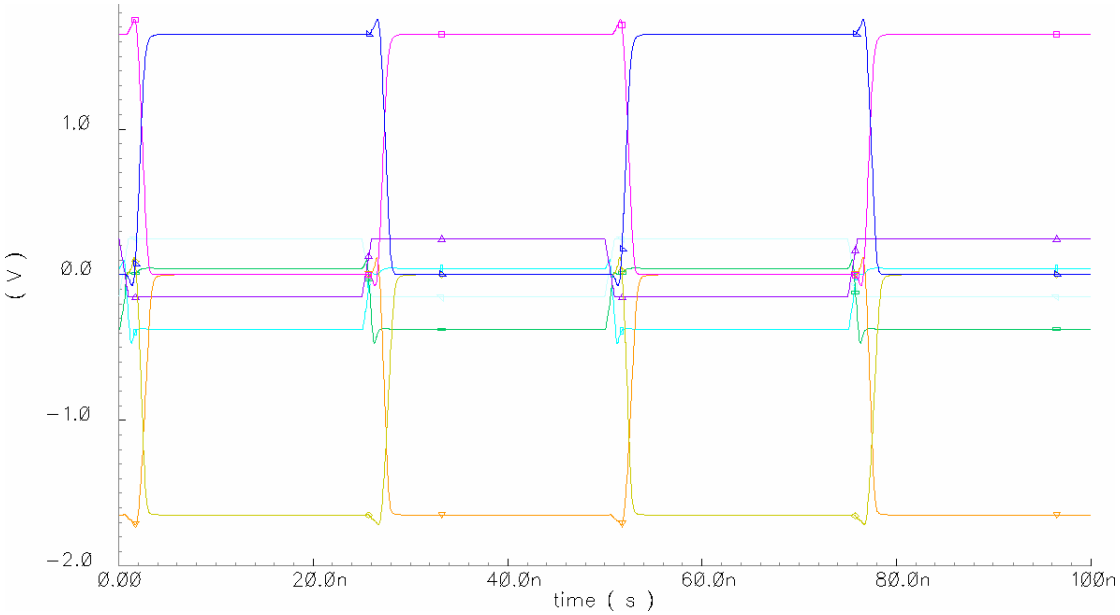

Figure 4-76. Post-layout transient simulation of clock generation.

The size of the output buffers of Figure 4-75 has been carefully adjusted through post-layout simulations of the complete channel to achieve the required delay between ECL and CMOS clocks and to maximize the symmetry in CMOS clocks. According to post-layout simulation results shown in Figure 4-77, the delay is about 1.7 ns.

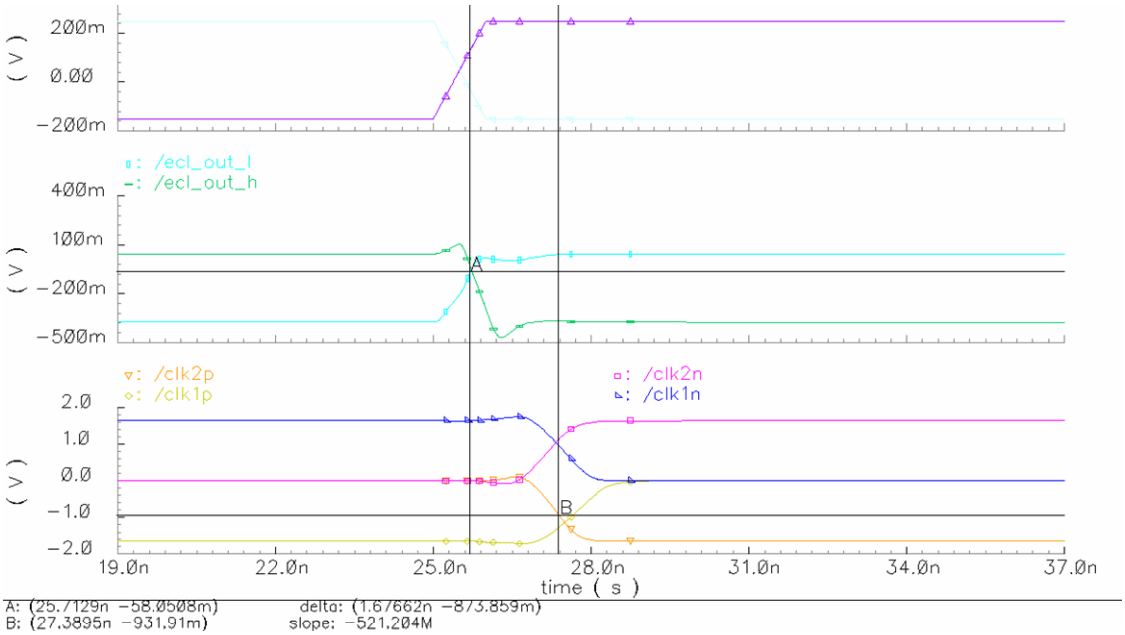

Figure 4-77. Post-layout transient simulation of clock generation. Detail of the ECL to CMOS delay.

4.6 Layout of the 8 channel ASIC

In Figure 4-78 it is shown the general view of the 8 channel discriminator ASIC. Die size is 5.254 mm x 5.500 mm (30 mm^2).

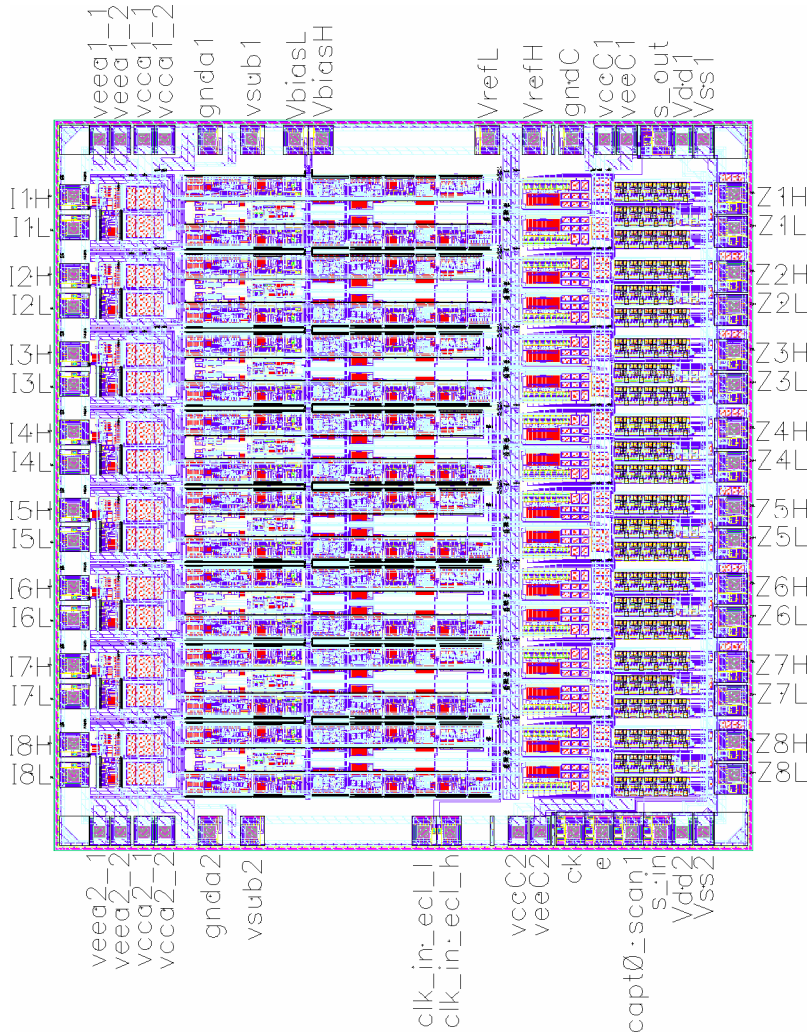

Figure 4-78. General view of the layout of the 8 channel ASIC.

The power supply distribution of the chip is divided in three different groups, separated to minimize the common mode interference:

1. Analogue supply (*Veea, Vcca)* and reference (*gnda*). The substrate is biased trough a dedicated pad (*Vsub*) to minimize the injection of substrate noise.
2. Digital supply (*Vdd,Vss*). On that part the substrate contacts are connected to *Vss*.
3. Clock distribution and generation system supply (*VccC, VeeC*) and reference *gndC*

The two duplicated signal paths in a channel, called subchannels, are shown in Figure 4-79. The subchannel comprise from the integrator to the comparator and DAC. The digital interface, the multiplexer, the clock generation and the preamplifier are single elements. Details of input and output parts of the channel are shown in Figure 4-80 and Figure 4-81 respectively.

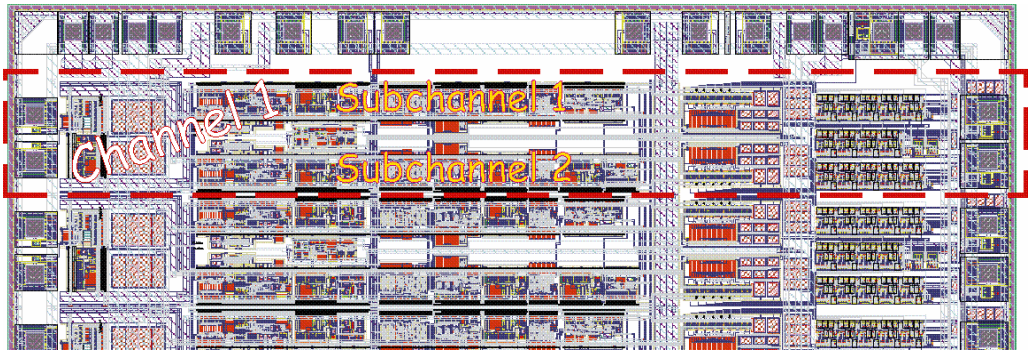

Figure 4-79. Detail of the two first channels of the chip.

The preamplifier has been placed nearby the input signal pads (*IXX*), see Figure 4-80. Between preamplifier and integrator there are the analog voltage supply lines with pads at the top and at the bottom (*Veea, Vcca, gnda and vsub*) to have the most symmetrical bias current distribution; this is done also for digital and clock supply lines (see Figure 4-81). On chip decoupling capacitors are used for all the supplies.

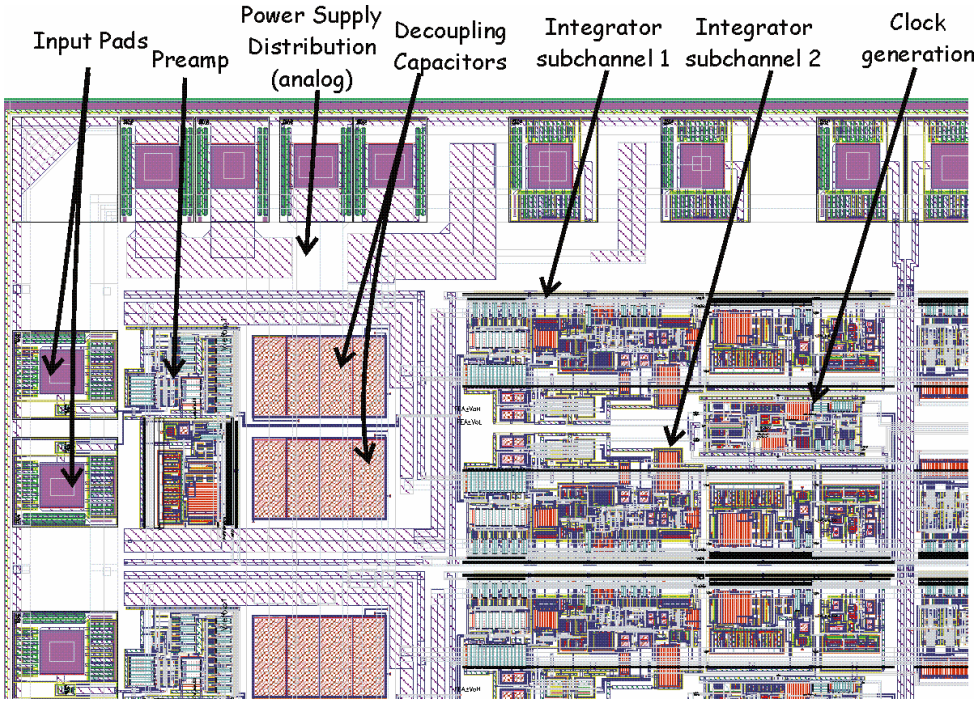

Figure 4-80. Input part of the channel 1.

Clock distribution is done from the output of the channel to the input to avoid interference with sensitive analog signals: preamplifier input and outputs.

Standard AMS pads are used to include ESD protection [160].

The output is differential to try to cancel the digital pick-up noise and balance the supply currents.

Guard rings are widely used in all the CMOS components, both analog and digital, to prevent the Single Event Latch-up provoked by heavy ions and neutrons.

The EDQUAD (TQFP 64 pins) package of ASAT has been chosen because it is optimized to dissipate power through a top metal sink connected to die substrate and its small size (13.2 mm side).

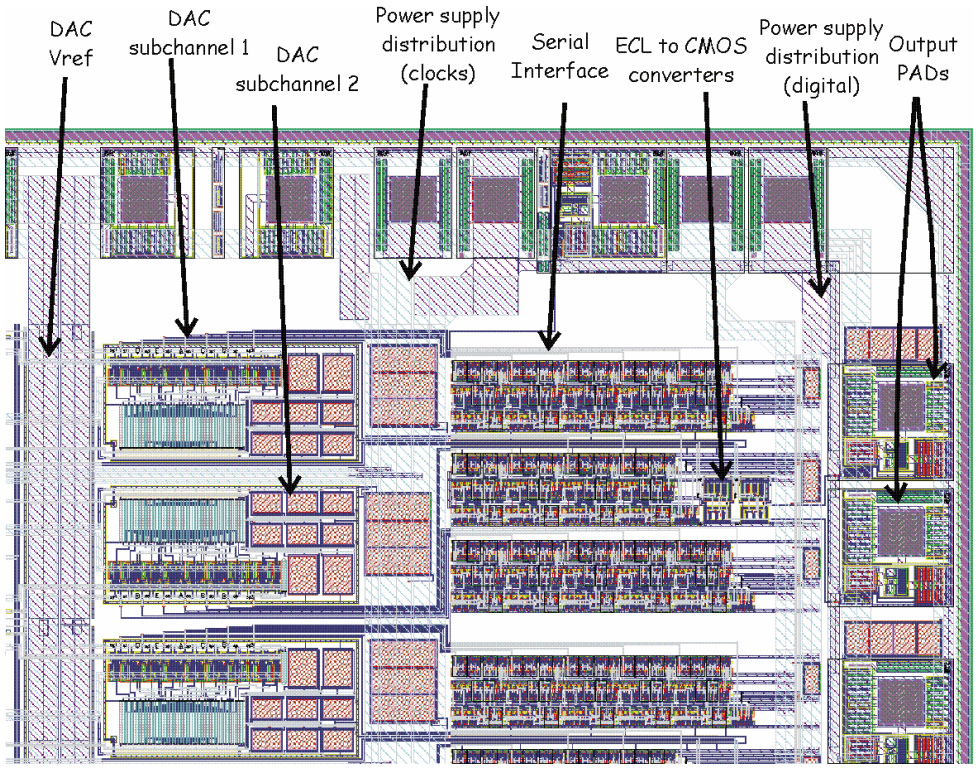

Figure 4-81. Output part of the channel 1.

5 Analysis of the resolution of the ASD

In this section, the factors that will determine the precision or absolute resolution[t] of the ASD are analyzed. First of all the intrinsic noise of the circuit is computed, both through hand calculations and simulations.

Although the intrinsic limit for the resolution of the circuit is given by the random noise, the dispersion of circuit parameters introduce also an offset which is translated into a threshold dispersion that degrades the final "available" resolution of the discrimination. This can be taken into account by measuring the offset of each channel and by adjusting the corresponding threshold. Nevertheless, the full scale range of the channel DACs must be high enough to cope with the threshold dispersion in the 8 channels of a chip. Figure 5-1 shows how the threshold range (DAC range) must fit the signal range plus the offset dispersion accepted for the ASD circuitry (2.5σ in that case). Then, as the DAC has a limited number of bits, the "available" resolution or minimal variation of the threshold that can be set, is given by the offset dispersion.

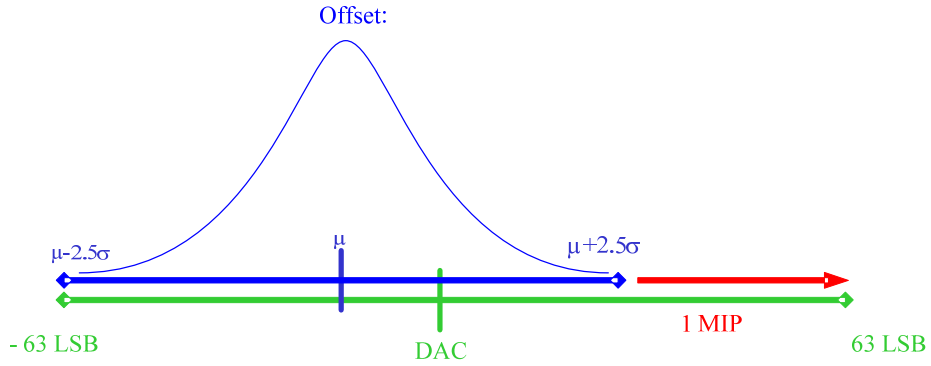

Figure 5-1. Threshold range (DAC range) versus signal range taking into account offset dispersion.

Provided that 1 LSB of the DAC is bigger than the r.m.s of the intrinsic noise, the resolution of the system is given by the full scale voltage (V_{ref}) of the channel DAC divided by 2^6-1, because the internal DAC has 6 bit to set the magnitude of the output voltage and 1 bit to set the sign. As said above, the full scale voltage of the DAC has to be able to cover the offset dispersion plus the signal of 1 MIP. For negative thresholds the most negative value that could be required is 2.5 σ (the limit set to accept a chip) below the mean offset voltage (μ). As the signal is positive, the most positive threshold will be 1 MIP above the most positive offset voltage (μ+2.5σ). Then, the final resolution of the circuit will be:

$$\begin{aligned} &\left|\frac{\mu-2,5\sigma}{63}\right| \quad if \quad |\mu-2,5\sigma| > \mu+2,5\sigma+1\,MIP \\ &\left|\frac{\mu+2,5\sigma+1\,MIP}{63}\right| \quad if \quad |\mu-2,5\sigma| < \mu+2,5\sigma+1\,MIP \end{aligned} \tag{5.1}$$

The susceptibility to external interferences, the offset-voltage drifts and the gain variation may introduce additional degradation of the accuracy of the circuit. Temperature dependence of the offset

[t] We define resolution as the minimal variation of the signal that can be detected [79]. It can be defined as an absolute or a relative magnitude, see chapter 2.

and of the gain, and common mode noise rejection have been analyzed in previous chapter, but it is also very important to analyze the robustness of the circuit against power supply variations. For this reason, at the end of this chapter, the power supply rejection ratio (PSRR) of the sensitive analogue input blocks will be evaluated.

5.1 Noise

In order to analyze the noise of the ASD, first, relevant noise sources will be drawn on a simple circuit model and the equivalent input noise generators will be computed. Then the effect of the time variant shaping will be studied.

5.1.1 Input equivalent noise generators

According to Friis formula (section 2.4.5) when the gain of the first stage of a system composed by a series of cascaded stages is high enough; the output noise of the system is determined by the noise introduced by the first stage and, of course, the transfer function of the system. In the present case the first stage is a voltage preamplifier with a gain 5 approximately for the frequency range of interest. We consider that this is enough to take into account only the noise sources in the preamplifier for the following reasons:

- Input stage of the integrator (and of most stages) is very similar to the one of the preamplifier, therefore noise sources will be comparable and the contribution of the output noise will be given by its position in the amplification chain.
- Noise sources add in quadrature (when uncorrelated).

The preamplifier is a differential circuit. Differential circuits where each input is accessible can not in general be represented as a two-port and its noise performance can not be represented in the usual fashion by two input noise generators [66]. Each input has equivalent noise current and voltage sources [79] as shown in Figure 5-2. Although it is often neglected, correlation between series and parallel noise might have to be considered as discussed in section 2.4. We will try first to analyze the circuit without taking into account that correlation.

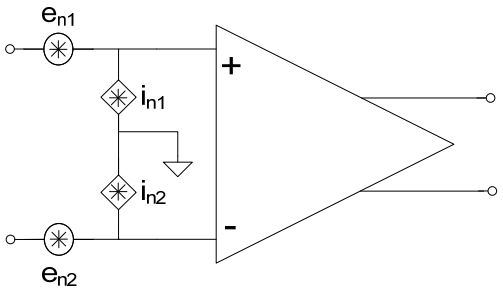

Figure 5-2. Equivalent input noise generators for a differential circuit.

However, we can profit from the symmetry of fully differential circuits: it is possible to analyze the differential half circuit to obtain the input equivalent noise generators of the two identical inputs: $e_{n1}=e_{n2}$ and $i_{n1}=i_{n2}$. The PSD of the output noise of each half circuit will be $e_{no1}=e_{no2}$ if the input is shorted to ground (no input parallel noise, only series noise e_n) and $i_{no1}=i_{no2}$ if the input is left open (no input series noise, only parallel noise i_n).

5.1.1.1 Equivalent input noise voltage (series noise)

To compute the input equivalent series noise source, usually referred as e_n (voltage source) or a, the differential half circuit of the preamplifier (see section 4.2.1.2) is drawn in Figure 5-3, including the noise generators corresponding to each element. In bipolar transistors both base and collector current show shot noise, represented by i^2_{sib} and i^2_{sic} respectively. Flicker noise in bipolar transistor has been found experimentally to be represented by current generator across internal base-emitter junction. This is conveniently combined with the shot noise generator in i^2_{sib}. Burst noise is not considered. Transistor base resistor r_b is a physical resistor and thus has thermal noise (e^2_{trb}). Note that resistors r_π and r_o in the model are fictitious resistors that are used for modeling purposes only, and they do not exhibit thermal noise. Current source $g_m v_{be}$ is also fictitious; all the noise contributions of the transistor are represented by e^2_{trb}, i^2_{sib} and i^2_{sic}. Polysilicon resistors R_E and R_C also exhibit thermal noise. Thermal noise of the PMT load resistor will be considered later on.

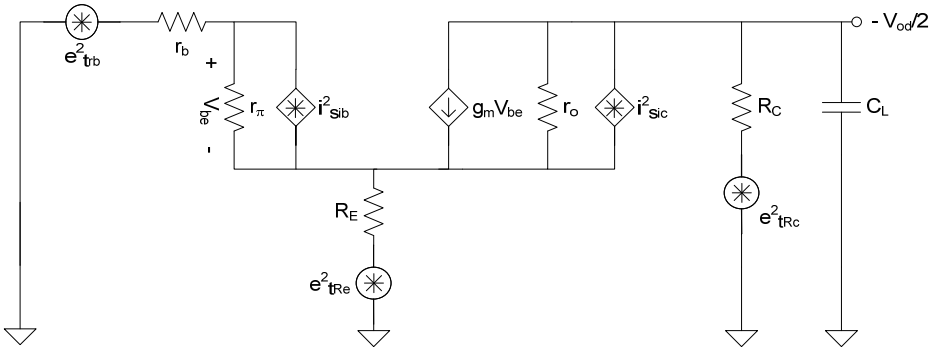

Figure 5-3. Differential half circuit of the preamplifier with noise sources. Input is shorted to ground to compute input series noise voltage e_n.

In practice current source and other preamplifier elements not present in differential half circuit of figure Figure 5-3 will also generate noise. However, as circuit is perfectly balanced, the current source represents a common mode signal and will not contribute to differential output [66].

We follow now the procedure described in section 2.4 (see also section 11.5 in [66]). We will consider that noise sources are uncorrelated. The input is shorted to ground so that the effect of an equivalent input current noise source will be null as it will be shorted. We compute the PSD of the total noise at the output e^2_{no} in such conditions. We will obtain the PSD e^2_n dividing e^2_{no} by the square of the amplitude of the voltage gain of the preamplifier.

Then, to find the contribution of each noise source to the noise at the output we use a signal generator in the same position and of the same type of each noise source. We can analyze each source by superposition, all the others independent voltage sources must be short-circuited whereas independent current sources must be open-circuited. As seen in section 4.2.1.2, the dominant pole of the preamplifier is at the output node. Therefore, we will only take into account the capacitance at the output node (C_L) and we will neglect the effect of the rest of parasitic capacitances.

For a voltage source v_{trb} placed in the same circuit position as the thermal noise from r_b (e^2_{trb}) and assuming that the output impedance r_o is high enough to neglect the influence of the voltage of the output node on the input mesh (base-emitter),

$$v_{tr_b} = \frac{v_{be}}{r_\pi} r_b + v_{be} + \left(\frac{v_{be}}{r_\pi} + g_m v_{be} \right) R_E \tag{5.2}$$

If $r_b/\beta << R_E$ and $1/\beta << 1$,

$$v_{be} \simeq \frac{v_{tr_b}}{1 + g_m R_E} \tag{5.3}$$

If the output impedance r_o is much higher than other impedances at the node,

$$-\frac{v_{od}}{2} \simeq -g_m v_{be} Z_C(j\omega) \qquad where \quad Z_C(j\omega) = R_C \,//\, \frac{1}{j\omega C_L} = \frac{1}{C_L\left(j\omega + \frac{1}{R_C C_L}\right)} \quad (5.4)$$

Using (5.3) and (5.4),

$$\frac{\frac{v_{od}}{2}}{v_{tr_b}} = \frac{g_m}{1+g_m R_E} Z_C(j\omega) \quad (5.5)$$

Therefore, the contribution to series output noise PSD of the base resistor thermal noise is,

$$e_{no_1}^2\Big|_{e_{tr_b}^2} = e_{no_2}^2\Big|_{e_{tr_b}^2} \simeq \left|\frac{g_m}{1+g_m R_E} Z_C(j\omega)\right|^2 e_{tr_b}^2 \quad (5.6)$$

In the same way, for a voltage source v_{rRe} placed in the same circuit position as the thermal noise from R_E (e^2_{tRe}), we have

$$0 = \frac{v_{be}}{r_\pi} r_b + v_{be} + \left(\frac{v_{be}}{r_\pi} + g_m v_{be}\right) R_E + v_{tR_e} \quad (5.7)$$

Isolating v_{be} on (5.7), assuming $R_E/r_\pi << 1$ and $r_b/r_\pi << 1$ and combining the result with (5.4),

$$\frac{\frac{v_{od}}{2}}{v_{tR_e}} = -\frac{g_m}{1+g_m R_E} Z_C(j\omega) \quad (5.8)$$

The contribution to series output noise PSD of the emitter resistor thermal noise is,

$$e_{no_1}^2\Big|_{e_{iR_e}^2} = e_{no_2}^2\Big|_{e_{iR_e}^2} \simeq \left|\frac{g_m}{1+g_m R_E} Z_C(j\omega)\right|^2 e_{tR_e}^2 \quad (5.9)$$

For a current source i_{sib} placed in the same circuit position as the shot and flicker noise generator related to i_b (i^2_{sib}), we have

$$0 = \left(\frac{v_{be}}{r_\pi} + i_{sib}\right) r_b + v_{be} + \left(\frac{v_{be}}{r_\pi} + i_{sib} + g_m v_{be}\right) R_E \quad (5.10)$$

Isolating v_{be} on (5.10), assuming $R_E/r_\pi << 1$ and $r_b/r_\pi << 1$, and combining the result with (5.4),

$$\frac{\frac{v_{od}}{2}}{i_{si_b}} = -(R_E + r_b)\frac{g_m}{1+g_m R_E} Z_C(j\omega) \quad (5.11)$$

The contribution to series output noise PSD of the shot and flicker noise of base current is,

$$e_{no_1}^2\Big|_{i_{si_b}^2} = e_{no_2}^2\Big|_{i_{si_b}^2} \simeq \left|(R_E + r_b)\frac{g_m}{1+g_m R_E} Z_C(j\omega)\right|^2 i_{si_b}^2 \quad (5.12)$$

For a voltage source v_{rRc} placed in the same circuit position as the thermal noise from R_C (e^2_{tRc}), we only have some influence on the input mesh through the output impedance r_o,

$$0 = \frac{v_{be}}{r_\pi} r_b + v_{be} + \left(\frac{v_{be}}{r_\pi} + g_m v_{be} + \frac{-\frac{v_{od}}{2}}{r_o}\right) R_E + v_{tR_e} \quad (5.13)$$

If $R_E/r_\pi << 1$ and $r_b/r_\pi << 1$,

$$v_{be} \simeq \frac{R_E}{r_o} \frac{-\frac{v_{od}}{2}}{1+g_m R_E} \tag{5.14}$$

The nodal equation at the output node is,

$$\frac{-\frac{v_{od}}{2}}{r_o} + g_m v_{be} + \frac{-\frac{v_{od}}{2} - v_{tR_c}}{R_C} + \frac{-\frac{v_{od}}{2}}{\frac{1}{j\omega C_L}} = 0 \tag{5.15}$$

Using (5.14) and with $r_o >> R_C$,

$$\frac{\frac{v_{od}}{2}}{v_{tR_c}} \simeq \frac{1}{R_C C_L} \frac{1}{j\omega + \frac{1}{R_C C_L}} = \frac{Z_C(j\omega)}{R_C} \tag{5.16}$$

Therefore, the contribution to series output noise PSD of the collector resistor thermal noise is,

$$e_{no_1}^2\Big|_{e_{tR_c}^2} = e_{no_2}^2\Big|_{e_{tR_c}^2} \simeq \left|\frac{Z_C(j\omega)}{R_C}\right|^2 e_{tR_c}^2 \tag{5.17}$$

For a current source i_{sic} placed in the same circuit position as the shot noise generator related to i_c (i^2_{sic}), we have

$$0 = \frac{v_{be}}{r_\pi} r_b + v_{be} + \left(\frac{v_{be}}{r_\pi} + i_{si_c} + g_m v_{be}\right) R_E \tag{5.18}$$

On the other hand, for the output node,

$$\frac{-\frac{v_{od}}{2}}{r_o} + g_m v_{be} + \frac{-\frac{v_{od}}{2}}{Z_C(j\omega)} + i_{si_c} = 0 \tag{5.19}$$

Isolating v_{be} on (5.18) (assuming $R_E/r_\pi << 1$ and $r_b/r_\pi << 1$) and v_{od} on (5.19), and combining the results,

$$\frac{\frac{v_{od}}{2}}{i_{si_c}} = \frac{1}{1+g_m R_E} Z_C(j\omega) \tag{5.20}$$

The contribution to series output noise PSD of the shot noise of collector current is,

$$e_{no_1}^2\Big|_{i_{si_c}^2} = e_{no_2}^2\Big|_{i_{si_c}^2} \simeq \left|\frac{Z_C(j\omega)}{1+g_m R_E}\right|^2 i_{si_c}^2 \tag{5.21}$$

The total output noise $e_{no1}=e_{no2}$ related to input series voltage noise source $e_{n1}=e_{n2}$ is

$$e_{no_1}^2 = e_{no_2}^2 \simeq \left|Z_C(j\omega)\right|^2 \left(\left|\frac{g_m}{1+g_m R_E}\right|^2 \left(e_{tr_b}^2 + e_{tR_e}^2\right) + \left|\frac{1}{R_C}\right|^2 e_{tR_c}^2 + \left|\frac{g_m(R_E+r_b)}{1+g_m R_E}\right|^2 i_{si_b}^2 + \left|\frac{1}{1+g_m R_E}\right|^2 i_{si_c}^2 \right) \tag{5.22}$$

As said before, the PSD of the input equivalent voltage noise is obtained dividing the PSD of the noise at the output when the input is shorted to ground by the square of the amplitude of the voltage gain of the DM half circuit,

$$e_{n1}^2 = e_{n2}^2 = \frac{e_{no1}^2}{\left|A_{DD}(j\omega)\right|^2} = \frac{e_{no2}^2}{\left|A_{DD}(j\omega)\right|^2} \qquad (5.23)$$

If the effect of non-dominant poles is neglected the DM voltage of the preamplifier is given by (5.5), then the PSD of equivalent input voltage noise at each input of the differential preamplifier is

$$e_{n_1}^2 = e_{n_2}^2 \simeq \left(e_{tr_b}^2 + e_{tR_e}^2\right) + \left|\frac{1+g_m R_E}{g_m R_C}\right|^2 e_{tR_c}^2 + \left(R_E + r_b\right)^2 i_{si_b}^2 + \left|\frac{1}{g_m}\right|^2 i_{si_c}^2 \qquad (5.24)$$

Note that voltage noise generator of R_C is divided by the square of the DC gain of the preamplifier and current shot noise generator of collector current by the square of the transconductance of the input transistor.

Now, we can evaluate expression (5.24) at a temperature T=300 K. The values for the model components are given in section 4.2.1. First, we will compute the value of each individual noise source. Parameters of the Flicker noise for base current are extracted from the Austriamicrosystems simulation model of the bipolar transistor, see appendix A. K_f corresponds to KF and A_f to AF. Being $i_c = I_{bias}/2 = 0.5$ mA, $g_m = i_C/(KT/q)$ is 0.02 S.

It is important to consider the multiplier effect in devices of the circuit, i.e. to take into account that one transistor is composed by several elementary devices to improve matching. It can readily shown that there is no difference for thermal and shot white noises, that is to say, the sum of the noise contribution of elementary devices equals the noise of the combination of the devices. This is not true any more for Flicker noise in base current as it depends on the DC bias current flowing through the base of each elementary device to the power of A_f. On that case we need to compute the sum of the PSD of each elementary device. For the transistors of the preamplifier the multiplicity is 4.

$$e_{tr_b}^2 = 4kT\,r_b = 4\left(1.38\cdot10^{-23}\,J/K\right)\left(300\,K\right)\left(180\,\Omega\right) \simeq 3\cdot10^{-18}\ \frac{\mathrm{V}^2}{\mathrm{Hz}}$$

$$e_{tR_e}^2 = 4kTR_E = 4\left(1.38\cdot10^{-23}\,J/K\right)\left(300\,K\right)\left(460\,\Omega\right) \simeq 7.7\cdot10^{-18}\ \frac{\mathrm{V}^2}{\mathrm{Hz}}$$

$$e_{tR_c}^2 = 4kTR_C = 4\left(1.38\cdot10^{-23}\,J/K\right)\left(300\,K\right)\left(2.4\,k\Omega\right) \simeq 40\cdot10^{-18}\ \frac{\mathrm{V}^2}{\mathrm{Hz}}$$

$$i_{si_b}^2 = 2q\frac{I_C}{\beta} + 4K_f\frac{\left(I_C/4/\beta\right)^{A_f}}{f} = 2\left(1.6\cdot10^{-19}\,C\right)\frac{500\,\mu A}{100} + 2(1.5\cdot10^{-16})\frac{\left(500\,\mu A/100\right)^{0.5}}{f} \simeq 1.6\cdot10^{-24} + \frac{6.6\cdot10^{-19}}{f}\ \frac{\mathrm{A}^2}{\mathrm{Hz}}$$

$$i_{si_c}^2 = 2qI_C = 2\left(1.602\cdot10^{-19}\,C\right)\left(500\,\mu A\right) \simeq 1.6\cdot10^{-22}\ \frac{\mathrm{A}^2}{\mathrm{Hz}}$$

(5.25)

It is interesting to note that the corner frequency f_{Cib}[u] for the base current noise is given by,

$$f_{Cib} = \frac{K_f\left(I_C/\beta\right)^{A_f-1}}{q} \simeq 400\ \mathrm{kHz} \qquad (5.26)$$

The value of the PSD of equivalent input voltage noise at each input of the differential preamplifier is

[u] Corner frequency f_{Cib} of base current noise is defined as the frequency where contribution of shot and flicker noise have the same value or the frequency where the PSD of the base current noise is twice (3dB) the value of such noise at high frequency (when flicker noise can be neglected compared to shot noise).

$$e_{n_1}^2 = e_{n_2}^2 \simeq \left(3{\cdot}10^{-18}\,\frac{V^2}{Hz} + 7.7{\cdot}10^{-18}\,\frac{V^2}{Hz} \right) + \left| \frac{1}{4.7} \right|^2 40{\cdot}10^{-18}\,\frac{\mathrm{V}^2}{\mathrm{Hz}} +$$

$$+ \left(460\,\Omega + 180\,\Omega\right)^2 \left(1.6{\cdot}10^{-24} + \frac{6.6{\cdot}10^{-9}}{f}\,\frac{A^2}{Hz} \right) + \left| \frac{1}{0.02\,S} \right|^2 1.6{\cdot}10^{-22}\,\frac{\mathrm{A}^2}{\mathrm{Hz}} \simeq \qquad (5.27)$$

$$\simeq 13.6{\cdot}10^{-18} + \frac{2.7{\cdot}10^{-13}}{f}\,\frac{\mathrm{V}^2}{\mathrm{Hz}}$$

We can also define a corner frequency f_{Cen} for the equivalent input voltage noise as,

$$f_{Cen} = \frac{\left(R_E + r_b\right)^2 2K_f \left(I_C / \beta \right)^{A_f}}{\left(e_{tr_b}^2 + e_{tR_e}^2 \right) + \left| \frac{1 + g_m R_E}{g_m R_C} \right|^2 e_{tR_c}^2 + \left(R_E + r_b\right)^2 2q\frac{I_C}{\beta} + \left| \frac{1}{g_m} \right|^2 i_{si_c}^2} \simeq 20\ kHz \qquad (5.28)$$

Figure 5-4 shows the result of the simulation of the PSD of the input referred noise voltage at each input of the preamplifier. As said before, it corresponds to series noise (e^2_{n1}=e^2_{n2}) when R_s=*0*. In noise simulations it is only possible to refer the noise to the input with a single source (voltage or current). Thus, voltage controlled sources are used and a factor $1/\sqrt{2}$ is applied in the gain to compensate for referring the noise to a single source.

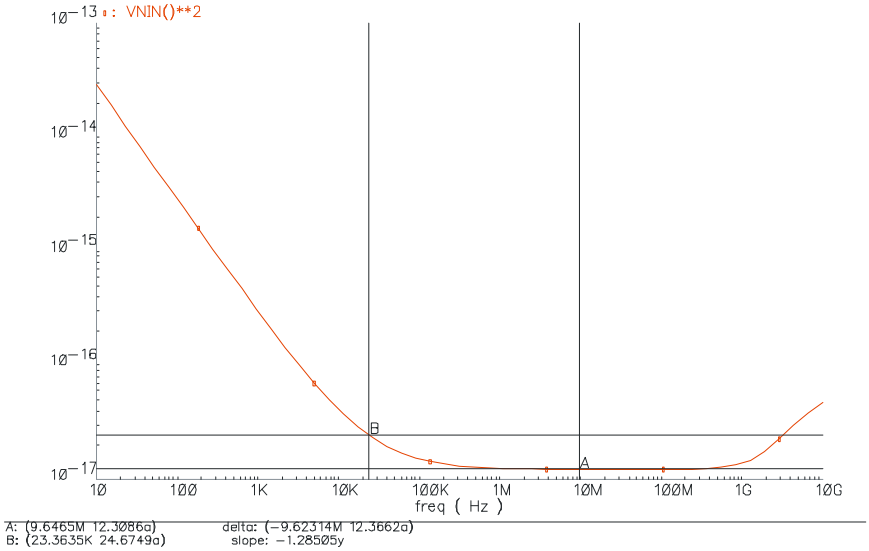

Figure 5-4. Spectre simulation of the PSD of the input referred noise voltage at each input (e^2_{n1}=e^2_{n2}) of the preamplifier.

According Figure 5-4 the value of the corner frequency f_{Cen} is 23.4 kHz and the PSD in the frequency band f_{Cen}<*f*<*1* GHz is flat with a value if $12.3{\cdot}10^{-18}$, it corresponds to the white noise term of e_n. Simulation results are in agreement with calculations (expression (5.27)) except for the increase in noise for frequencies above 1 GHz. For high frequencies the dominant pole model used for previous calculations is not valid any more, C_π and C_μ must be taken into account and the transfer function needed to weight the contribution of each noise source varies. The noise produced at the output (collector current and R_C) and on the output stage (emitter follower) is seen with no attenuation at the input because the gain of the differential stage drops.

Nevertheless the noise contribution at high frequencies is not very relevant as the preamplifier pole is at 200 MHz. In Figure 5-5 we see that the PSD at the output of the preamplifier related to series noise (with R_s=*0*) decreases according the DM gain of the preamplifier ($A_{DD}(j\omega)$). In the simulation we see the PSD of the two DM half circuits: e^2_{no1}+e^2_{no2}.

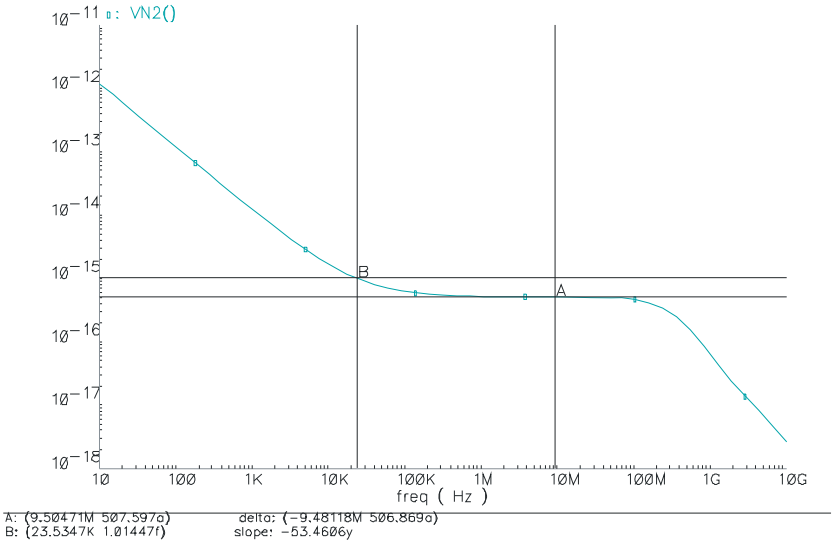

Figure 5-5. Spectre simulation of the PSD of the noise voltage at the DM output ($e^2_{no1}+e^2_{no2}$) of the preamplifier for the input series noise $e^2_{n1}+e^2_{n2}$ (with $R_s=0$).

The PSD in the frequency band $f_{Cen}<f<1$ GHz at the output can be easily computed using (5.23),

$$e^2_{no1}+e^2_{no2} \simeq \left(e^2_{n1}+e^2_{n2}\right)\left|A_{DD}(0)\right|^2 = 2e^2_n\left|A_{DD}(0)\right|^2 = 2{\cdot}13.6{\cdot}10^{-18}\left|4.6\right|^2\frac{V^2}{Hz} = 576{\cdot}10^{-18}\frac{V^2}{Hz} \qquad (5.29)$$

5.1.1.2 Equivalent input noise current (parallel noise)

To compute the input equivalent parallel noise source, usually referred as i_n (current source) or b, the differential half circuit of the preamplifier is drawn in Figure 5-6, including the noise generators corresponding to each element.

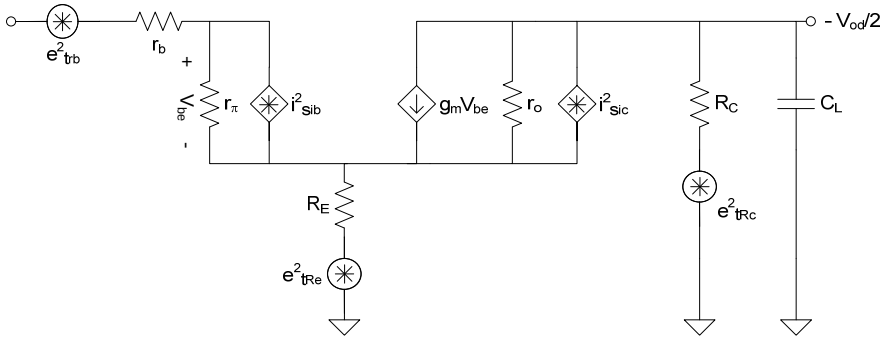

Figure 5-6. Differential half circuit of the preamplifier with noise sources. Input is left open to compute input parallel noise current i_n.

The input is left open so that the effect of an equivalent input voltage noise source will be null as one terminal of the source is open. We compute the PSD of the total noise at the output e_{no} in such conditions. We will obtain the PSD of the input equivalent noise current as

$$i^2_{n1} = i^2_{n2} = \frac{e^2_{no}}{\left|Z_{DD}(j\omega)\right|^2} \qquad (5.30)$$

where $Z_{DD}(j\omega)$ is the DM current to voltage gain (or transimpedance) of the preamplifier. It can be readily shown that,

$$Z_{DD}(j\omega) = Z_C(j\omega)\,g_m r_\pi = Z_C(j\omega)\,\beta \qquad (5.31)$$

To find the contribution to the output we use a signal generator in the same position and of the same type of a given noise source. We can analyze each source by using the superposition theorem. A voltage source v_{trb} placed in the same circuit position as the thermal noise from r_b (e^2_{trb}) has no effect because one terminal is open (for the same reason that we can neglect e_n).For a voltage source v_{rRe} placed in the same circuit position as the thermal noise from R_E (e^2_{tRe}) no current flows through r_π, thus $v_{be}=0$ and there is no current flowing through the voltage controlled current source representing transistor transconductance. Then, analyzing the output mesh,

$$\frac{\frac{v_{od}}{2}}{v_{tR_e}} = -\frac{Z_C(j\omega)}{r_o + R_E + Z_C(j\omega)} \tag{5.32}$$

The contribution to parallel output noise PSD of the emitter resistor thermal noise is,

$$e^2_{no_1}\Big|_{e^2_{tR_e}} = e^2_{no_2}\Big|_{e^2_{tR_e}} \simeq \left|\frac{Z_C(j\omega)}{r_o + R_E + Z_C(j\omega)}\right|^2 e^2_{tR_e} \tag{5.33}$$

For a voltage source v_{rRc} placed in the same circuit position as the thermal noise from R_C (e^2_{tRc}), same happens (no current flows through r_π). Then applying KVL to output mesh and considering,

$$\frac{-\frac{v_{od}}{2}}{r_o} + \frac{-\frac{v_{od}}{2} - v_{tR_c}}{R_C} + \frac{-\frac{v_{od}}{2}}{\frac{1}{j\omega C_L}} = 0 \tag{5.34}$$

with $r_o >> R_C$,

$$\frac{\frac{v_{od}}{2}}{v_{tR_c}} \simeq \frac{1}{R_C C_L}\frac{1}{j\omega + \frac{1}{R_C C_L}} = \frac{Z_C(j\omega)}{R_C} \tag{5.35}$$

Therefore, the contribution to parallel output noise PSD of the collector resistor thermal noise is,

$$e^2_{no_1}\Big|_{e^2_{tR_c}} = e^2_{no_2}\Big|_{e^2_{tR_c}} \simeq \left|\frac{Z_C(j\omega)}{R_C}\right|^2 e^2_{tR_c} \tag{5.36}$$

For a current source i_{sib} placed in the same circuit position as the shot and flicker noise generator related to i_b (i^2_{sib}), since no current flows through r_b we have

$$v_{be} = i_{sib} r_\pi \tag{5.37}$$

If $r_o >> Z_c(j\omega)$,

$$\frac{v_{od}}{2} = g_m v_{be} Z_C(j\omega) = g_m i_{sib} r_\pi Z_C(j\omega) = i_{sib}\beta Z_C(j\omega) \tag{5.38}$$

The contribution to series output noise PSD of the shot and flicker noise of base current is,

$$e^2_{no_1}\Big|_{i^2_{si_b}} = e^2_{no_2}\Big|_{i^2_{si_b}} \simeq \left|\beta Z_C(j\omega)\right|^2 i^2_{si_b} \tag{5.39}$$

In the same way, for the shot noise of the collector current,

$$e^2_{no_1}\Big|_{i^2_{si_c}} = e^2_{no_2}\Big|_{i^2_{si_c}} \simeq \left|Z_C(j\omega)\right|^2 i^2_{si_c} \tag{5.40}$$

and the total output noise $e_{no1}=e_{no2}$ related to the input parallel current noise source $i_{n1}=i_{n2}$ is

$$e_{no_1}^2 = e_{no_2}^2 \simeq \left|Z_C\left(j\omega\right)\right|^2 \left(\left| \frac{1}{r_o + R_E + Z_C\left(j\omega\right)} \right|^2 e_{tR_e}^2 + \left| \frac{1}{R_C} \right|^2 e_{tR_c}^2 + \left|\beta\right|^2 i_{si_b}^2 + i_{si_c}^2 \right) \quad (5.41)$$

Using (5.30) the equivalent input noise current is,

$$i_{n_1}^2 = i_{n_1}^2 \simeq \left(\left| \frac{1}{\beta\left(r_o + R_E + Z_C\left(j\omega\right)\right)} \right|^2 e_{tR_e}^2 + \left| \frac{1}{\beta R_C} \right|^2 e_{tR_c}^2 + i_{si_b}^2 + \left| \frac{1}{\beta} \right|^2 i_{si_c}^2 \right) \quad (5.42)$$

We can evaluate this expression, using (5.25), neglecting the contribution of the emitter resistance noise because it is divided by a very large impedance r_o and taking into account that $\beta \approx 100$,

$$\begin{aligned} i_{n_1}^2 = i_{n_1}^2 &\simeq \left(\left| \frac{1}{\beta R_C} \right|^2 e_{tR_c}^2 + i_{si_b}^2 + \left| \frac{1}{\beta} \right|^2 i_{si_c}^2 \right) \simeq \left(\left| \frac{1}{100\ 2K4\ \Omega} \right|^2 40{\cdot}10^{-18}\ \frac{\mathrm{V}^2}{\mathrm{Hz}} \right) + \\ &+ \left(1.6{\cdot}10^{-24} + \frac{6.6{\cdot}10^{-19}}{f}\ \frac{A^2}{Hz} \right) + \left(\left| \frac{1}{100} \right|^2 1.6{\cdot}10^{-22}\ \frac{\mathrm{A}^2}{\mathrm{Hz}} \right) \simeq \quad (5.43) \\ &\simeq 1.62{\cdot}10^{-24} + \frac{6.6{\cdot}10^{-19}}{f}\ \frac{\mathrm{A}^2}{\mathrm{Hz}} \end{aligned}$$

The base current noise dominates total equivalent parallel noise and the corner frequency related to the Flicker noise will be given by the corner frequency of the base current noise (5.26).

Simulation of parallel noise is trickier than simulation of series noise because the contribution of parallel noise is dominant at the output only when the source resistance is high enough. As seen in section 2.4, the parallel noise dominates when R_S is much higher than the ratio e_n/i_n, which is defined as the optimal source resistance R_{OP},

$$R_{OP} = \frac{e_n}{i_n} \simeq 3\ k\Omega \quad (5.44)$$

In addition R_S is needed to bias the input differential pair of the preamplifier and its value must be adequate to set a correct DC bias point. Figure 5-7 shows the PSD of the input referred noise current at each input of the preamplifier for different values of source resistance R_S. Note that for $R_S > 3$ kΩ curves start to converge and approximate to the definition of parallel noise ($i^2_{n1}=i^2_{n2}$). For those curves, both white noise PSD value and Flicker noise corner frequency are in good agreement with (5.43) for $R_S > 3$ kΩ. For simulations of input equivalent noise current, generation of thermal noise in R_S is disabled.

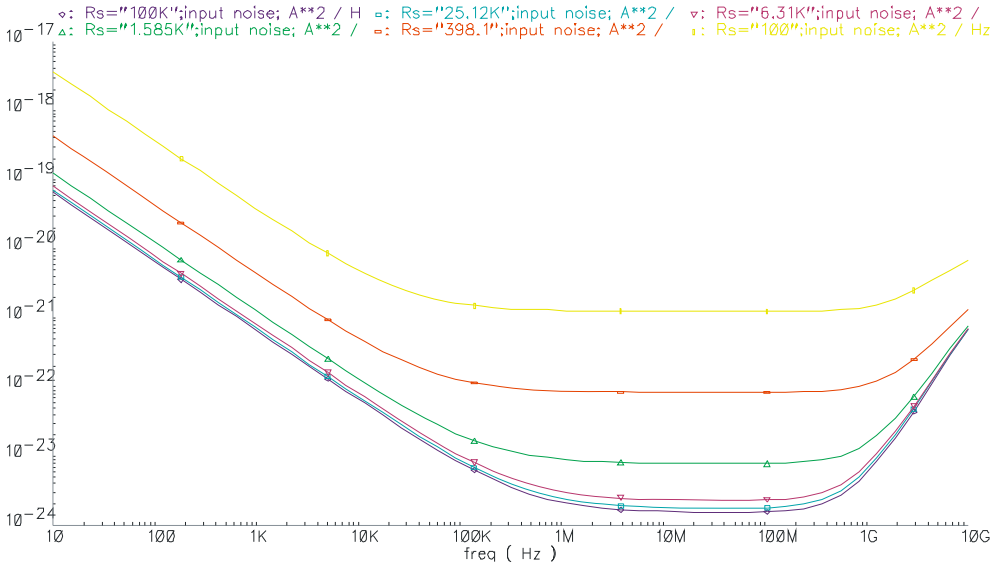

Figure 5-7. Spectre simulation of the PSD of the input referred noise current at each input of the preamplifier for different values of source resistance R_S.

Looking at the PSD of the noise at the output of the preamplifier as a function of source resistance R_S in Figure 5-8 we can see that for $R_S<3$ kΩ the noise has little dependence on R_S and it corresponds to the series noise generators ($e^2_{n1}=e^2_{n2}$), whereas for $R_S>3$ kΩ the PSD of the noise depends almost linearly with R_S and it corresponds to parallel noise generators ($i^2_{n1}=i^2_{n2}$). Large values of R_S displace the pole related to the input capacitance of the preamplifier to low frequencies.

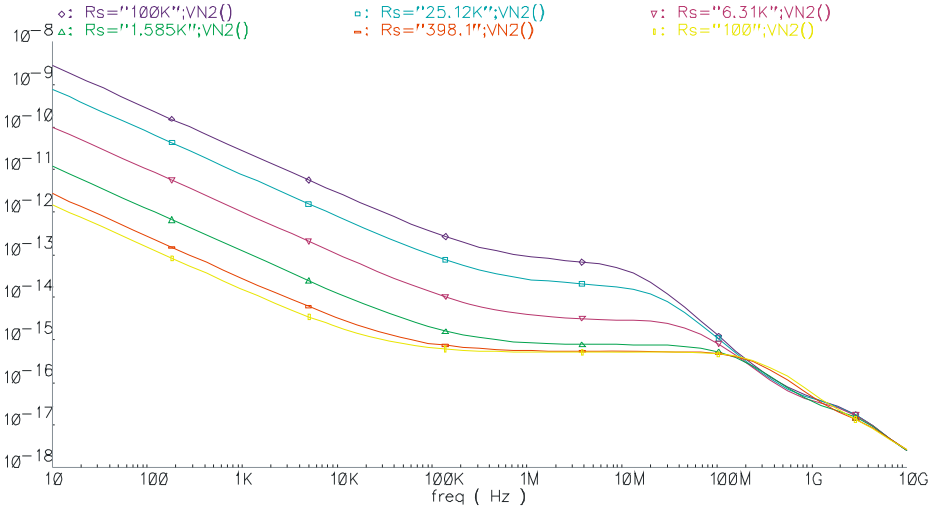

Figure 5-8. Spectre simulation of the PSD of the noise voltage at the DM output ($e^2_{no1}+e^2_{no2}$) of the preamplifier for different values of source resistance R_S.

In Figure 5-7 we see that the input-referred noise rises at high frequencies because the transistor current gain begins to fall, i.e. β is not constant but depends on frequency (see section in 11.5 in [66]). The fall of β with frequency can be understood from the small-signal model of the transistor as an effect related to C_π and C_μ which starts to be relevant at high frequency (see section in 1.4.8 in [66]). This effect is analyzed in [66] for the bipolar parallel noise and it is shown that its spectrum rises as f^2 at high frequencies with a corner frequency $f_b = f_T \Big/ \sqrt{\beta_{LF}} \simeq 1.2$ GHz .

5.1.2 PSD of the total input equivalent noise.

The value of the source impedance and the way it is connected to the input of the preamplifier greatly influence the noise performance (see section 2.4.2). Figure 5-9 shows the input of the preamplifier with source impedance and noise generators. R_s is the load resistance of the MaPMT and has a nominal value of 470 Ω.

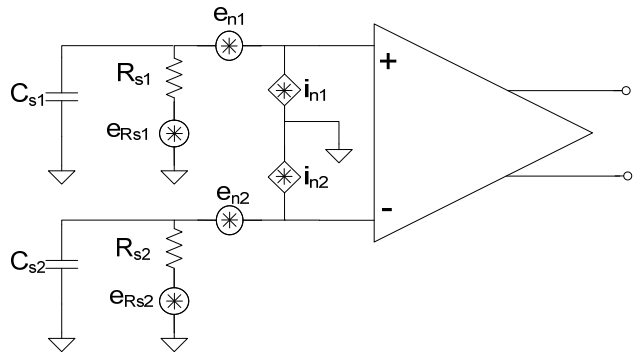

Figure 5-9. Input of the preamplifier with source impedance and noise generators.

Although the anode of the MaPMT is connected only to one of the preamplifier inputs, the same load is connected to the other input to keep the circuit balanced. The PSD of the thermal noise of R_s is denoted by e^2_{Rs}. It is also important to consider the parasitic capacitance at the input of the preamplifier C_s. Main contributions for C_s are the stray capacitance of the PCB, the capacitance at the anode of the PMT, the input capacitance of the preamplifier and the one of the input pads, being 10 pF an approximated value for C_s (see appendix C).

Now, we will combine the effect of all the noise sources in Figure 5-9 to obtain the PSD of the total input equivalent noise voltage e^2_{ni}. Equivalent noise will be evaluated as a voltage because we have a high input impedance preamplifier with a voltage transfer function $A_{DD}(j\omega)$; thus, noise δ impulses will be voltage δ impulses and not current δ impulses as use to be considered for nuclear instrumentation using low input impedance preamplifiers such as CSPs. We will follow the same procedure used in last section to obtain the contribution of each source to the total equivalent noise voltage evaluated at the input of the preamplifier.

For the series noise generators $e_{n1}=e_{n2}$ the contribution to the PSD of the equivalent input noise is,

$$e^2_{ni}\Big|_{e^2_{n1}} = e^2_{ni}\Big|_{e^2_{n2}} \simeq \left|\frac{Z_I(j\omega)}{Z_I(j\omega)+Z_S(j\omega)}\right|^2 e^2_n \simeq\Big|_{Z_S(j\omega)\ll Z_I(j\omega)} e^2_n \qquad (5.45)$$

where the source impedance is

$$Z_S(j\omega) = \frac{R_S}{\frac{j\omega}{\omega_S}+1} \qquad (5.46)$$

with $\omega_S=R_sC_s$ and $Z_I(j\omega)$ being the input impedance of the preamplifier. If $Z_I(j\omega)$ is much higher than the source impedance series noise contributes directly to the total input equivalent noise.

The contribution of the parallel noise generators $i_{n1}=i_{n2}$ is,

$$e^2_{ni}\Big|_{i^2_{n1}} = e^2_{ni}\Big|_{i^2_{n2}} \simeq \left|Z_S(j\omega)\right|^2 i^2_n \qquad (5.47)$$

According to (5.46) the contribution of parallel noise to the output has a low pass characteristic with a corner frequency $f_s=\omega_s/2\pi\approx 40$ MHz.

And for the PSD of the thermal noise of the MaPMT load resistor,

$$e_{ni}^2\Big|_{e_{R_{S1}}^2} = e_{ni}^2\Big|_{e_{R_{S2}}^2} \simeq \left|\frac{1}{\frac{j\omega}{\omega_S}+1}\right|^2 e_{R_S}^2 \tag{5.48}$$

Therefore, the PSD of the total equivalent input noise is,

$$e_{ni}^2 \simeq \left(e_{n_1}^2 + e_{n_2}^2\right) + \left|\frac{R_S}{\frac{j\omega}{\omega_S}+1}\right|^2 \left(i_{n1}^2 + i_{n2}^2\right) + \left|\frac{1}{\frac{j\omega}{\omega_S}+1}\right|^2 \left(e_{R_{S1}}^2 + e_{R_{S1}}^2\right) \tag{5.49}$$

Considering that all the elements of the differential circuit are matched,

$$e_{ni}^2 \simeq 2\left(e_n^2 + \left|\frac{R_S}{\frac{j\omega}{\omega_S}+1}\right|^2 i_n^2 + \left|\frac{1}{\frac{j\omega}{\omega_S}+1}\right|^2 e_{R_S}^2\right) \simeq\Big|_{\omega \ll \omega_S} 2\left(e_n^2 + R_S^2 i_n^2 + e_{R_S}^2\right) \tag{5.50}$$

The PSD of the thermal noise of the source resistance is at 300K,

$$e_{tR_S}^2 = 4kTR_S = 4\left(1.38{\cdot}10^{-23} J/K\right)\left(300\,K\right)\left(470\,\Omega\right) \simeq 7.8{\cdot}10^{-18}\,\frac{V^2}{Hz} \tag{5.51}$$

We will now evaluate the PSD of the equivalent input noise at low frequency ($\omega << \omega_s$),

$$\begin{aligned} e_{ni}^2 &\simeq\Big|_{\omega \ll \omega_S} 2\left(\left(13.6{\cdot}10^{-18} + \frac{2.7{\cdot}10^{-13}}{f}\,\frac{V^2}{Hz}\right) + \left(470\,\Omega\right)^2\left(1.62{\cdot}10^{-24} + \frac{6.6{\cdot}10^{-19}}{f}\,\frac{A^2}{Hz}\right) + 7.8{\cdot}10^{-18}\,\frac{V^2}{Hz}\right) \simeq \\ &\simeq 2\left(\left(13.6{\cdot}10^{-18} + \frac{2.7{\cdot}10^{-13}}{f}\,\frac{V^2}{Hz}\right) + \left(3.6^{-19} + \frac{14.7{\cdot}10^{-14}}{f}\,\frac{V^2}{Hz}\right) + 7.8{\cdot}10^{-18}\,\frac{V^2}{Hz}\right) \simeq \\ &\simeq 43.5{\cdot}10^{-18} + \frac{8.34{\cdot}10^{-13}}{f}\,\frac{V^2}{Hz} \end{aligned} \tag{5.52}$$

From (5.52) it is clear that the contribution of the parallel noise is one order of magnitude smaller than the contribution of series and source noise due to the relatively small value of the source resistance.

We can approximate the corner frequency f_{Ceni} for the equivalent input voltage Flicker noise as,

$$f_{C_{eni}} \simeq \frac{\left(\left(R_E + r_b\right)^2 + R_S^2\right) 2K_f \left(I_C \big/ \beta\right)^{A_f}}{\left(e_{tr_b}^2 + e_{tR_e}^2 + e_{R_S}^2\right) + \left|\frac{1+g_m R_E}{g_m R_C}\right|^2 e_{tR_c}^2 + \left(\left(R_E + r_b\right)^2 + R_S^2\right) 2q\frac{I_C}{\beta} + \left|\frac{1}{g_m}\right|^2 i_{si_c}^2} \simeq 20\ \text{kHz} \tag{5.53}$$

Figure 5-10 shows the PSD of the total equivalent input noise voltage with R_S=*470* Ω. The value of the white noise term is $44{\cdot}10^{-18}$ V^2/Hz, close to calculations. However, the corner frequency f_{Ceni} is 50 % higher than expected. This means that the contribution of Flicker noise is 50 % higher than expected. So far all noise sources have been considered uncorrelated which is clearly false if we examine expressions for e_n and i_n noise generators, all of them depend on the same generators. If contributions of e_n and i_n are not comparable (if one is much higher than the other one) we can perform the quadratic sum without much error. This was the case for the computation of series and parallel noise because R_S had extreme values, and it is also true if we compare the contribution of

white terms of e_n and i_n in (5.52). It is not true for *1/f* terms in (5.52) which dominate at low frequency, we should consider correlation because both depend on Flicker noise of the base current and this is a reason for the excess in Flicker noise in simulation respect to (5.52).

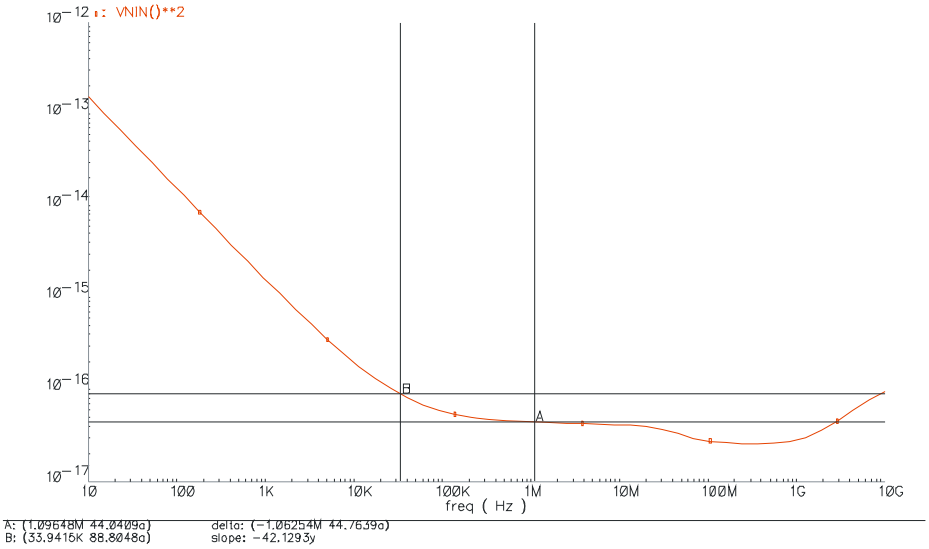

Figure 5-10. Simulation of the PSD of the total equivalent input noise voltage e^2_{ni} with R_S=*470* Ω.

As said in section 2.4 the combination of two correlated processes is:

$$S_o^2(f) \simeq \left|G_{S_{X_1}}(f)\right|^2 S_{X_1}(f) + \left|G_{S_{X_2}}(f)\right|^2 S_{X_2}(f) + 2\,\mathrm{cov}\left(\sqrt{S_{X_1}(f)}, \sqrt{S_{X_2}(f)}\right)\left|G_{S_{X_1}}(f)\right|\left|G_{S_{X_2}}(f)\right| \tag{5.54}$$

Therefore, expression (5.50) must be redefined as,

$$e_{ni}^2 \simeq 2\left(e_n^2 + \left|\frac{R_S}{\frac{j\omega}{\omega_S}+1}\right|^2 i_n^2 + \left|\frac{1}{\frac{j\omega}{\omega_S}+1}\right|^2 e_{R_S}^2 + 2\,\mathrm{cov}\left(e_n^2, i_n^2\right)\right) \tag{5.55}$$

Recalling expressions for e_n,

$$e_{n_1}^2 = e_{n_2}^2 \simeq \left(e_{tr_b}^2 + e_{tR_e}^2\right) + \left|\frac{1+g_m R_E}{g_m R_C}\right|^2 e_{tR_c}^2 + \left(R_E + r_b\right)^2 i_{si_b}^2 + \left|\frac{1}{g_m}\right|^2 i_{si_c}^2 \tag{5.56}$$

And for i_n,

$$i_{n_1}^2 = i_{n_1}^2 \simeq \left(\left|\frac{1}{\beta R_C}\right|^2 e_{tR_c}^2 + i_{si_b}^2 + \left|\frac{1}{\beta}\right|^2 i_{si_c}^2 \right) \tag{5.57}$$

It becomes clear that there are terms in e_n and i_n that depend on base current, collector current and collector resistor noise. Therefore correlation must be considered for those terms, which are fully correlated. As said before, if X and Y are fully correlated real-valued random variables,

$$\mathrm{cov}\left(S_{X_1}(f), S_{X_2}(f)\right) = S_{X_1}(f) S_{X_2}(f) \tag{5.58}$$

Therefore,

$$e_{ni}^2 \simeq 2\left(\left(e_{tr_b}^2 + e_{tR_e}^2\right) + \left|\frac{1+g_m R_E}{g_m R_C}\right|^2 e_{tR_c}^2 + \left(R_E + r_b\right)^2 i_{si_b}^2 + \left|\frac{1}{g_m}\right|^2 i_{si_c}^2 + \left|\frac{R_S}{\frac{j\omega}{\omega_S}+1}\right|^2 \left(\left|\frac{1}{\beta R_C}\right|^2 e_{tR_c}^2 + i_{si_b}^2 + \left|\frac{1}{\beta}\right|^2 i_{si_c}^2 \right) + \left|\frac{1}{\frac{j\omega}{\omega_S}+1}\right|^2 e_{R_S}^2 + \right.$$

$$\left. +2\left(R_E + r_b\right) \left|\frac{R_S}{\frac{j\omega}{\omega_S}+1}\right| \sqrt{i_{si_b}^2}\sqrt{i_{si_b}^2} + 2\left|\frac{1}{g_m}\right|\left|\frac{1}{\beta}\right| \left|\frac{R_S}{\frac{j\omega}{\omega_S}+1}\right| \sqrt{i_{si_c}^2}\sqrt{i_{si_c}^2} + \left|\frac{1}{\beta R_C}\right| \left|\frac{R_S}{\frac{j\omega}{\omega_S}+1}\right| \left|\frac{1+g_m R_E}{g_m R_C}\right| \sqrt{e_{tR_c}^2} \right) =$$

$$= 2\left(\left(e_{tr_b}^2 + e_{tR_e}^2\right) + \left|\frac{1}{\frac{j\omega}{\omega_S}+1}\right|^2 e_{R_S}^2 + \left(\left|\frac{1+g_m R_E}{g_m R_C}\right| + \left|\frac{1}{\beta R_C}\right| \left|\frac{R_S}{\frac{j\omega}{\omega_S}+1}\right| \right)^2 e_{tR_c}^2 + \left(R_E + r_b + \left|\frac{R_S}{\frac{j\omega}{\omega_S}+1}\right| \right)^2 i_{si_b}^2 + \left(\left|\frac{1}{g_m}\right| + \left|\frac{1}{\beta}\right| \left|\frac{R_S}{\frac{j\omega}{\omega_S}+1}\right| \right)^2 i_{si_c}^2 \right.$$

(5.59)

It can be readily shown that we would achieve the same result analyzing directly the preamplifier noise circuit adding the source impedance $Z_S(\omega)$.

The white noise part of the total input noise is, for $\omega << \omega_S$,

$$e_{ni\_white}^2 \simeq_{\omega \ll \omega_S} 2\left(\left(e_{tr_b}^2 + e_{tR_e}^2 + e_{R_S}^2\right) + \left(\left|\frac{1+g_m R_E}{g_m R_C}\right| + \left|\frac{R_S}{\beta R_C}\right| \right)^2 e_{tR_c}^2 + \left(R_E + r_b + R_S\right)^2 2q\frac{I_C}{\beta} + \left(\left|\frac{1}{g_m}\right| + \left|\frac{R_S}{\beta}\right| \right)^2 i_{si_c}^2 \right) =$$

$$= 2\left(3\cdot 10^{-18} + 7.7\cdot 10^{-18} + 7.8\cdot 10^{-18}\ \frac{V^2}{Hz} + \left(\frac{1}{4.7} + \frac{1}{500}\right)^2 40\cdot 10^{-18}\ \frac{V^2}{Hz} \right) +$$

$$+ \left(460\ \Omega + 180\ \Omega + 470\ \Omega\right)^2 \left(1.62\cdot 10^{-24}\ \frac{A^2}{Hz} \right) + \left(\frac{1}{0.02\ S} + \frac{1}{0.2\ S} \right)^2 \left(1.6\cdot 10^{-22}\ \frac{A^2}{Hz} \right) \simeq 46\cdot 10^{-18}\ \frac{\mathrm{V}^2}{\mathrm{Hz}}$$

(5.60)

As said before, the effect of the correlation is minimal because the thermal noise of r_b, R_E, and R_s of e_n dominates by far. For the Flicker part of the total input noise,

$$e_{ni\_Flicker}^2 \simeq_{\omega \ll \omega_S} 2\left(\left(R_E + r_b + R_S\right)^2 \frac{2K_f \left(I_C / \beta\right)^{A_f}}{f} \right) = \frac{16.2\cdot 10^{-13}}{f}\ \frac{\mathrm{V}^2}{\mathrm{Hz}} \quad (5.61)$$

And the corner frequency f_{Ceni} for the equivalent input voltage Flicker noise is now in better agreement with simulations (Figure 5-10),

$$f_{C_{eni}} \simeq \frac{\left(R_E + r_b + R_S\right)^2 2K_f \left(I_C / \beta\right)^{A_f}}{\left(e_{tr_b}^2 + e_{tR_e}^2 + e_{R_S}^2\right) + \left(\left|\frac{1+g_m R_E}{g_m R_C}\right| + \left|\frac{R_S}{\beta R_C}\right| \right)^2 e_{tR_c}^2 + \left(R_E + r_b + R_S\right)^2 2q\frac{I_C}{\beta} + \left(\left|\frac{1}{g_m}\right| + \left|\frac{R_S}{\beta}\right| \right)^2 i_{si_c}^2} \simeq 35\ \mathrm{kHz}$$

In Figure 5-10 we have also seen the effect of ω_s pole. The effect is mainly on the thermal noise component of the source resistance, as can be seen from Figure 5-11. When the thermal noise generator in of R_S is disabled the effect of the ω_s pole is almost negligible, it only affects input

equivalent noise current term, whose white term is negligible compared to input equivalent voltage noise term and source resistance thermal noise term.

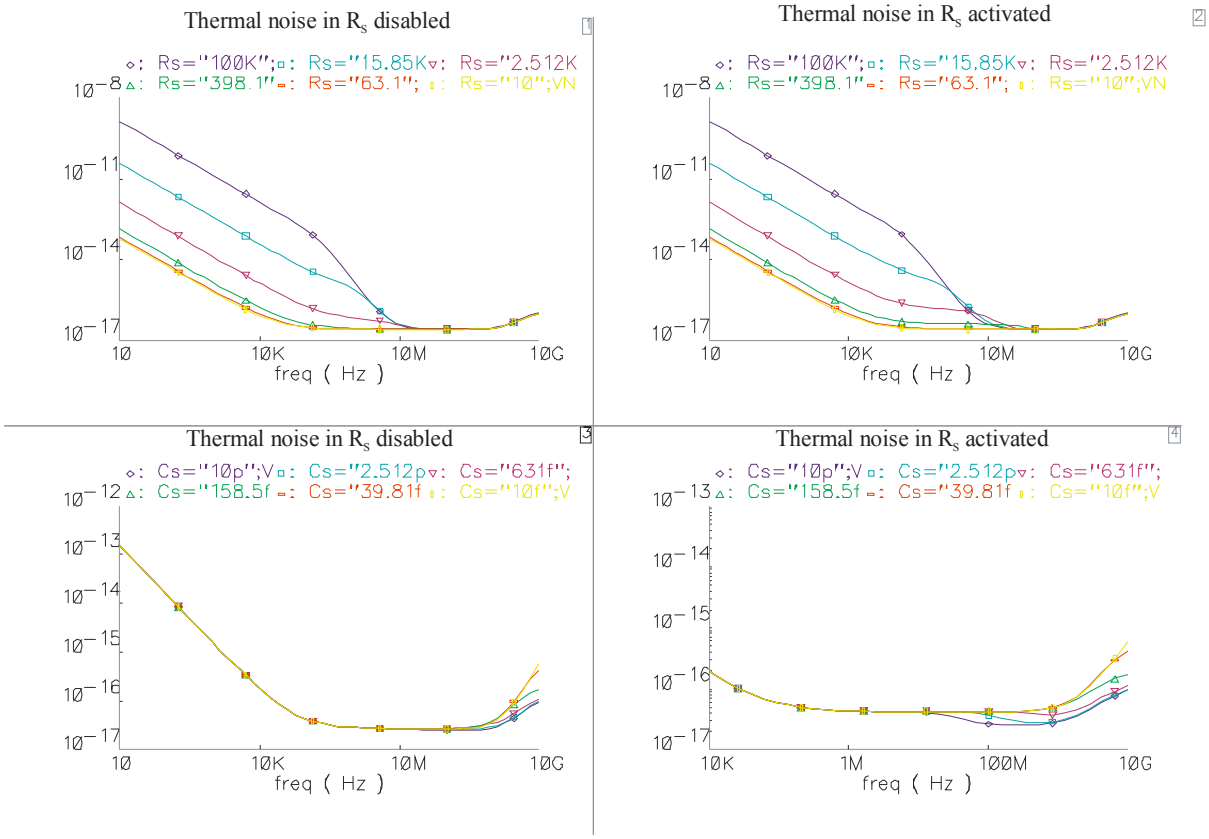

Figure 5-11. Simulation of the PSD of the total equivalent input noise voltage (e^2_{ni}) for several values of R_S (top) and of C_S (bottom) and with the thermal noise generator in of R_S activated (right) or disabled (left).

5.1.3 Output noise after shaping

The transfer function of the gated integrator has been studied in section 4.2.2.3 for the integration state. Nevertheless, the effect of finite width of the gate has to be taken into account to evaluate effect of this shaper on the noise. Whereas noise impulses are not related to the gate, the signal is synchronized with the gate and the output response of the integrator is just the integral of the input signal at ΔT=25 ns. As said before we can study the system either in time domain or in frequency domain.

5.1.3.1 Time domain analysis

The time domain analysis technique for time variant shapers has been summarized in section 2.6.5. Indeed the ASD responds exactly to the architecture presented on this section: a gated integrator as time variant with shaping before the gate *p(t)*. Transfer function *p(t)* is defined as the response at the gated integrator input (preamplifier output) to a unit δ noise impulse. It depends both on the preamplifier transfer function and on the source impedance. As said before, current noise and source resistance noise must be translated to series noise because we work with a voltage preamplifier (high input impedance). Then, using (5.50) we obtain the PSD at the output of the preamplifier,

$$e_{no}^2 \simeq 2\left|A_{DD}(s)\right|^2\left(e_n^2+\left|\frac{R_S}{\frac{j\omega}{\omega_S}+1}\right|^2 i_n^2+\left|\frac{1}{\frac{j\omega}{\omega_S}+1}\right|^2 e_{R_S}^2\right) \tag{5.62}$$

Thus from (5.62), the response to a δ impulse of a series generator $p_{en1}(t)$ or $p_{en2}(t)$ is,

$$p_{en1}(t)=p_{en1}(t)\simeq L^{-1}\left\{A_{DD}(s)\right\}\simeq L^{-1}\left\{\frac{g_m R_C}{(1+g_m R_E)}\frac{1}{\tau_C}\frac{1}{\left(s+\frac{1}{\tau_C}\right)}\right\}=\frac{g_m R_C}{(1+g_m R_E)}\frac{1}{\tau_C}e^{-\frac{t}{\tau_C}}u(t) \tag{5.63}$$

where $\tau_C=R_C C_L=1/2\pi f_C=600\ ps$ (f_C is the bandwidth of the preamplifier). In the same way, for the parallel noise generators $p_{in1}(t)$ or $p_{in2}(t)$,

$$p_{in1}(t)=p_{in1}(t)\simeq L^{-1}\left\{\frac{g_m R_C R_S}{(1+g_m R_E)}\frac{1}{\tau_C\tau_S}\frac{1}{\left(s+\frac{1}{\tau_C}\right)\left(s+\frac{1}{\tau_S}\right)}\right\} \tag{5.64}$$

where $\tau_S=R_S C_S\approx 4\ ns$ is the time constant associated to the source impedance, as $\tau_S>>\tau_C$ the time constant of the source impedance dominates and,

$$p_{in1}(t)=p_{in1}(t)\simeq L^{-1}\left\{\frac{g_m R_C R_S}{(1+g_m R_E)}\frac{1}{\tau_S}\frac{1}{\left(s+\frac{1}{\tau_S}\right)}\right\}=\frac{g_m R_C R_S}{(1+g_m R_E)}\frac{1}{\tau_S}e^{-\frac{t}{\tau_S}}u(t) \tag{5.65}$$

In the same way, for source resistance noise generators $p_{eRs1}(t)$ or $p_{eRs2}(t)$,

$$\begin{aligned} p_{e_{R_{S1}}}(t)=p_{e_{R_{S2}}}(t)&\simeq L^{-1}\left\{\frac{g_m R_C}{(1+g_m R_E)}\frac{1}{\tau_C\tau_S}\frac{1}{\left(s+\frac{1}{\tau_C}\right)\left(s+\frac{1}{\tau_S}\right)}\right\}\simeq\Big|_{\tau_C\ll\tau_S}\\ &\simeq L^{-1}\left\{\frac{g_m R_C}{(1+g_m R_E)}\frac{1}{\tau_S}\frac{1}{\left(s+\frac{1}{\tau_S}\right)}\right\}=\frac{g_m R_C}{(1+g_m R_E)}\frac{1}{\tau_S}e^{-\frac{t}{\tau_S}}u(t)\end{aligned} \tag{5.66}$$

The impulse response of the prefilter for all the noise sources is of the type $\frac{1}{\tau}e^{-\frac{t}{\tau}}$, we will continue the analysis of the weighting function corresponding to a generic impulse response of the form,

$$p(t)=A\frac{1}{\tau}e^{-\frac{t}{\tau}}u(t) \tag{5.67}$$

where A is the DC gain for a given noise source.

Now to compute the weighting function we will follow the method presented in section 2.6.5 for a gated integrator. We can define the weighting function $w(t_0,t_i)$ by parts. *The Noise Weighting function $w(t_0,t_i)$ is defined as the output at the measuring time $t_0= t_1+T$ where T is which results from a unit*

impulse $\delta(t_0-t_i)$ delivered by an input noise generator at a time t_i. Integration time T is 25 nanoseconds and t_1 is the time where MIP signal arrives and integration starts.

The integrator is approximated by an ideal integrator with constant $1/\tau_i$ (4.131). As the prefilter function of (5.67) has infinite duration, we consider only three cases instead of the four cases considered in section 2.6.5 for a prefilter with impulse response of finite duration:

1. If the current impulse is produced after the end of the integration ($t_i>t_1+T$) the contribution is null: $w(t_0,t_i)=0$.
2. If the current impulse is produced at a t_i before the start of the integration t_1 ($t_i \leq t_1$) part of the tail of pulse is inside the integration window:

$$w(t_0=t_1+T,t_i)=\frac{A}{\tau_i}\int_{t_1-t_i}^{t_1+T-t_i} p(x)\,dx \simeq \frac{A}{\tau_i}\left(e^{-\frac{(t_1-t_i)}{\tau}}-e^{-\frac{(t_1+T-t_i)}{\tau}}\right) \qquad -\infty < t_i \leq t_1 \qquad (5.68)$$

3. If the current impulse arrives after start of integration ($t_i>t_1$), only the initial part of the pulse is integrated and contributes to the noise response at $t_0=t_1+T$:

$$w(t_0=t_1+T,t_i)=\frac{A}{\tau_i}\int_{0}^{t_1+T-t_i} p(x)\,dx \simeq \frac{A}{\tau_i}\left(1-e^{-\frac{(t_1+T-t_i)}{\tau}}\right) \qquad t_1 < t_i \leq t_1+T \qquad (5.69)$$

Using the step function $u(t)$ we could define also the weighting function of a gated integrator as,

$$w(t_0=t_1+T,t_i)=\frac{1}{\tau_i}\int_{-\infty}^{+\infty} p(t-t_i)g(t)\,dt \qquad (5.70)$$

Where the gate function is $g(t)=u(t-t_1)-u(t-t_1-T)$. Expression (5.70) is very similar to the convolution function, although it is not the same because in convolution operation the integral is performed over the mirror of $p(t)$, over $p(t_i-t)$. Unfortunately relationship (5.70) does not help to determine the weighting function in time domain, but it will be useful in frequency domain.

The normalized noise weighting function is drawn in Figure 5-12.

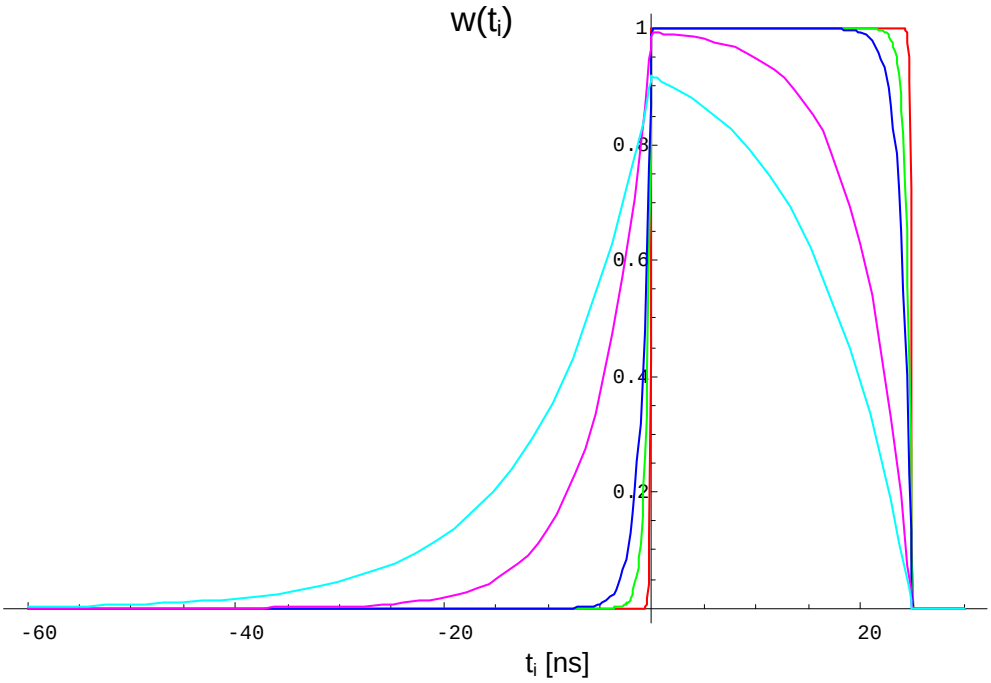

Figure 5-12. Normalized weighting function for t_1=0, T=25 ns and for different values of the prefilter time constant τ. Light blue τ=10 ns, magenta τ=5ns, dark blue τ=1ns, green τ=0.5 ns and red τ=0.1 ns.

Using theory of section 2.5.2, the variance of the signal at the output of the integrator at the measurement time $t_0=t_1+T$ becomes

$$\sigma^2_{white}=\frac{1}{2}G_{xx\_white}\int_{-\infty}^{+\infty}w^2(t)\,dt \qquad (5.71)$$

Where G_{xx_white} or $e^2_{ni\_white}$ is the white component of the PSD of the total input equivalent noise $e^2_{ni}(f)$. We perform the integration (5.71) in two ranges:

$$\sigma^2_{white}(t_0=t_1+T)=\frac{1}{2}e^2_{ni\,white}\left(\frac{A}{\tau_i}\right)^2\left(\int_{-\infty}^{t_1}\left(e^{-\frac{(t_1-t_i)}{\tau}}-e^{-\frac{(t_1+T-t_i)}{\tau}}\right)^2dt_i+\int_{t_1}^{t_1+T}\left(1-e^{-\frac{(t_1+T-t_i)}{\tau}}\right)^2dt_i\right)=$$

$$=\frac{1}{2}e^2_{ni\,white}\left(\frac{A}{\tau_i}\right)^2\left(\frac{\tau}{2}\left(1+e^{-\frac{2T}{\tau}}-2e^{-\frac{T}{\tau}}\right)+\left(T+\frac{\tau}{2}-2\tau-\frac{\tau}{2}e^{-\frac{2T}{\tau}}+2\tau e^{-\frac{T}{\tau}}\right)\right)= \qquad (5.72)$$

$$=\frac{1}{2}e^2_{ni\,white}\left(\frac{A}{\tau_i}\right)^2\left(T-\tau\left(1-e^{-\frac{T}{\tau}}\right)\right)\simeq\Big|_{T\gg\tau}\frac{1}{2}e^2_{ni\,white}\left(\frac{A}{\tau_i}\right)^2T$$

The relative error of this simplification when we assume $T>>\tau$, is $\frac{\tau}{T}\left(e^{-\frac{2T}{\tau}}-2e^{-\frac{T}{\tau}}\right)$ and for the worst case ($\tau=\tau_S=4\ ns$) is of the order of 10^{-4}.Figure 5-13 shows the normalized noise variance at the output of the integrator as a function of the time constant τ, if we consider the white noise $e^2_{ni\,white}$ independent of τ. It is clear that approximation is accurate for τ<5 ns.

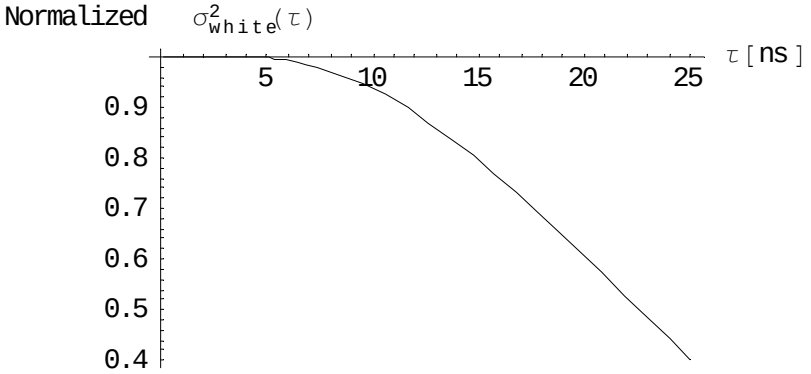

Figure 5-13. Normalized noise variance at the output of the integrator as a function of τ.

Taking into account the different noise sources (5.72) can be particularized,

$$\sigma^2_{white}(t_0=t_1+T)\simeq\Big|_{T\gg\tau}\left(\frac{1}{2}\frac{g_mR_C}{(1+g_mR_E)}\frac{1}{\tau_i}\right)^2e^2_{ni_{white}}T=\left(\frac{g_mR_C}{(1+g_mR_E)}\frac{1}{\tau_i}\right)^2\left(e^2_{n_{white}}+|R_S|^2\,i^2_{n_{white}}+e^2_{R_S}\right)T \quad (5.73)$$

Taking the values for the circuit and considering only white noise we compute the noise power at the measurement time $t_0=t_1+T$ and at 300K,

$$\sigma^2_{white}(t_0=t_1+T)\simeq\Big|_{T\gg\tau}\left(4.5\frac{1}{1.5\ ns}\right)^2\left(45\cdot10^{-18}\frac{V^2}{Hz}\right)22\ ns=5.4\cdot10^{-6}\ V^2 \quad (5.74)$$

We use $T=22\ ns$ because the integrator output is sampled 2 nanoseconds after the clock edge to avoid problems induced by clock jitter and about 1 nanosecond is needed for the commutation of the CMOS switch. The noise voltage at the output of the integrator, or in other words, the standard deviation of the voltage at the output of the integrator,

$$\sigma_{white}\left(t_0 = t_i + T\right) = 2.31\,mV\ r.m.s. \qquad (5.75)$$

Figure 5-13 may suggest that increasing time constant τ_S by increasing the source resistance R_S would reduce the noise. However we considered that $e^2_{ni\,white}$ is independent of τ_S and then of τ, and it is not completely true because the thermal noise of R_S would increase if we increase R_S. As we can appreciate in Figure 5-14 the variance at the output of the integrator (considering thermal noise on R_S as the only noise source) increases linearly with R_S for small values of R_S and hence of τ, whereas for higher values of τ the effect of increasing the thermal noise it is partially compensated with the change of the shape of the weighting function. Of course, we could try to increase τ_S increasing the parasitic capacitance (C_S) at the input, this would reduce the noise because we would reduce the bandwidth of the system. However, this is an impractical solution because the signal would get widened, and we would loss effective signal in the period T (see section 4.2).

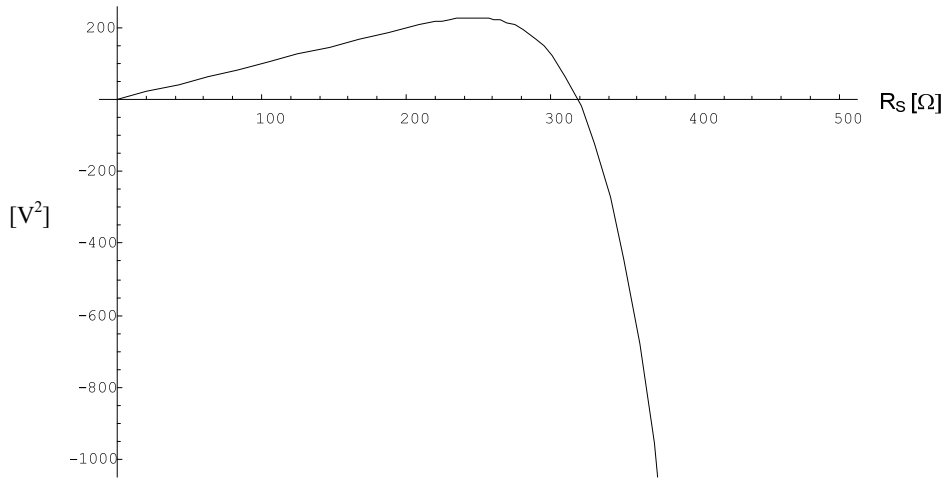

Figure 5-14. Noise variance at the output of the integrator related only to R_S thermal noise, as a function of the time constant R_S. A typical parasitic capacitance C_S of 10 pF is assumed.

5.1.3.2 Frequency domain analysis

According to expression (2.65) it is possible to compute the variance of a time-variant shaper using the Fourier transform of the weighting function ($W\left(\omega,t_0\right) = F\left\{w\left(t_i,t_0\right)\right\}$)

$$\sigma^2\left(t_0\right) = \int_0^{+\infty} e_{ni}^2\left(f\right)\left|W\left(f,t_0\right)\right|^2 df = \Big|_{\omega=2\pi f} \frac{1}{2\pi}\int_0^{+\infty} e_{ni}^2\left(\omega\right)\left|W\left(\omega,t_0\right)\right|^2 d\omega \qquad (5.76)$$

One way to determine $W(\omega,t_o)$ is to transform $w(t_i,t_o)$ by parts as in [115] using expressions (5.68) and (5.69),

$$W\left(\omega,t_0\right) = \frac{A}{\tau_i}\overbrace{\int_{-\infty}^{t_1} e^{-\frac{t_1-t_i}{\tau}} e^{-j\omega t_i} dt_i}^{\alpha} - \frac{A}{\tau_i}\overbrace{\int_{-\infty}^{t_1} e^{-\frac{t_1+T-t_i}{\tau}} e^{-j\omega t_i} dt_i}^{\beta} + \frac{A}{\tau_i}\overbrace{\int_{t_1}^{t_1+T} e^{-j\omega t_i} dt_i}^{\chi} - \frac{A}{\tau_i}\overbrace{\int_{t_1}^{t_1+T} e^{-\frac{t_1+T-t_i}{\tau}} e^{-j\omega t_i} dt_i}^{\delta} \qquad (5.77)$$

Integral α is carried out performing the variable change (v.c.) $x=t_i-t_1$,

$$\begin{aligned}\alpha &= \int_{-\infty}^{t_1} e^{-\frac{t_1-t_i}{\tau}} e^{-j\omega t_i} dt_i = \Big|_{\substack{v.c.\\ x=t_i-t_1}} \int_{-\infty}^{0} e^{-\frac{x}{\tau}} e^{-j\omega\left(x+t_1\right)} dx = e^{-j\omega t_1}\int_{-\infty}^{0} e^{\left(\frac{1}{\tau}-j\omega\right)x} dx \\ &= \frac{e^{-j\omega t_1}}{1/\tau - j\omega}\left[e^{\left(\frac{1}{\tau}-j\omega\right)x}\right]_{-\infty}^{0} = \frac{e^{-j\omega t_1}}{1/\tau - j\omega}\end{aligned} \qquad (5.78)$$

In the same way integral β is carried out performing the variable change $x=t_i-t_1-T$,

$$\beta = \int_{-\infty}^{t_1} e^{-\frac{t_1+T-t_i}{\tau}} e^{-j\omega t_i} dt_i = \Big|_{\substack{v.c. \\ x=t_i-t_1-T}} \int_{-\infty}^{-T} e^{-\frac{x}{\tau}} e^{-j\omega(x+t_1+T)} dx = e^{-j\omega(t_1+T)} \int_{-\infty}^{-T} e^{\left(\frac{1}{\tau}-j\omega\right)x} dx$$
$$= \frac{e^{-j\omega(t_1+T)}}{1/\tau - j\omega} \left[e^{\left(\frac{1}{\tau}-j\omega\right)x} \right]_{-\infty}^{-T} = \frac{e^{-j\omega(t_1+T)} e^{-\left(\frac{1}{\tau}-j\omega\right)T}}{1/\tau - j\omega} = \frac{e^{-j\omega t_1} e^{-\frac{T}{\tau}}}{1/\tau - j\omega} \tag{5.79}$$

Integral χ gives,

$$\chi = \int_{t_1}^{t_1+T} e^{-j\omega t_i} dt_i = \left[-\frac{e^{-j\omega t_i}}{j\omega} \right]_{t_1}^{t_1+T} = \frac{e^{-j\omega t_1} - e^{-j\omega(t_1+T)}}{j\omega} \tag{5.80}$$

And integral δ is carried out performing the variable change $x=t_i-t_1-T$,

$$\delta = \int_{t_1}^{t_1+T} e^{-\frac{t_1+T-t_i}{\tau}} e^{-j\omega t_i} dt_i = \Big|_{\substack{v.c. \\ x=t_i-t_1-T}} \int_{-T}^{0} e^{-\frac{x}{\tau}} e^{-j\omega(x+t_1+T)} dx = e^{-j\omega(t_1+T)} \int_{-T}^{0} e^{\left(\frac{1}{\tau}-j\omega\right)x} dx$$
$$= \frac{e^{-j\omega(t_1+T)}}{1/\tau - j\omega} \left[e^{\left(\frac{1}{\tau}-j\omega\right)x} \right]_{-T}^{0} = \frac{e^{-j\omega(t_1+T)} \left(1 - e^{-\left(\frac{1}{\tau}-j\omega\right)T} \right)}{1/\tau - j\omega} = \frac{e^{-j\omega t_1} \left(e^{-j\omega T} - e^{-\frac{T}{\tau}} \right)}{1/\tau - j\omega} \tag{5.81}$$

Then, the Fourier transform of the weighting function or time variant transfer function for the measurement time $t_0=t_1+T$ is

$$W(\omega, t_0 = t_1 + T) = \frac{A}{\tau_i} \frac{e^{-j\omega t_1}}{1/\tau - j\omega} \left[1 - e^{-\frac{T}{\tau}} + \frac{j\omega}{1/\tau - j\omega} - \frac{j\omega}{1/\tau - j\omega} e^{-j\omega T} - e^{-j\omega T} + e^{-\frac{T}{\tau}} \right] =$$
$$= \frac{A}{\tau_i} \left(\frac{1/\tau}{1/\tau - j\omega} \right) \left(\frac{1 - e^{-j\omega T}}{j\omega} \right) e^{-j\omega t_1} \tag{5.82}$$

It is also possible to compute the Fourier transform of the weighting function using expression (5.70),

$$W(\omega, t_0) = F\{w(t_i, t_0)\} = F\left\{ \frac{1}{\tau_i} \int_{-\infty}^{+\infty} p(t - t_i) g(t) dt \right\} \tag{5.83}$$

We will use a procedure analogous to the one of the convolution theorem of the Fourier transform, using a variable change $t_i=t+x$,

$$W(\omega, t_0 = t_1 + T) = F\left\{ \frac{1}{\tau_i} \int_{-\infty}^{+\infty} p(t - t_i) g(t) dt \right\} = \frac{1}{\tau_i} \int_{-\infty}^{+\infty} \left(\int_{-\infty}^{+\infty} p(t - t_i) g(t) dt \right) e^{-j\omega t_i} dt_i =$$
$$= \Big|_{\substack{v.c. \\ t_i=x+t}} \frac{1}{\tau_i} \int_{-\infty}^{+\infty} \left(\int_{-\infty}^{+\infty} p(-x) g(t) dt \right) e^{-j\omega(x+t)} dx = \frac{1}{\tau_i} \int_{-\infty}^{+\infty} g(t) e^{-j\omega t} dt \int_{-\infty}^{+\infty} p(-x) e^{-j\omega x} dx = \tag{5.84}$$
$$= \frac{1}{\tau_i} F\{g(t)\} F\{p(-x)\}$$

This means that the Fourier transform of a gated integrator can be computed as the product of the Fourier transform of the gate function and the mirror of the prefilter impulse response (times the integrator time constant $1/\tau_i$).

For the gate function,

$$F\{g(t)\} = F\{u(t - t_1) - u(t - t_1 - T)\} = e^{-j\omega t_1} \left(\frac{1 - e^{-j\omega T}}{j\omega} \right) \tag{5.85}$$

For the mirror of the impulse response of the prefilter[v],

$$F\{p(-t)\} = F\left\{A\frac{1}{\tau}e^{\frac{t}{\tau}}u(t)\right\} = A\left(\frac{1/\tau}{1/\tau - j\omega}\right) \qquad (5.86)$$

Therefore, combining (5.84), (5.85) and (5.86) we obtain the same result as in the computation of the Fourier transform of the weighting function integrating by parts (5.82). Furthermore, expression (5.84) is valid for any prefilter, thus we obtain a general expression to compute the noise PSD and variance at the output of a gated integrator, the PSD of the noise at the output as a function of the PSD of the noise at the input e^2_{no} (prefilter output) is,

$$G_{yy}(\omega) = G_{xx}(\omega)\left|W(\omega,t_0)\right|^2 d\omega = e^2_{ni}(\omega)\left(\frac{1}{\tau_i}\right)^2 \left|F\{p(-t)\}\right|^2 \left|F\{g(t)\}\right|^2 = e^2_{no}(\omega)\left(\frac{1}{\tau_i}\right)^2 \left|F\{g(t)\}\right|^2 =$$

$$= e^2_{no}(\omega)\left(\frac{1}{\tau_i}\right)^2 \left|e^{-j\omega t_1}\left(\frac{1-e^{-j\omega T}}{j\omega}\right)\right|^2 = e^2_{no}(\omega)\left(\frac{1}{\tau_i}\right)^2 \frac{2(1-\cos(\omega T))}{\omega^2} = e^2_{no}(\omega)\left(\frac{1}{\tau_i}\right)^2 \frac{4\left(sen\left(\frac{\omega T}{2}\right)\right)^2}{\omega^2}$$

(5.87)

Expression (5.87) is important, because as pointed out in [114] it provides a way to compute the PSD of the noise of a system which includes a gated integrator using conventional electrical simulators. Therefore $\frac{1}{\tau_i}F\{g(t)\}$ (expression (5.85)) can be understood like a "transfer function" of the gated integrator. Its square modulus $\left|\frac{1}{\tau_i}F\{g(t)\}\right|^2$ is drawn on Figure 5-15. The response is almost flat for $\omega << 1/T$.

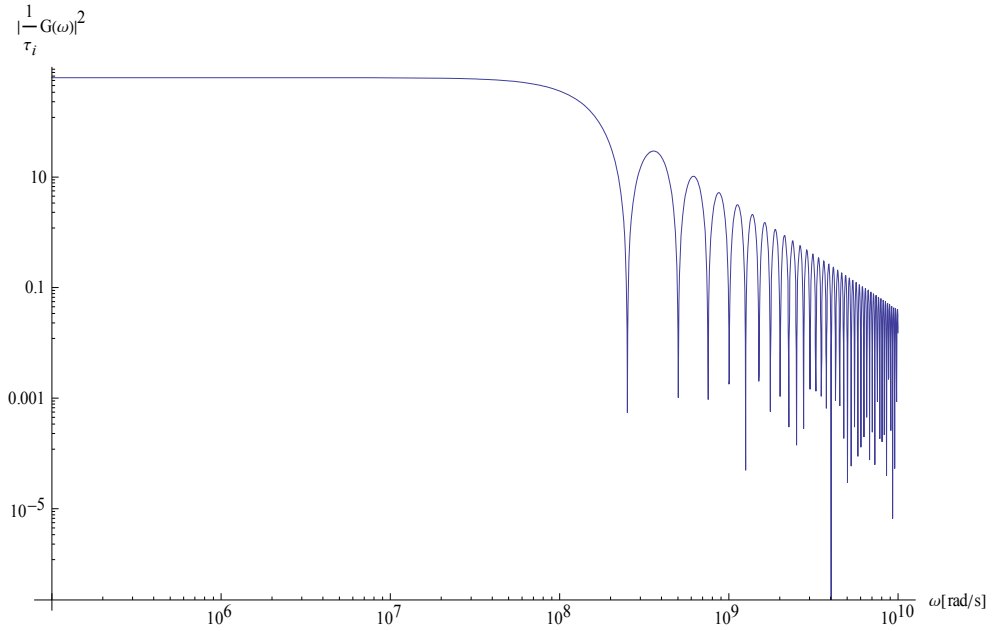

Figure 5-15. Square modulus of the Fourier transform of *g(t)*.

An alternative way to derive $F\{g(t)\}$ is using the definition of a system that integrates during a time T,

[v]The convolution operation ⊗ already involves the mirror function of *p(t)*, thus $F\{p(t) \otimes g(t)\} \neq F\{p(t)\}F\{g(t)\}$

$$y(t)=\int_{t-t_1-T}^{t-t_1} x(u)du \tag{5.88}$$

Taking the derivative,

$$y'(t)=\left[x(t-t_1)-x(t-t_1-T)\right] \tag{5.89}$$

Using Fourier transform,

$$j\omega F\{y(t)\}=\left[F\{x(t)\}e^{-j\omega t_1}-F\{x(t)\}e^{-j\omega t_1}e^{-j\omega T}\right] \tag{5.90}$$

Then by definition of transfer function,

$$F\{g(t)\}=\frac{F\{y(t)\}}{F\{x(t)\}}=e^{-j\omega t_1}\left(\frac{1-e^{-j\omega T}}{j\omega}\right) \tag{5.91}$$

To compute the noise variance we need the square modulus of the noise weighting function,

$$\left|W(\omega,t_0)\right|^2=\left|\frac{A}{\tau_i}\left(\frac{1/\tau}{1/\tau-j\omega}\right)\left(\frac{1-e^{-j\omega T}}{j\omega}\right)e^{-j\omega t_1}\right|^2=\left(\frac{A}{\tau_i}\right)^2\left(\frac{(1/\tau)^2}{(1/\tau)^2+\omega^2}\right)\frac{2(1-\cos(\omega T))}{\omega^2}=$$

$$=\left(\frac{A}{\tau_i}\right)^2\left(\frac{(1/\tau)^2}{(1/\tau)^2+\omega^2}\right)\frac{4\left(sen\left(\frac{\omega T}{2}\right)\right)^2}{\omega^2} \tag{5.92}$$

In Figure 5-16 the square modulus of the Fourier transform of the weighting function for different time constant τ is shown. There is no remarkable inside preamplifier bandwidth effect for τ≤5 ns.

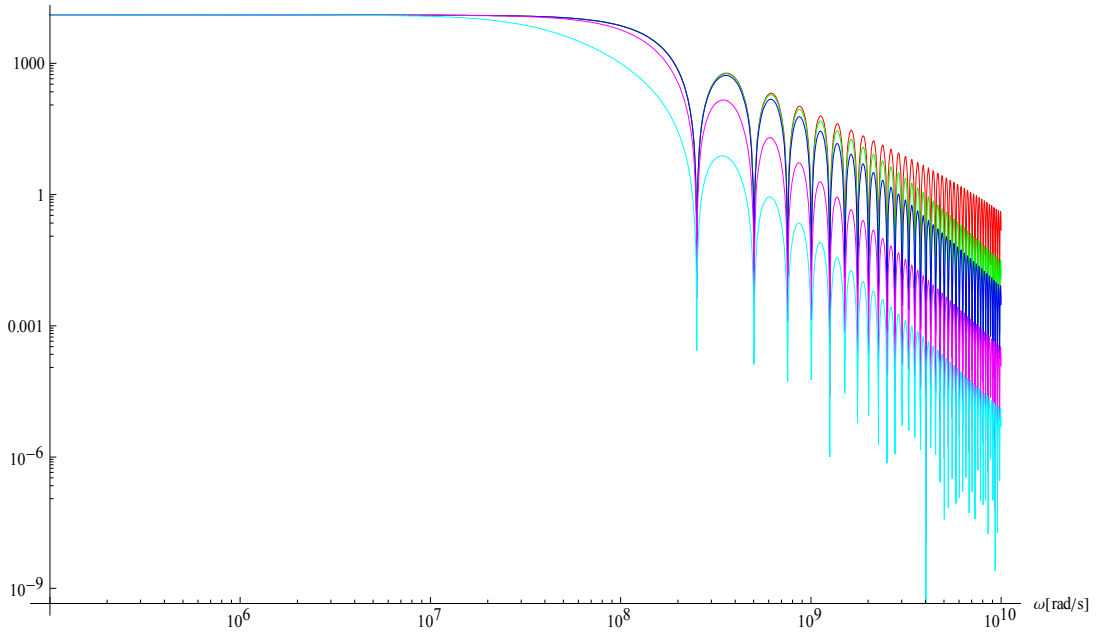

Figure 5-16. Magnitude of the Fourier transform of the weighting function for different values of prefilter time constant τ. Cyan τ=25 ns, magenta τ=5ns, blue τ=1ns, green τ=0.5 ns and red τ=0.1 ns.

In order to compute the integral we rewrite expression (5.92),

$$\left|W(\omega,t_0)\right|^2=\left(\frac{A}{\tau_i}\right)^2\left(1-\frac{\omega^2}{(1/\tau)^2+\omega^2}\right)\frac{2(1-\cos(\omega T))}{\omega^2}=2\left(\frac{A}{\tau_i}\right)^2\left(\frac{(1-\cos(\omega T))}{\omega^2}-\frac{(1-\cos(\omega T))}{(1/\tau)^2+\omega^2}\right) \tag{5.93}$$

We will compute the noise variance for the white noise component of e^2_{ni},

$$\sigma^2_{white}(t_0)=\frac{1}{2\pi}e^2_{ni\_white}\int_0^{+\infty}\left|W(\omega,t_0)\right|^2 d\omega=\frac{1}{\pi}\left(\frac{A}{\tau_i}\right)^2 e^2_{ni\_white}\int_0^{+\infty}\left(\frac{(1-\cos(\omega T))}{\omega^2}-\frac{(1-\cos(\omega T))}{\left(1/\tau\right)^2+\omega^2}\right)d\omega \tag{5.94}$$

The solution for the different terms of the definite integral can be found in [174] (integral tables 2).

$$\sigma^2_{white}(t_0)=\frac{1}{\pi}\left(\frac{A}{\tau_i}\right)^2 e^2_{ni\_white}\frac{\pi}{2}\left(T-\tau\left(1-e^{-\frac{T}{\tau}}\right)\right)\simeq\Big|_{T\gg\tau}\frac{1}{2}\left(\frac{A}{\tau_i}\right)^2 e^2_{ni\_white}T \tag{5.95}$$

We obtain, thus, the same result as we obtained using time domain analysis (5.72).

The Flicker component of the PSD of the total input equivalent noise is, as shown in section 5.1.2,

$$e^2_{ni\_Flicker}(f)\simeq 2\left(R_E+r_b+R_S\right)^2 i^2_{si_b\_Flicker}=\frac{C_F}{f} \tag{5.96}$$

Where C_F is about $16\cdot10^{-13}\ V^2$, taking into account the correlation of Flicker noise sources in e_n and in. It is more convenient to write the expression as a function of $\omega=2\pi f$,

$$e^2_{ni\_Flicker}(\omega)\simeq 2\pi\frac{C_F}{\omega} \tag{5.97}$$

The Flicker noise is relevant at low frequency ($\omega<2\pi f_{Ceni}<<1/\tau_C$). As the system bandwidth (preamplifier) $1/\tau_C$ is much higher than the Flicker noise corner frequency, the preamplifier has a flat response for the range of interest. The noise variance related to the Flicker noise is,

$$\sigma^2_{Flicker}(t_0)=\frac{1}{2\pi}\int_0^{1/\tau_{Ceni}} e^2_{ni\_Flicker}(\omega)\left|W(\omega,t_0)\right|^2 d\omega=\left(\frac{A}{\tau_i}\right)^2\int_0^{1/\tau_{Ceni}}\frac{C_F}{\omega}\frac{4\left(sen\left(\frac{\omega T}{2}\right)\right)^2}{\omega^2}d\omega \tag{5.98}$$

Figure 5-17 shows the PSD of the Flicker noise at the output of the integrator, corresponding to expression (5.98).

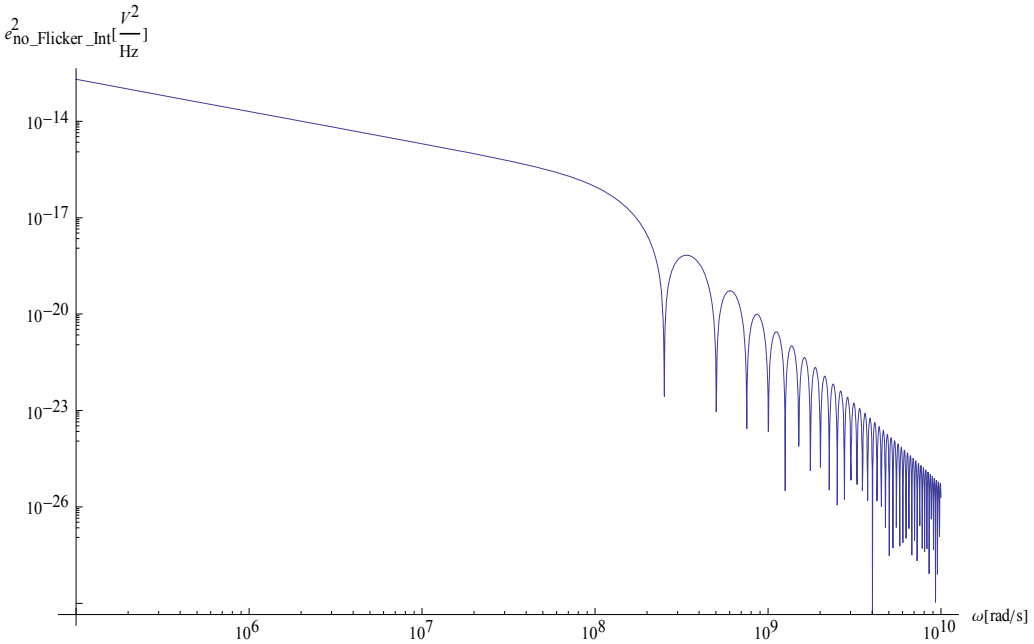

Figure 5-17. PSD of the noise Flicker noise at the output of the integrator.

Where $\tau_{Ceni}=1/2\pi f_{Ceni}$. As $2\pi f_{Ceni}<<1/T$, then $\omega T<<1$ for the range of interest, we will use following simplification: $sen(x)\simeq|_{x\ll 1} x$. This means that for low frequency the PSD of the Flicker noise at the output of the integrator can be approximated by a $1/\omega$ characteristics, as shown in Figure 5-18. The approximation is good for $f<3MHz$ (or ω<20 Mrad/s), i.e. it is valid for frequencies about 100 times higher than the corner frequency f_{Ceni}.

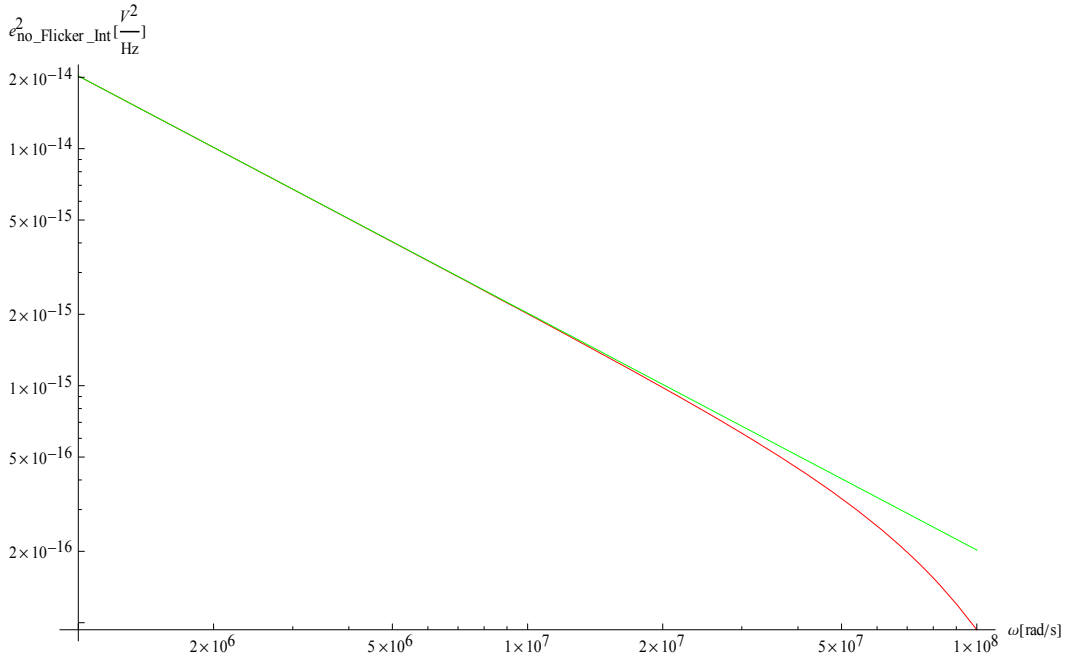

Figure 5-18. PSD of the Flicker noise at the output of the integrator (expression (5.98)) versus ideal 1/ω slope (expression (5.99).

Then,

$$\sigma^2_{Flicker}(t_0)\simeq|_{\omega\ll 1/T} C_F\left(A\frac{T}{\tau_i}\right)^2\int_0^{1/\tau_{Ceni}}\frac{1}{\omega}d\omega \qquad (5.99)$$

A PSD inverse to the frequency seems suggest "infinite" noise at DC. This is not the case because the "zero" frequency does not exist: any electronic circuit or equipment is turned on (and off) at some moment. Therefore, the minimum frequency is $1/T_{OP}$ where T_{OP} is the time the circuit is kept powered on.

$$\sigma^2_{Flicker}(t_0)\simeq|_{\omega\ll 1/T} C_F\left(A\frac{T}{\tau_i}\right)^2\int_{1/T_{OP}}^{1/\tau_{Ceni}}\frac{1}{\omega}d\omega = C_F\left(A\frac{T}{\tau_i}\right)^2\ln\left(\frac{T_{OP}}{\tau_{Ceni}}\right) \qquad (5.100)$$

For a T_{OP} of 1 day we have $\sigma^2_{Flicker}(t_0)\simeq|_{T_{OP}=1\ day} 1.66\cdot10^{-7}\ V^2$ and for 1 year $\sigma^2_{Flicker}(t_0)\simeq|_{T_{OP}=1\ year} 2.06\cdot10^{-7}\ V^2$. In any case the white noise term dominates ($\sigma^2_{white}(t_0)\simeq 6.7\cdot10^{-6}\ V^2$) and the contribution of the Flicker noise is <1% of the total output noise voltage (r.m.s.). Comparing (5.100) and (5.95) we see that the power of the white noise increases proportionally to the integration time T whereas the power of the Flicker noise increases as T^2. This means that if the integration time is large enough Flicker noise will become dominant. We define a corner integration time when both noise components are equal, for a temperature of 300K and after 1 hour of operation, it is

$$T_C=\frac{e^2_{ni\_white}}{2C_F\ln\left(\frac{T_{OP}}{\tau_{Ceni}}\right)}\simeq 1\,\mu s \qquad (5.101)$$

5.2 Offset

For differential circuits, the effect of device mismatches on DC performance is conveniently represented by two quantities, the input offset voltage (V_{0S}) and the input offset current (I_{0S}) [66]. These quantities represent the input-referred effect of all the component mismatches within the amplifier on its DC performance [132]. The DC behavior of the amplifier containing mismatches is identical to an ideal amplifier with no mismatches but with the input offset voltage source added in series with the input and the input offset current source in shunt across the input terminals. Figure 5-19 shows the input offset voltage and currents for a differential circuit, like the preamplifier or the input stage of the integrator. I_p and I_n current sources describe bias or leakage currents for each input terminal and therefore they can flow in or out of the preamplifier input. Difference of I_p and I_n is the input offset current (I_{0S})

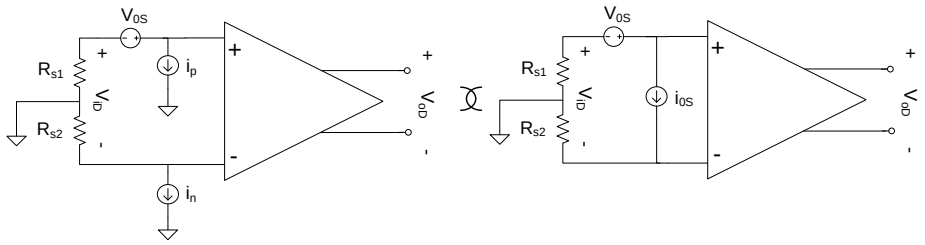

Figure 5-19. Input offset voltage and currents for a differential circuit.

First we will determine the value of the offset voltage and noise sources for the two front end circuits: the preamplifier and the input stage of the integrator. Those blocks will determine the offset of the channel, as the gain is concentrated on the front end. After that we will combine the effect of the noise sources to determine the offset at the output of the integrator in the reset state and in the integration state.

5.2.1 Offset of the preamplifier

The offset of the preamplifier (Figure 4-3) is mainly determined by the offset of the emitter-coupled differential pair. DC gain of this stage is high enough to neglect the effect of the emitter follower at the outputs (see simulation results at the end of the section).

The predominant sources of offset error in the emitter-coupled pair are the mismatches in the base width, base doping level, and collector doping level of the transistors, mismatches in the effective emitter area of the transistors, and mismatches in the collector load resistors and in the emitter degeneration resistors [66]. For the purpose of predicting the offset voltage from device parameters that are directly measurable, we will express the offset in terms of mismatch in saturation current of the transistors (I_S) instead of structural parameters such as the area or doping levels of the transistor.

The input offset voltage of the preamplifier (V_{0SP}) can be defined as the negative of the DM input voltage (V_{0SP}') that must be applied to drive the differential output voltage of a mismatched amplifier to zero $V_{oD}=0$. By definition, V_{0SP}' cancels out the effect of the mismatch. Thus, using superposition theorem we can state that the amplifier with mismatch has the same behavior as an ideal amplifier with a voltage source in series $V_{0SP}=- V_{0SP}'$.

With the condition $V_{oD}=0$,

$$I_{C1}R_{C1} = I_{C2}R_{C2} \qquad (5.102)$$

The input offset voltage is computed with an ideal voltage source ($R_{S1}=R_{S2}=0$). Applying KVL,

$$V_{0SP}^{'} + V_{BE2} + I_{E2}R_{E2} = V_{BE1} + I_{E1}R_{E1} \qquad (5.103)$$

Combining both expressions and as $V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right)$ and $\frac{I_C}{\alpha_F} = I_E$,

$$V'_{0SP} = V_T \ln\left(\frac{R_{C2}}{R_{C1}}\frac{I_{S2}}{I_{S1}}\right) + \frac{I_{C1}}{\alpha_{F1}}R_{E1} - \frac{I_{C2}}{\alpha_{F2}}R_{E2} \qquad (5.104)$$

Defining the mismatch term of the variables of the previous equation as $\Delta R_C = R_{C1} - R_{C2}$, $\Delta R_E = R_{E1} - R_{E2}$, $\Delta I_C = I_{C1} - I_{C2}$, $\Delta I_S = I_{S1} - I_{S2}$ and $\Delta\alpha_F = \alpha_{F1} - \alpha_{F2}$, then

$$V_{0SP} = -V'_{0SP} = -V_T \ln\left(\left(\frac{R_C - \frac{\Delta R_C}{2}}{R_C + \frac{\Delta R_C}{2}}\right)\left(\frac{I_S - \frac{\Delta I_S}{2}}{I_S + \frac{\Delta I_S}{2}}\right)\right) + \frac{\left(I_C + \frac{\Delta I_C}{2}\right)\left(R_E + \frac{\Delta R_E}{2}\right)}{\left(\alpha_F + \frac{\Delta\alpha_F}{2}\right)} - \frac{\left(I_C - \frac{\Delta I_C}{2}\right)\left(R_E - \frac{\Delta R_E}{2}\right)}{\left(\alpha_F - \frac{\Delta\alpha_F}{2}\right)} \qquad (5.105)$$

With the assumption that $\Delta I_C << I_C$, $\Delta I_S << I_S$, $\Delta R_C << R_C$, $\Delta R_E << R_E$ and $\Delta\alpha_F << \alpha_F$, (5.105) can be simplified[w]

$$V_{0SP} \simeq -V_T \ln\left(\left(1 - \frac{\Delta R_C}{R_C}\right)\left(1 - \frac{\Delta I_S}{I_S}\right)\right) + \frac{I_C R_E}{\alpha_F}\frac{\left(\left(1 - \frac{\Delta\alpha_F}{2\alpha_F}\right)\left(1 + \frac{\Delta I_C}{2I_C}\right)\left(1 + \frac{\Delta R_E}{2R_E}\right)\right) - \left(\left(1 + \frac{\Delta\alpha_F}{2\alpha_F}\right)\left(1 - \frac{\Delta I_C}{2I_C}\right)\left(1 - \frac{\Delta R_E}{2R_E}\right)\right)}{1 - \left(\frac{\Delta\alpha_F}{2\alpha_F}\right)^2} \simeq$$

$$\simeq_{\left(\frac{\Delta\alpha_F}{2}\right)^2 \ll 1} -V_T \ln\left(\left(1 - \frac{\Delta R_C}{R_C}\right)\left(1 - \frac{\Delta I_S}{I_S}\right)\right) + \frac{I_C R_E}{\alpha_F}\left(\frac{\Delta I_C}{I_C} + \frac{\Delta R_E}{R_E} - \frac{\Delta\alpha_F}{\alpha_F}\right) \qquad (5.106)$$

If $x << 1$, a Taylor series can be used to show that

$$\ln(1+x) = x - \frac{x^2}{2} + \frac{x^3}{3} - \ldots \qquad (5.107)$$

Applying (5.107) in the logarithm of (5.106) and ignoring terms higher than first order in the expansion gives

$$V_{0SP} \simeq -V_T\left(-\frac{\Delta R_C}{R_C} - \frac{\Delta I_S}{I_S}\right) + \frac{I_C R_E}{\alpha_F}\left(\frac{\Delta I_C}{I_C} + \frac{\Delta R_E}{R_E} - \frac{\Delta\alpha_F}{\alpha_F}\right) \qquad (5.108)$$

---

[w] For terms of the form $\frac{x - \frac{\Delta x}{2}}{x + \frac{\Delta x}{2}} = \frac{\left(x - \frac{\Delta x}{2}\right)^2}{x^2 - \left(\frac{\Delta x}{2}\right)^2} = \frac{\left(1 - \frac{\Delta x}{2x}\right)^2}{1 - \left(\frac{\Delta x}{2x}\right)^2} = \frac{1 - \frac{\Delta x}{x} + \left(\frac{\Delta x}{2x}\right)^2}{1 - \left(\frac{\Delta x}{2x}\right)^2} \simeq_{\left(\frac{\Delta x}{2x}\right)^2 \ll \frac{\Delta x}{x}} 1 - \frac{\Delta x}{x}$ and of the form :

$$\frac{\left(x + \frac{\Delta x}{2}\right)\left(y + \frac{\Delta y}{2}\right)}{\left(z + \frac{\Delta z}{2}\right)} = \frac{xy}{z}\frac{\left(1 + \frac{\Delta x}{2x}\right)\left(1 + \frac{\Delta y}{2y}\right)}{\left(1 + \frac{\Delta z}{2z}\right)} = \frac{xy}{z}\frac{1 + \frac{\Delta x}{2x} + \frac{\Delta y}{2y} + \frac{\Delta y \Delta x}{4yx}}{1 + \frac{\Delta z}{2z}} \simeq_{\frac{\Delta y \Delta x}{4yx} \ll \frac{\Delta x}{2x}, \frac{\Delta y}{2y}} \frac{xy}{z}\frac{1 + \frac{\Delta x}{2x} + \frac{\Delta y}{2y}}{1 + \frac{\Delta z}{2z}}$$

With the condition (5.102) it can be readily shown that $\frac{\Delta I_C}{I_C} = -\frac{\Delta R_C}{R_C}$ and using $I_C = g_m V_T$,

$$V_{0SP} \simeq V_T \left(\frac{\Delta R_C}{R_C} \left(1 + \frac{g_m R_E}{\alpha_F} \right) + \frac{\Delta I_S}{I_S} - \frac{g_m R_E}{\alpha_F} \left(\frac{\Delta R_E}{R_E} - \frac{\Delta \alpha_F}{\alpha_F} \right) \right) \quad (5.109)$$

Comparing (5.109) with the expression for the input offset voltage without emitter degeneration $V_{0SP} \simeq V_T \left(\frac{\Delta R_C}{R_C} + \frac{\Delta I_S}{I_S} \right)$ (see [66]) we can conclude that emitter degeneration does not help to improve the offset, even if relative tolerances of the terms corresponding to mismatch of R_C an R_E in (5.109) are equal and cancel out. Therefore, emitter degeneration does not improve offset in differential emitter coupled pairs, by contrast in current mirrors it improves matching between currents.

Mismatch factors ($\Delta x/x$) in (5.109) are actually random parameters that take on a different value on each circuit fabricated, and the distribution of the observed values is described by a probability distribution. For large samples the distribution tends to a normal, or Gaussian, distribution with zero mean. Knowing the value of the mismatch in the components, expression (5.109) gives the offset for one sample of a design.

On differential circuits, asymmetries in the circuit topology or on the layout origin a non-zero value of the mean of the distribution of the mismatch of the values of the components. As can be observed on Figure 4-3 the scheme of the preamplifier is fully symmetrical. Nevertheless, looking at the layout (Figure 4-20) we can see that the metal path connecting the elementary resistors that compose R_{E1} is about 48μm longer than the one that connect the elementary resistors that compose R_{E2}. As the width of the line is 3μm and the resistivity of this metal layer is 50 mΩ/□, there is a systematic difference between R_{E1} and R_{E2} of ΔR_E=1.12 Ω. The same happens with the collector resistor, however on that case $R_{C1}<R_{C2}$ of ΔR_c=-1.21 Ω. The applying those systematic mismatches to expression (5.109), we obtain the average value of the input offset voltage, $\mu_{V_{0SP}} \simeq -0.75\,mV$.

A parameter of more interest to the circuit designer than the offset of one sample is the standard deviation of the total offset voltage. Since the offset is the sum of uncorrelated random parameters, the standard deviation of the sum is equal to the square root of the sum of the squares of the standard deviation of the mismatch contributors, or

$$\sigma_{V_{0SP}} \simeq V_T \sqrt{\left(\frac{\sigma_{\Delta R_C}}{R_C} \right)^2 \left(1 + \frac{g_m R_E}{\alpha_F} \right)^2 + \left(\frac{\sigma_{\Delta I_S}}{I_S} \right)^2 + \left(\frac{\sigma_{\Delta R_E}}{R_E} \right)^2 \left(\frac{g_m R_E}{\alpha_F} \right)^2 + \left(\frac{\sigma_{\Delta \alpha_F}}{\alpha_F} \right)^2 \left(\frac{g_m R_E}{\alpha_F} \right)^2} \quad (5.110)$$

As discussed in section 4.2.1.4, the typical resistor standard deviation $\sigma_{\Delta R_E/R}$ of 0.25 % and $\sigma_{\Delta R_C/R}$ of 0.22 % can be computed directly from [73]. According to [73] and [162] for an emitter area of 3 units and a multiplier parameter of 4 the standard deviation of the mismatch of the saturation current is $\frac{\sigma_{\Delta I_S}}{I_S} = 0.7\,\%$. As $\alpha_F = \frac{\beta_F}{1+\beta_F}$, using theory of error propagation $\sigma_{\Delta \alpha_F} = \left| \left(\frac{\partial \alpha_F(\beta_F)}{\partial \beta_F} \right) \right| \sigma_{\Delta \beta_F} = \frac{1}{(1+\beta_F)^2} \sigma_{\Delta \beta_F}$, then $\frac{\sigma_{\Delta \alpha_F}}{\alpha_F} = \frac{1}{1+\beta_F} \frac{\sigma_{\Delta \beta_F}}{\beta_F}$. As $\beta_F \approx 100$ and $\frac{\sigma_{\Delta \beta_F}}{\beta_F} \simeq 2\,\%$, $\alpha_F \approx 0.99$ and $\frac{\sigma_{\Delta \alpha_F}}{\alpha_F} \simeq 0.02\,\%$. With g_m=*0.02 S*, R_E=*460* Ω, R_C=*2k4* Ω and V_T=*26 m*V at 300K, the standard deviation of the input offset voltage of the preamplifier V_{0SP} is $\sigma_{V_{0SP}} \simeq 0.8$ mV *r.m.s.*

The input offset current I_{0SP} is measured with the inputs connected only to current sources and is the negative difference in the base currents that must be applied to drive the DM output voltage to

zero. Since the base current of each transistor is equal to the corresponding collector current divided by beta, the offset current is

$$I_{0SP} = -\left(\frac{I_{C1}}{\beta_{F1}} - \frac{I_{C2}}{\beta_{F2}} \right) \tag{5.111}$$

when V_{oD}=0. As before, we can write terms in (5.111) as a function of their mismatch,

$$I_{0SP} = -\left(\frac{I_C + \frac{\Delta I_C}{2}}{\beta_F + \frac{\Delta \beta_F}{2}} - \frac{I_C - \frac{\Delta I_C}{2}}{\beta_F - \frac{\Delta \beta_F}{2}} \right) \tag{5.112}$$

and neglecting higher-order terms, this becomes

$$I_{0SP} = -\frac{I_C}{\beta_F}\left(\frac{\Delta I_C}{I_C} - \frac{\Delta \beta_F}{\beta_F} \right) \tag{5.113}$$

with the condition (5.102) for V_{oD} to be zero, $I_{C1}R_{C1} = I_{C2}R_{C2}$ and then $\frac{\Delta I_C}{I_C} = -\frac{\Delta R_C}{R_C}$, so

$$I_{0SP} = \frac{I_C}{\beta_F}\left(\frac{\Delta R_C}{R_C} + \frac{\Delta \beta_F}{\beta_F} \right) \tag{5.114}$$

and the standard deviation of the input offset current I_{0SP} is

$$\sigma_{I_{0SP}} = \frac{I_C}{\beta_F}\sqrt{\left(\frac{\sigma_{\Delta R_C}}{R_C} \right)^2 + \left(\frac{\sigma_{\Delta \beta_F}}{\beta_F} \right)^2} \tag{5.115}$$

the mismatch in β_F dominates, and the approximated value is $\sigma_{I_{0SP}} \simeq 100$ nA *r.m.s.*

Looking at Figure 5-19 , it is clear that both input voltage and input current offset sources can be combined to define the input zero error (IZE) of the preamplifier [79] as,

$$IZE_P = V_{0SP} + 2R_S I_{0SP} \tag{5.116}$$

and the output zero error (OZE) taking the DM gain of the preamplifier at DC $A_{DD}(0)$,

$$OZE_P = A_{DD}(0)\left(V_{0SP} + 2R_S I_{0SP} \right) \tag{5.117}$$

To compute the standard deviation of the IZE and the OZE it has to be taken into account that input voltage and input current offset sources are correlated since they do depend on the mismatch of the same device parameters, thus

$$\sigma^2_{OZE_P} = A^2_{DD}(0)\left(\sigma^2_{V_{0SP}} + \left(2R_S\right)^2 \sigma^2_{I_{0SP}} + 2\left(2R_S\right)\mathrm{cov}\left(V_{0SP}, I_{0SP}\right) \right) \tag{5.118}$$

However, according to the computed values of the standard deviation of the input voltage and input current offset sources, for source load below 5 kΩ the input offset voltage dominates. Thus,

$$\sigma_{OZE_P} \simeq \big|_{R_S \ll 5\,K\Omega}\, A_{DD}(0)\sigma_{V_{0SP}} = 3.6 \text{ mV r.m.s.} \tag{5.119}$$

being the mean OZE

$$\mu_{OZE_P} \simeq \big|_{R_S \ll 5\,K\Omega}\, A_{DD}(0)\mu_{V_{0SP}} = -3.4 \text{ mV} \tag{5.120}$$

Figure 5-20 shows statistical results of Monte Carlo simulation of the OZE of the preamplifier. The values for the mean and the standard deviation are close to the ones expected from hand calculations. The effect of the output buffer is negligible, as expected. The parasitic resistances of the preamplifier are included in the simulation using the extraction tool of the design kit, thus the effect of layout asymmetry is visible. This asymmetry was not corrected because it introduces an offset

which has a similar value and the opposite sign. On this way the range that must cover the threshold is balanced, see Figure 5-1. As said before the effect of the emitter follower is negligible.

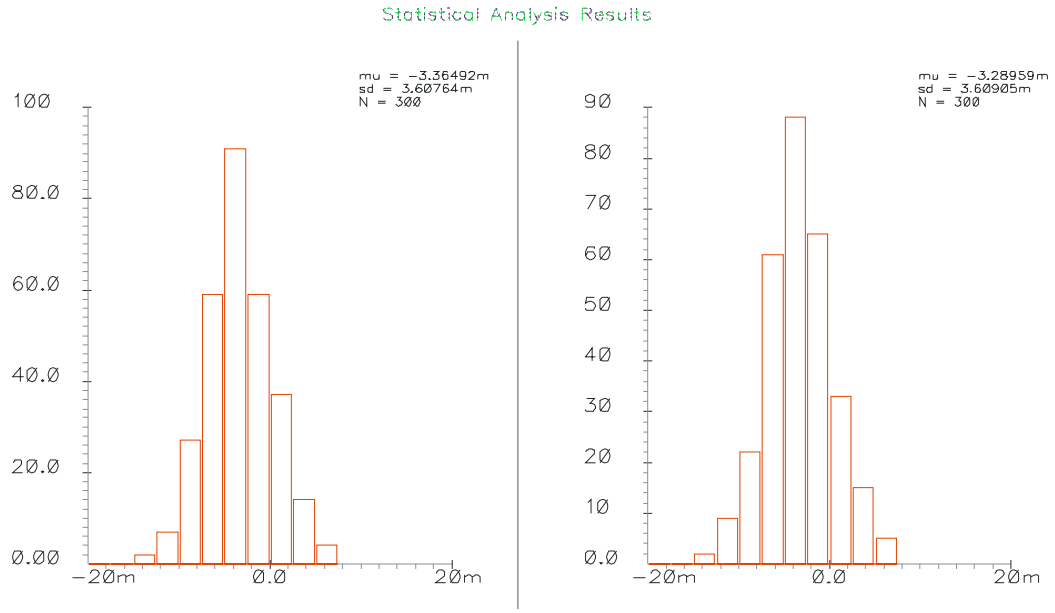

Figure 5-20. Statistical results of Monte Carlo simulation of the OZE of the preamplifier. Differential pair and output buffer (left) and only differential pair (right).

The offset drift with temperature or time is also an important parameter. In expression (5.109) both $V_T=kT/q$ and $g_m=I_C/V_T= I_C\, q/kT$ depend on the temperature, but inversely. Hence we can expect that thess terms cancel out in the temperature dependence of the offset. Even if poly resistors have a non negligible temperature coefficient we do not expect that the relative matching varies with temperature, as ΔR should have the same TC as R. Thus, differentiating (5.108) respect to the temperature

$$\frac{\partial V_{0SP}}{\partial T} \simeq -\frac{\partial V_T}{\partial T}\left(-\frac{\Delta R_C}{R_C}-\frac{\Delta I_S}{I_S}\right)+\frac{\frac{\partial I_C}{\partial T}R_E+I_C\frac{\partial R_E}{\partial T}}{\alpha_F}\left(\frac{\Delta I_C}{I_C}+\frac{\Delta R_E}{R_E}-\frac{\Delta\alpha_F}{\alpha_F}\right)=$$

$$=-\frac{k}{q}\left(-\frac{\Delta R_C}{R_C}-\frac{\Delta I_S}{I_S}\right)+\frac{I_C R_E}{\alpha_F}\left(\frac{1}{I_C}\frac{\partial I_C}{\partial T}+\frac{1}{R_E}\frac{\partial R_E}{\partial T}\right)\left(\frac{\Delta I_C}{I_C}+\frac{\Delta R_E}{R_E}-\frac{\Delta\alpha_F}{\alpha_F}\right)= \qquad (5.121)$$

$$=-\frac{k}{q}\left(-\frac{\Delta R_C}{R_C}-\frac{\Delta I_S}{I_S}\right)+\frac{I_C R_E}{\alpha_F}\left(TC_{I_C}+TC_{R_E}\right)\left(\frac{\Delta I_C}{I_C}+\frac{\Delta R_E}{R_E}-\frac{\Delta\alpha_F}{\alpha_F}\right)$$

The difference between the TC of the bias current and the TC of R_E is about -100 ppm/K as seen in section 4.5.1. Therefore, approximated values for the offset voltage drift with temperature are for the mean,

$$\frac{\partial \mu_{V_{0SP}}}{\partial T} \simeq \frac{k}{q}\left(\frac{\Delta R_C}{R_C}\right)+\frac{I_C R_E}{\alpha_F}\left(TC_{I_C}+TC_{R_E}\right)\left(\frac{\Delta R_E}{R_E}\right)\simeq -0.5\,\frac{\mu V}{K} \qquad (5.122)$$

For the standard deviation, as $\frac{k}{q} >> \left(TC_{I_C}+TC_{R_E}\right)$ and the relative mismatch of the saturation current is the highest one,

$$\frac{\partial \sigma_{V_{0SP}}}{\partial T} \simeq \frac{k}{q}\frac{\sigma_{\Delta I_S}}{I_S} \simeq 0.60\ \frac{\mu V}{K}\ \text{r.m.s.} \qquad (5.123)$$

According to Spectre simulations $\frac{\Delta\mu_{V_{0SP}}}{\Delta T} \simeq -0.45\,\frac{\mu V}{K}$ and $\frac{\Delta\sigma_{V_{0SP}}}{\Delta T} \simeq 0.50\,\frac{\mu V}{K}$ r.m.s. for a temperature variation of 100 K.

Temperature coefficients are, for the mean,

$$TC_{\mu_{V_{0SP}}} = \frac{1}{\mu_{V_{0SP}}}\frac{\partial\mu_{V_{0SP}}}{\partial T} \simeq 0.066\ \frac{\%}{K} \qquad (5.124)$$

and for the standard deviation,

$$TC_{\sigma_{V_{0SP}}} = \frac{1}{\sigma_{V_{0SP}}}\frac{\partial\sigma_{V_{0SP}}}{\partial T} \simeq 0.075\ \frac{\%}{K} \qquad (5.125)$$

5.2.2 Offset of the integrator

Again, main contributor to the offset of the integrator is the input stage which is a differential pair with emitter degeneration, exactly the same circuit topology as the preamplifier. Therefore, expression of the input-referred offset voltage is the same (5.109). Using values of table Table 4-3 and with $\sigma_{\Delta R_E/R} = 0.22\,\%$ [73], the standard deviation of the input offset voltage of the integrator is $\sigma_{V_{0SI}} \simeq 1.2$ mV r.m.s.

As the output stage of the preamplifier is a low impedance stage, the input offset current of the integrator plays no role and we can approximate the IZE of the integrator by

$$\sigma_{IZE_I} \simeq \sigma_{V_{0SI}} = 1.2\ \text{mV r.m.s.} \qquad (5.126)$$

Although the offset is a DC signal the integrator is a switched network and the transient response is relevant for the integration period, only 25 ns. The transfer function of the integrator *I(s)* is given by (4.125) (section 4.2.2.3). Two poles have been identified (4.128) and (4.129). The response V_{DCo} to DC input signal V_{DCi} is,

$$V_{DCo}(t) = L^{-1}\left[I(s)\frac{V_{DCi}}{s}\right] = L^{-1}\left[\frac{\omega_T\dfrac{1}{R_E C_f}}{(s+\omega_T)\left(s+\dfrac{1}{G_{DM0}R_C C_f}\right)}\frac{V_{DCi}}{s}\right] \qquad (5.127)$$

We can solve (5.127) using Heaviside's partial fraction expansion:

$$V_{DCo}(t) = V_{DCi}\frac{\omega_T}{R_E C_f}L^{-1}\left[\frac{\dfrac{G_{DM0}R_C C_f}{\omega_T}}{s} + \frac{\dfrac{1}{-\omega_T\left(\dfrac{1}{G_{DM0}R_C C_f}-\omega_T\right)}}{(s+\omega_T)} + \frac{\dfrac{-G_{DM0}R_C C_f}{\left(\omega_T-\dfrac{1}{G_{DM0}R_C C_f}\right)}}{s+\dfrac{1}{G_{DM0}R_C C_f}}\right] \simeq \left(\omega_T \gg \frac{1}{G_{DM0}R_C C_f}\right)$$

$$\simeq V_{DCi}L^{-1}\left[\frac{\dfrac{G_{DM0}R_C}{R_E}}{s} + \frac{\dfrac{1}{\omega_T R_E C_f}}{s+\omega_T} - \frac{\dfrac{G_{DM0}R_C}{R_E}}{s+\dfrac{1}{G_{DM0}R_C C_f}}\right] = V_{DCi}\left(\frac{G_{DM0}R_C}{R_E} + \frac{1}{\omega_T R_E C_f}e^{-\omega_T t} - \frac{G_{DM0}R_C}{R_E}e^{-\frac{t}{G_{DM0}R_C C_f}}\right)$$

(5.128)

The unity gain frequency ($f_T = 1/2\pi\omega_T$) of the Op Amp is about 200 MHz, then $\omega_T \cdot 25ns >> 1$ and we can neglect the term corrresponding to ω_T pole,

$$V_{DCo}(t) \simeq V_{DCi} \frac{G_{DM0} R_C}{R_E} \left(1 - e^{-\frac{t}{G_{DM0} R_C C_f}} \right) \qquad (5.129)$$

On the other hand, the second pole is at the kHz region, thus $t/G_{DM0}R_CC_f << 1$ for t<25 ns. If $x << 1$, a Taylor series development can be used to show that

$$e^{-x} = 1 - x + \frac{x^2}{2!} - \frac{x^3}{3!} - \ldots \simeq \Big|_{x \ll 1} 1 - x \qquad (5.130)$$

then, the transient response to a DC signals looks like linear if the integration, T_m time is short,

$$V_{DCo}(t = T_m) \simeq V_{DCi} \frac{T_m}{C_f R_E} \qquad (5.131)$$

As studied in section 4.2.2.3 the integration time constant τ_i is ideally $\tau_i = R_E C_f = 1.3$ ns, however taking into account second order effects a more precise values is $\tau_i = 1.5$ ns. Thus, apparent "gain" of the integrator for a DC signal is,

$$G_{0I} \simeq \frac{T_m}{\tau_i} \qquad (5.132)$$

thus the standard deviation of the OZE of the integrator (OZEI) for an effective integration period T_m of 22 ns is,

$$\sigma_{OZE_I} \simeq G_{0I} \sigma_{V_{0SI}} \simeq \frac{T_m}{\tau_i} \sigma_{V_{0SI}} = 18 \text{ mV r.m.s.} \qquad (5.133)$$

In Figure 5-21 we find a comparison of the theoretical expression (5.133) with results of Monte Carlo simulations for different values of the integration time. Results are compatible within the statiscal error of the simulation.

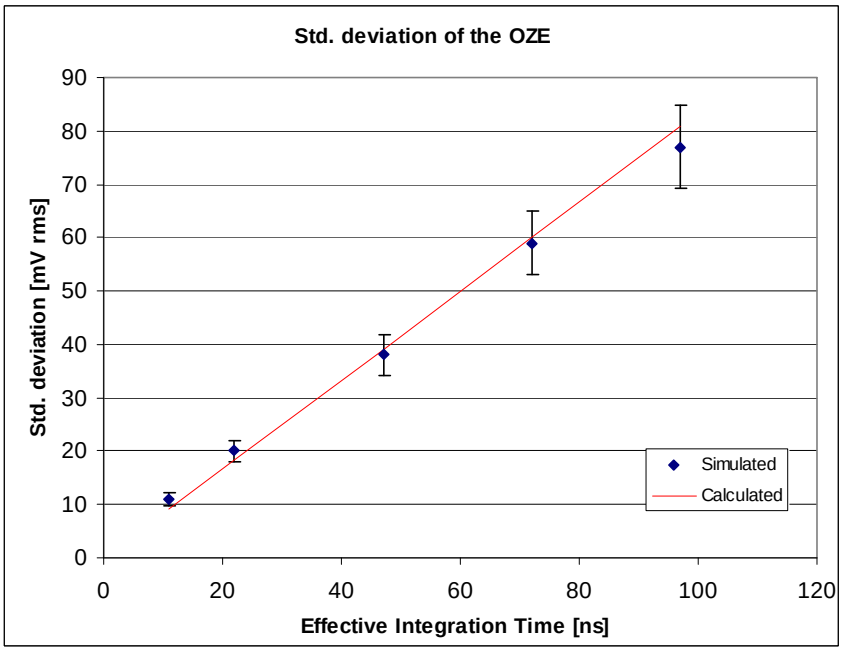

Figure 5-21. Calculation versus simulation result of the standard deviation of the OZE of the integrator for different values of integration time.

5.2.3 Offset of the full ASD channel

Looking at Figure 5-22, we will define the total offset of the channel V_0 at the input of the comparator as a function of the IZE of each separate block and the gain of each block at DC. The gain of the preamplifier $A_{DD}(0)$ and the gain of the tail correction block (the controllable gain of the cross coupled transconductor ($G_{CC}(V_{bias})$) are well defined at DC. The "gain" of the integrator for the IZE it is not so well defined because it is a switched network and transient effects have to be taken into account, we represent such gain as G_{0I}. As the open loop addition at the comparator input has three different inputs, we need to consider three different IZEs: IZE_{Ct} for the path coming from the integrator, IZE_{Ch} for the path coming from the tile correction block and IZE_{Cth} for the threshold path.

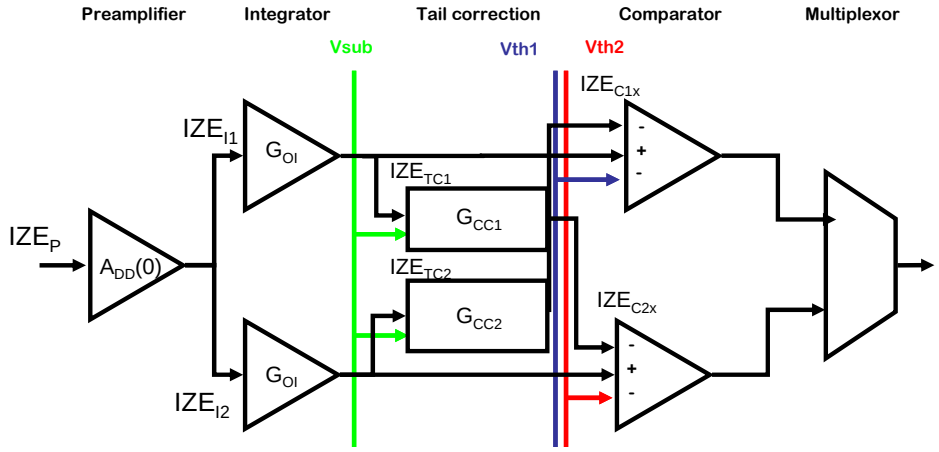

Figure 5-22. Block diagram of the offset of the channel with IZE and offset gain of the blocks.

Considering this, the total offset V_0 (for the comparator in the upper subchannel of Figure 5-22) is,

$$V_0 = G_{0I1}\left[A_{DD}(0)IZE_P + IZE_{I1}\right] + G_{CC2}\left[G_{0I2}\left[A_{DD}(0)IZE_P + IZE_{I2}\right] + IZE_{TC2}\right] + IZE_{C1t} + IZE_{C1h} + IZE_{C1th} \quad (5.134)$$

Symmetrical result would be obtained for the offset at the input of the other comparator. Reordering (5.134) and considering that the gain of the integrator and the tile compensation is matched ($G_{0I1} = G_{0I2} = G_{0I}$ and $G_{CC1} = G_{CC2} = G_{CC}$),

$$V_0 = IZE_P A_{DD}(0) G_{0I}(1+G_{CC}) + G_{0I}IZE_{I1} + G_{CC}G_{0I}IZE_{I2} + G_{CC}IZE_{TC2} + IZE_{C1t} + IZE_{C1h} + IZE_{C1th} \quad (5.135)$$

The standard deviation of V_0 is the square root of the quadratic sum of the standard deviation of the IZEs in previous expressions as all the IZEs are uncorrelated, and as $\sigma_{IZE_{I1}} = \sigma_{IZE_{I2}} = \sigma_{IZE_I}$,

$$\sigma_{V_0}^2 = \left[G_{0I}(1+G_{CC})\right]^2\left[\sigma_{IZE_P}^2\left[A_{DD}(0)\right]^2 + \sigma_{IZE_I}^2\right] + \left[G_{CC}\right]^2\sigma_{IZE_{TC}}^2 + \sigma_{IZE_{Ct}}^2 + \sigma_{IZE_{Ch}}^2 + \sigma_{IZE_{Cth}}^2 \quad (5.136)$$

The input stage of all the blocks of the ASD is based on the differential pair with emitter degeneration, therefore the standard deviation of the IZEs of those blocks has a comparable value, according Monte Carlo simulations around 4 mV r.m.s. for the tail correction block and 1 mV r.m.s. for the open loop addition. In addition the gain of tail correction block is $-0.3 < G_{CC}(V_{bias}) < 0$, thus $\left[G_{CC}\right]^2 \ll 1$. On the other hand $\left[A_{DD}\right]^2 \gg 1$ and $\left[G_{0I}\right]^2 \gg 1$,therefore, those IZEs can be neglected:

$$\sigma_{V_0}^2 \simeq \left[G_{0I}(1+G_{CC})\right]^2\left[\sigma_{IZE_P}^2\left[A_{DD}(0)\right]^2 + \sigma_{IZE_I}^2\right] \quad (5.137)$$

It is interesting to notice that according to (5.137), as $G_{CC}(V_{bias}) < 0$, the tail correction mechanism helps to decrease the apparent offset at the comparator input.

In Figure 5-23 we see the waveforms corresponding to the DM output of the preamplifier and of the two integrators. It is clear that the integrator's output is correlated with the offset at the

preamplifier, although the effect of statiscal fluctuations of integrator parameter is evident, especially on the second integrator.

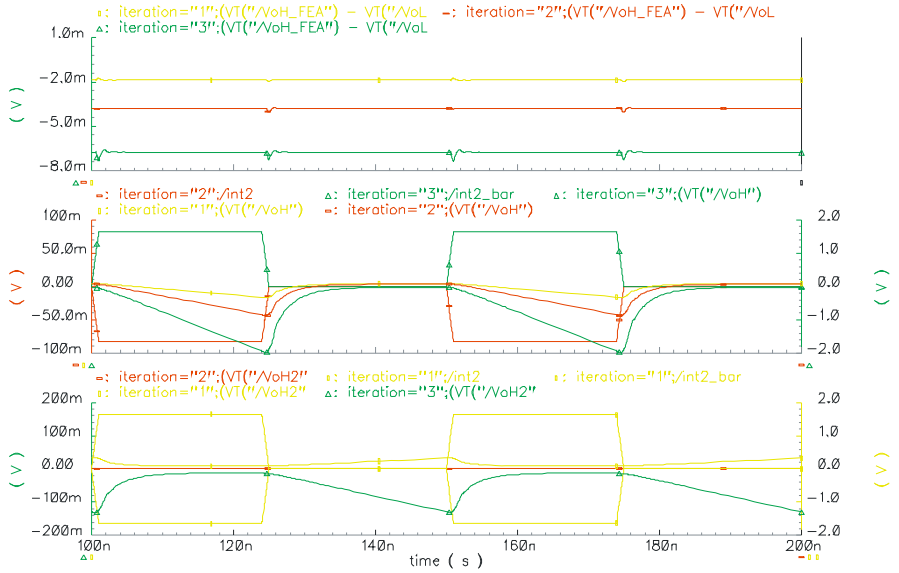

Figure 5-23. Monte Carlo simulation (3 runs) of the ASD channel with zero input signal. Top: output of the preamplifier. Mid: Output of the integrator 1 with switch control signal. Bottom: Output of the integrator 2 with switch control signal.

The standard deviation of V_0, $G_{CC}=0$ and for an effective integration period T_m of 22 ns and temperature of 300 K,

$$\sigma_{V_0} \simeq \frac{T_m}{\tau_i}\sqrt{\sigma_{IZE_P}^2\left[A_{DD}(0)\right]^2+\sigma_{IZE_I}^2} \simeq 55 \text{ mV r.m.s.} \qquad (5.138)$$

In the case of the mean value of the total offset the main systematic mismatch is on the preamplifier and in addition this IZE is multiplied by the gain of the full chain. Then, it follows that mean value for the total offset for an effective integration period T_m of 22 ns is,

$$\mu_{V_0} \simeq (1+G_{CC})\frac{T_m}{\tau_i}A_{DD}(0)\mu_{IZE_P} \simeq \Big|_{G_{CC}=0}\frac{T_m}{\tau_i}A_{DD}(0)\mu_{IZE_P} \simeq \text{-50 mV} \quad (5.139)$$

A comparison of the theoretical value of the offset of the channel (for G_{CC}=0) according to expression (5.138) and the result of Monte Carlo simulations is shown in Figure 5-24.

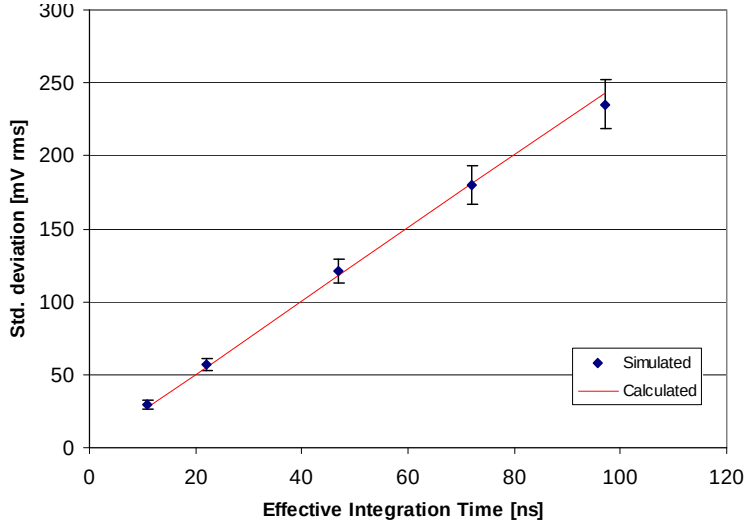

Figure 5-24. Calculation vs simulation of std. dev. of ASD offset as a function of integration time.

In the results shown in Figure 5-25 for the mean value of the offset, results are also compatible, but for large values of integration, the saturation of the integrator (DM range is ±1 V) might affect the tails of the distribution of V_0.

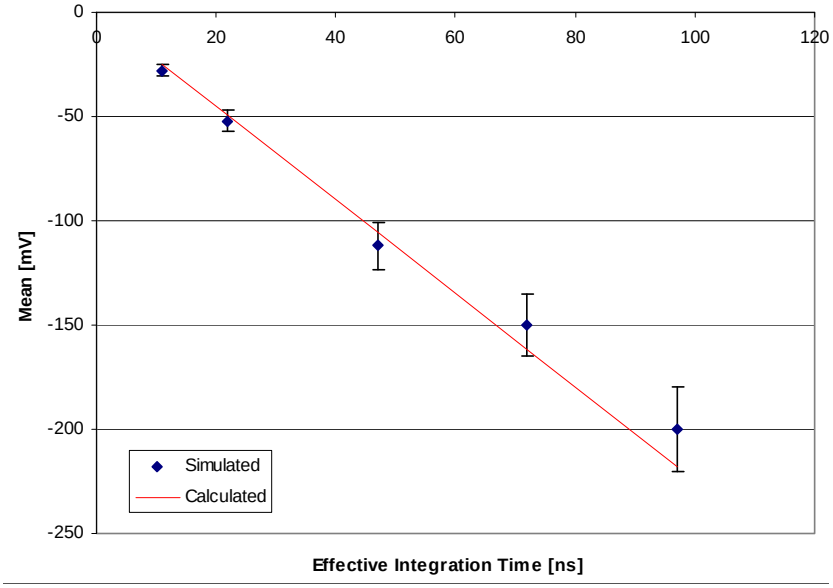

Figure 5-25. Calculation vs simulation of mean ASD offset as a function of integration time.

Regarding temperature dependence of the offset, for the mean value

$$\begin{aligned}\frac{\partial\mu_{V_0}}{\partial T}&=\frac{\partial\mu_{V_0}}{\partial G_{CC}}\frac{\partial G_{CC}}{\partial T}+\frac{\partial\mu_{V_0}}{\partial\tau_i}\frac{\partial\tau_i}{\partial T}+\frac{\partial\mu_{V_0}}{\partial A_{DD}}\frac{\partial A_{DD}}{\partial T}+\frac{\partial\mu_{V_0}}{\mu_{IZE_P}}\frac{\partial\mu_{IZE_P}}{\partial T}=\\&=\frac{T_m}{\tau_i}A_{DD}(0)\mu_{IZE_P}\frac{\partial G_{CC}}{\partial T}-(1+G_{CC})\frac{T_m}{\tau_i^2}A_{DD}(0)\mu_{IZE_P}\frac{\partial\tau_i}{\partial T}+\\&+(1+G_{CC})\frac{T_m}{\tau_i}\mu_{IZE_P}\frac{\partial A_{DD}}{\partial T}+(1+G_{CC})\frac{T_m}{\tau_i}A_{DD}(0)\frac{\partial\mu_{IZE_P}}{\partial T}=\\&=(1+G_{CC})\frac{T_m}{\tau_i}A_{DD}(0)\mu_{IZE_P}\left[\frac{G_{CC}}{1+G_{CC}}\frac{\partial G_{CC}}{G_{CC}\partial T}-\frac{\partial\tau_i}{\tau_i\partial T}+\frac{\partial A_{DD}}{A_{DD}\partial T}+\frac{\partial\mu_{IZE_P}}{\mu_{IZE_P}\partial T}\right]\end{aligned}\qquad(5.140)$$

For G_{CC}=0 and with $\frac{\partial\mu_{IZE_P}}{\mu_{IZE_P}\partial T}=\frac{\Delta\mu_{V_{0SP}}}{\mu_{V_{0SP}}\Delta T}$ and $\frac{\partial\tau_i}{\tau_i\partial T}=-\frac{1}{G_{Q\_Int}}\frac{G_{Q\_Int}}{\partial T}=-TC_{G_{Q\_Int}}$ (as τ_i=1/G_{Q_int}, see section 4.2.2.7), we have

$$\begin{aligned}\frac{\partial\mu_{V_0}}{\partial T}&=\frac{T_m}{\tau_i}A_{DD}(0)\mu_{IZE_P}\left[TC_{G_{Q\_Int}}+TC_{A_{DM}}+TC_{\mu_{V_{0SP}}}\right]=\\&=\mu_{V_0}\left[-150\ \frac{\text{ppm}}{\text{K}}-270\frac{\text{ppm}}{\text{K}}+660\frac{\text{ppm}}{\text{K}}\right]\simeq\\&=240\frac{\text{ppm}}{\text{K}}\mu_{V_0}=-15\frac{\mu\text{V}}{\text{K}}\end{aligned}\qquad(5.141)$$

In the same way it can be shown that the temperature dependence of the standard deviation of the offset is,

$$\frac{\partial \sigma_{V_0}}{\partial T} = (1+G_{CC})\frac{T_m}{\tau_i} A_{DD}(0)\sigma_{IZE_P}\left[\frac{G_{CC}}{1+G_{CC}}\frac{\partial G_{CC}}{G_{CC}\partial T} - \frac{\partial \tau_i}{\tau_i \partial T} + \frac{\partial A_{DD}}{A_{DD}\partial T} + \frac{\partial \sigma_{IZE_P}}{\sigma_{IZE_P}\partial T}\right] =$$

$$= \Big|_{G_{CC}=0} \frac{T_m}{\tau_i} A_{DD}(0)\sigma_{IZE_P}\left[TC_{G_{Q\_Imt}} + TC_{A_{DM}} + TC_{\mu_{V_{0SP}}}\right] = \tag{5.142}$$

$$= \sigma_{V_0}\left[-150\ \frac{\text{ppm}}{\text{K}} - 270\frac{\text{ppm}}{\text{K}} + 750\frac{\text{ppm}}{\text{K}}\right] \simeq 330\ \frac{\text{ppm}}{\text{K}}\ \sigma_{V_0} = 18\ \frac{\mu\text{V}}{\text{K}}$$

5.3 Power supply noise rejection

5.3.1 PSRR of the preamplifier

Power-supply voltages are not exactly constant due to the parasitic resistances, inductances and capacitances in power distribution lines and due to the power supply ripple and noise. Variations in power supply voltages contribute to the circuit output. The small signal variation on the positive (V_{cc}) and negative (V_{ee}) power supplies are v_{cc} and v_{ee}, respectively. If $v_{iC} = 0$ is assumed for simplicity, the resulting small-signal op-amp output voltage is

$$v_{oD} = A_{DM}v_{iD} + A_{+DM}v_{cc} + A_{-DM}v_{ee} \tag{5.143}$$

where A_{+DM} and A_{-DM} are the small signal gains for the positive and the negative power-supplies to the differential-mode output, respectively. Since circuits should be sensitive to changes in their differential mode input voltage but insensitive to changes in their supply voltages, this equation is rewritten below in a form that simplifies comparison of these gains referring all the effects to the input,

$$v_{oD} = A_{DM}\left(v_{iD} + \frac{A_{+DM}}{A_{DM}}v_{cc} + \frac{A_{-DM}}{A_{DM}}v_{ee}\right) = A_{DM}\left(v_{iD} + \frac{1}{PSRR^+}v_{cc} + \frac{1}{PSRR^-}v_{ee}\right) \tag{5.144}$$

where positive ($PSRR^+$) and negative ($PSRR^-$) power supply rejection ratios are defined as:

$$PSSR^+ = \frac{A_{DM}}{A_{+DM}}$$
$$PSSR^- = \frac{A_{DM}}{A_{-DM}} \tag{5.145}$$

In order to be able to calculate the PSRR of a complex system, the system can be divided into sub-circuits or into a block diagram, using control-system theory. A method is presented in [166], and as for other circuit parameters such random noise and offset it is shown that if the gain of the first stages is large enough the PSRR of the full system is given by the PSRR of the first stages. For this reason it is important to consider the PSRR of first stages, in our case the preamplifier and the input stage of the integrator.

Fully differential circuits such as the preamplifier, and other circuits of the chip, provide complete rejection of power supply variations since power supply variations are coupled identically to the two identical signal paths and consequently the differential output is zero. This is only true for fully balanced fully differential circuits, in practice mismatches cause differences in the two signal paths, and the coupling may not be identical causing imperfect cancellation. Also, if the power supply noise is large enough, nonlinearity may result and limit the extent of cancellation.

Since the PSRR depend on circuit mismatch the same method presented in chapter 4 can be used. To analyze input-output transfer functions (A_{DM}, A_{CM-DM}, A_{DM-CM} and A_{CM}) the current source was considered merely as a constant current generator with an associated output impedance. Conversely, the power supply noise generators are input signals for the bias circuitry and bias current will depend on power supply noise generators. Therefore, the bias circuit must be included in the analysis of power supply rejection. Figure 5-26 shows the bias circuit for the differential pair, the band-gap current source. The current source I_{bias} is composed by eight bipolar current mirror units (with emitter degeneration R_{Eb1}) in parallel, driven by a band-gap current master.

In this analysis it is assumed that there are no local variations of power supply. If it happens, for example between the preamplifier and its biasing circuitry, coupling can be higher. To prevent this effect, proper decoupling and layout techniques have been applied as in chapter 4.

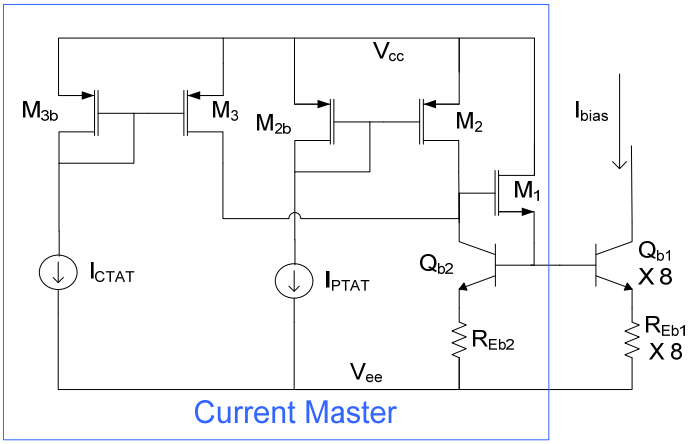

Figure 5-26. Band-Gap current source of the preamplifier.

Figure 5-27 shows the differential-mode small-signal half circuit for coupling of v_{cc} power supply variation. Since the emitter resistors R_{E1}-R_{E2} of the preamplifier are connected at a point which is virtual ground, the bias circuitry has no role in the differential-mode half circuit. The variation source v_{cc} is not directly present in differential-mode half circuit because it is a common-mode signal; however some effect is possible through the coupling with the common-mode circuit.

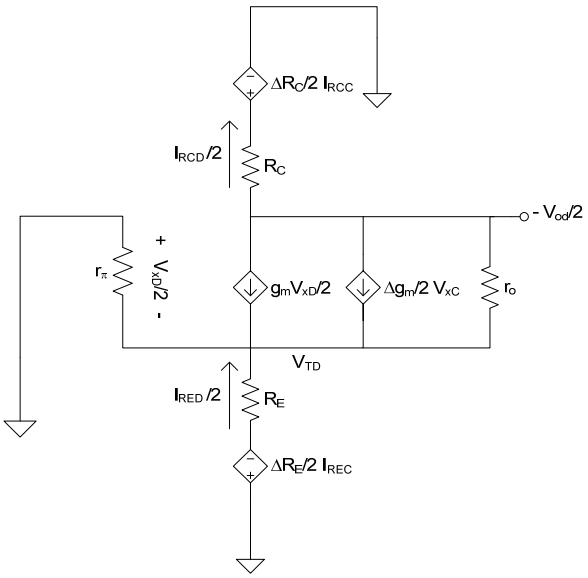

Figure 5-27. Differential-mode small-signal half circuit with mismatch generators for the analysis of the coupling of vcc power supply variation.

For the differential half-circuit,

$$V_{TD} = \left(g_m \frac{V_{xD}}{2} + \frac{\Delta g_m}{2} V_{xC} + \frac{1}{r_\pi} \frac{V_{xD}}{2} \right) R_E - \frac{\Delta R_E}{2} I_{REC}$$

$$\frac{V_{oD}}{2} = \left(g_m \frac{V_{xD}}{2} + \frac{\Delta g_m}{2} V_{xC} \right) R_C - \frac{\Delta R_C}{2} I_{RCC} \qquad (5.146)$$

$$\frac{V_{xD}}{2} = -V_{TD}$$

obtaining,

$$\frac{V_{oD}}{2} = -\frac{\Delta R_C}{2} I_{RCC} + \frac{R_C}{1 + g_m R_E} \frac{\Delta g_m}{2} V_{xC} + \frac{g_m R_C}{1 + g_m R_E} \frac{\Delta R_E}{2} I_{REC} \qquad (5.147)$$

For common-mode signals, as said before, it has to be taken into account that elements lying along the topological line of symmetry that divides the preamplifier circuit of Figure 4-3 have to be properly ratioed, such as the bias current source. As the bias current source is made of 8 identical current units, we just needed to divide it into two identical half-sources of 4 current units that can be separated by symmetry to construct the common-mode half circuit. The current master is equivalent to a voltage source, a voltage reference applied at the base of the transistors of the current units. A voltage source lying on the line of symmetry has to be replicated in each half-circuit.

The common-mode small-signal half circuit with mismatch generators for the analysis of the coupling of v_{cc} power supply variation is shown in Figure 5-28. Since v_{cc} is not present in the differential half circuit there is not any independent generator, thus the approximated values without mismatch generators ($\mathcal{I}_{RCD}/2$, $\mathcal{I}_{REC}/2$ and $\mathcal{V}_{xD}/2$) will be zero and the mismatch generators in the common-mode half circuit have no role in a first approximation, they are not present in the common-mode half circuit.

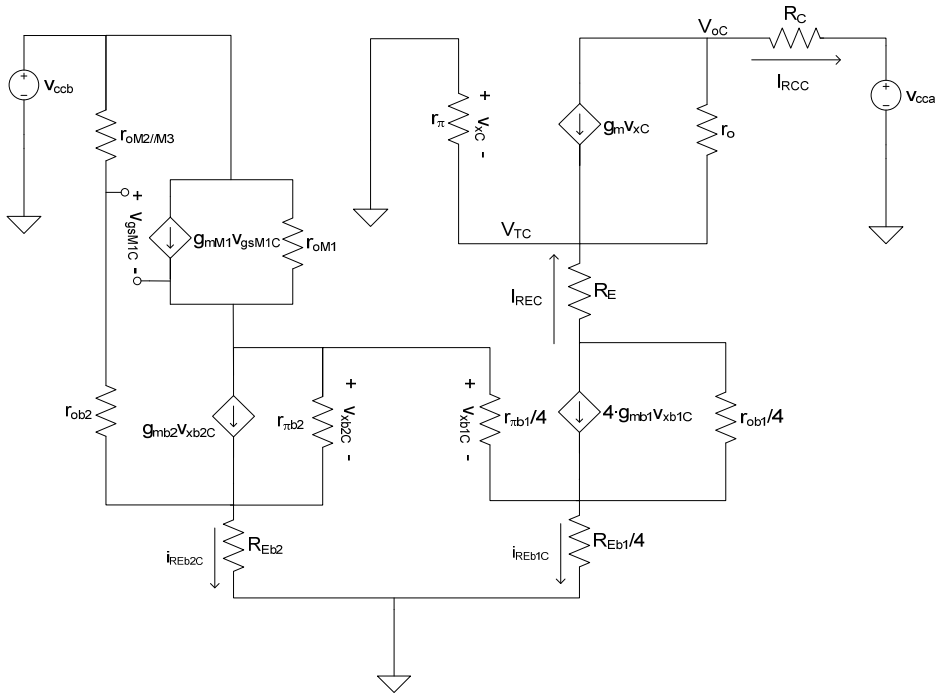

Figure 5-28. Common-mode small-signal half circuit with mismatch generators for the analysis of the coupling of v_{cc} power supply variation.

The v_{cc} generator affects the preamplifier through the collector resistor R_C and though the current source, both effects can be analyzed independently (superposition), greatly simplifying calculations. We represent effect of power supply variation in bias circuitry by v_{ccb} and on preamplifier R_C by v_{cca} generators, thus the common-mode output voltage can be expressed as:

$$v_{oC} = v_{oC}\big|_{vcca=0} + v_{oC}\big|_{vccb=0} \tag{5.148}$$

The output resistance r_o of Q_1-Q_2 is relevant for PSRR+ calculation and it included in the common-mode half circuit of Figure 5-28. The output resistance r_o in the small signal model of the bipolar transistor is defined as the ratio of the AC variation of v_{CE} to the variation of i_C. For a specific value of collector current IC the output resistance is given [67] by $r_o = V_E / I_C$, where V_E is the Early voltage. According to the model of the transistor (see section A)V_E is about 40 V (for an area parameter value of 3), then the output resistance r_o is about 83.3 kΩ for a collector current of 4x120μA. Relevant device parameters derived from [73] and [162], are summarized in Table 5-1.

Parameter	Value	Parameter	Value
$g_{m\,=\,4\,x\,}g_{mb1}$	19 mS	I_{bias}	990 μA
r_π	8 kΩ	$r_{oM2//M3}$	400 kΩ
r_o	80 kΩ	C_{sbM23}	300 fF
$\sigma_{\Delta Rc}/R_C$	0.25 %	R_{oIb}	135 kΩ
$\sigma_{\Delta Is}/Is=\sigma_{\Delta gm}/g_m$	0.7 %	C_{oIb}	450 fF
$\sigma_{\Delta Rc}/R_C$	0.22 %	R_{Eb2}/R_{Eb1}	1.5
R_E	460 Ω	$\sigma_{\Delta REb1}/R_{Eb1}$	0. 5 %
R_C	2.4 kΩ	g_{mb2}	3 mS

Table 5-1. Value of device parameters

With only the effect of v_{cca} generator (v_{ccb}=0) the bias current source can be replaced in common-mode half circuit by its output impedance R_{oIb} as in previous section, then we can write the following expressions,

$$V_{TC} = -g_m V_{TC}\left(R_E + 2R_{oIb}\right) + \frac{v_{oC}\big|_{vccb=0} - V_{TC}}{r_o}\left(R_E + 2R_{oIb}\right) - \frac{V_{TC}}{r_\pi} \tag{5.149}$$

$$\frac{v_{cca} - v_{oC}\big|_{vccb=0}}{R_C} = -g_m V_{TC} + \frac{v_{oC}\big|_{vccb=0} - V_{TC}}{r_o} \tag{5.150}$$

From (5.149) and (5.150), and with $g_m >> 1/r_o$,

$$v_{oC}\big|_{vccb=0} \simeq v_{cca}\left(1 - \frac{R_C}{g_m r_o r_\pi}\right) \tag{5.151}$$

The signals that control mismatch generators in differential-mode half circuit are I_{RCC}, I_{REC} and V_{xC}. We will find approximations to these quantities $\mathcal{I}_{RCC}$, $\mathcal{I}_{REC}$ and $\mathcal{V}_{xC}$. First, using the simplified common-mode half circuit with v_{ccb}=0,

$$\begin{aligned}
\mathcal{V}_{xC}\big|_{v_{ccb}=0} &= \frac{-v_{cca}}{g_m r_o} \\
\mathcal{I}_{REC}\big|_{v_{ccb}=0} &= -\frac{V_{TC}}{\left(R_E + 2R_{oIbE}\right)} = \frac{\mathcal{V}_{xC}}{\left(R_E + 2R_{oIbE}\right)} = \frac{-v_{cca}}{g_m\left(R_E + 2R_{oIbE}\right) r_o} \\
\mathcal{I}_{RCC}\big|_{v_{ccb}=0} &= \mathcal{I}_{r\pi C}\big|_{v_{ccb}=0} + \mathcal{I}_{REC}\big|_{v_{ccb}=0} \simeq \mathcal{I}_{r\pi C}\big|_{v_{ccb}=0} = \frac{\mathcal{V}_{xC}}{r_\pi} = \frac{-v_{cca}}{g_m r_o r_\pi}
\end{aligned} \tag{5.152}$$

For the v_{ccb} generator (v_{cca}=0) the full common-mode half circuit in Figure 5-28 has to be considered. Following expressions can be easily derived (considering $g_{mb2}>>1/r_{ob2}$ and $g_{mb1}>>1/r_{ob1}$)

$$v_{ccb} = g_{mb2} v_{xb2C} r_{oM2} + v_{gsC} + v_{xb2C} + R_{Eb2C}\left(g_{mb2} v_{xb2C} + \frac{v_{xb2C}}{r_{\pi b2}} \right) \quad (5.153)$$

$$v_{ccb} = \left(\frac{v_{xb2C}}{r_{\pi b2}} + \frac{v_{xb1C}}{r_{\pi b1}} - g_{nM1} v_{gsC} \right) r_{oM1} + v_{xb1C} + R_{Eb1C}\left(g_{mb1} v_{xb1C} + \frac{v_{xb1C}}{r_{\pi b1}} \right) \quad (5.154)$$

$$v_{xb1C} + R_{Eb1C}\left(g_{mb1} v_{xb1C} + \frac{v_{xb1C}}{r_{\pi b1}} \right) = v_{xb2C} + R_{Eb2C}\left(g_{mb2} v_{xb2C} + \frac{v_{xb2C}}{r_{\pi b2}} \right) \quad (5.155)$$

With $g_{mb2}>>1/r_{\pi b2}$ and $g_{mb1}>>1/r_{\pi b1}$ expression (5.155) can be rewritten as

$$v_{xb2C} \simeq \frac{1 + g_{mb1} R_{Eb1C}}{1 + g_{mb2} R_{Eb2C}} v_{xb1C} \quad (5.156)$$

It can be shown [66] that current mirrors with emitter degeneration have to be matched, having $I_{Cb1} R_{Eb1} = I_{Cb2} R_{Eb2}$ and therefore $g_{mb1} R_{Eb1} = g_{mb2} R_{Eb2}$. Then,

$$v_{xb2C} \simeq v_{xb1C} \quad (5.157)$$

Using (5.157) in (5.153) and (5.154) and taking $g_{mb2}>>1/r_{ob2}$, $g_{mb2}>>1/r_{\pi b2}$, $g_{mb2}>>1/r_{ob2}$, $g_{mb1}>>1/r_{\pi b1}$, $g_{mM1}>>1/r_{oM1}$, $g_m>>1/r_o$ and $g_m>>1/r_\pi$ we obtain,

$$v_{xb2C}\big|_{v_{cca}=0} \simeq \frac{1}{g_{mb2}} \frac{1}{r_{oM2//M3}} v_{ccb} \quad (5.158)$$

Then, the approximated controlling signals of mismatch generators for v_{ccb} supply are

$$\begin{aligned} \boldsymbol{\mathcal{I}}_{\boldsymbol{RCC}}\big|_{v_{ccba}=0} &\simeq -\frac{g_{mb1}}{g_{mb2}} \frac{1}{r_{oM2//M3}} v_{ccb} \\ \boldsymbol{\mathcal{V}}_{\boldsymbol{xC}}\big|_{v_{cca}=0} &\simeq \frac{g_{mb1}}{g_m g_{mb2}} \frac{1}{r_{oM2//M3}} v_{ccb} \simeq\big|_{g_m \simeq g_{mb1}} \frac{1}{g_{mb2}} \frac{1}{r_{oM2//M3}} v_{ccb} \\ \boldsymbol{\mathcal{I}}_{\boldsymbol{RCC}}\big|_{v_{cca}=0} &\simeq\big|_{r_\pi \gg 1/g_m} \boldsymbol{\mathcal{I}}_{\boldsymbol{REC}}\big|_{v_{cca}=0} \simeq -\frac{g_{mb1}}{g_{mb2}} \frac{1}{r_{oM2//M3}} v_{ccb} \end{aligned} \quad (5.159)$$

And the common-mode output due to v_{ccb} supply

$$v_{oC}\big|_{vcca=0} \simeq -\frac{g_{mb1}}{g_{mb2}} \frac{R_C}{r_{oM2//M3}} v_{ccb} \quad (5.160)$$

Adding both v_{cca} and v_{ccb} effects for approximated controlling signals of mismatch generators we obtain

$$\begin{aligned} \boldsymbol{\mathcal{V}}_{\boldsymbol{xC}} &= \boldsymbol{\mathcal{V}}_{\boldsymbol{xC}}\big|_{v_{ccb}=0} + \boldsymbol{\mathcal{V}}_{\boldsymbol{xC}}\big|_{v_{cca}=0} \simeq \left(\frac{1}{g_{mb2} r_{oM2//M3}} - \frac{1}{g_m r_o} \right) v_{cc} \simeq \frac{g_m r_o - g_{mb2} r_{oM2//M3}}{g_{mb2} r_{oM2//M3} g_m r_o} v_{cc} \\ \boldsymbol{\mathcal{I}}_{\boldsymbol{REC}} &= \boldsymbol{\mathcal{I}}_{\boldsymbol{REC}}\big|_{v_{ccb}=0} + \boldsymbol{\mathcal{I}}_{\boldsymbol{REC}}\big|_{v_{ccba}=0} \simeq -\left(\frac{g_{mb1}}{g_{mb2}} \frac{1}{r_{oM2//M3}} + \frac{1}{g_m \left(R_E + 2R_{olbE} \right) r_o} \right) v_{cc} \simeq -\frac{g_{mb1}}{g_{mb2}} \frac{1}{r_{oM2//M3}} v_{cc} \\ \boldsymbol{\mathcal{I}}_{\boldsymbol{RCC}} &= \boldsymbol{\mathcal{I}}_{\boldsymbol{RCC}}\big|_{v_{ccb}=0} + \boldsymbol{\mathcal{I}}_{\boldsymbol{RCC}}\big|_{v_{ccba}=0} \simeq -\left(\frac{g_{mb1}}{g_{mb2}} \frac{1}{r_{oM2//M3}} + \frac{1}{g_m r_o r_\pi} \right) v_{cc} \simeq -\frac{g_{mb1}}{g_{mb2}} \frac{1}{r_{oM2//M3}} v_{cc} \end{aligned} \quad (5.161)$$

And the common-mode output,

$$v_{oC} = v_{oC}\big|_{vccb=0} + v_{oC}\big|_{vcca=0} \simeq \left(1 - \frac{R_C}{g_m r_o r_\pi} - \frac{g_{mb1}}{g_{mb2}} \frac{R_C}{r_{oM2//M3}}\right) v_{cc} \qquad (5.162)$$

and the gain from the v_{cc} power supply variation generator to the common-mode output,

$$A_{+CM} \simeq 1 - \frac{R_C}{g_m r_o r_\pi} - \frac{g_{mb1}}{g_{mb2}} \frac{R_C}{r_{oM2//M3}} = 0.962 \qquad (5.163)$$

Expression (5.152) shows that, for an infinite transistor output resistance, variations in v_{cc} do not affect the controlling voltage of the transistor transconductance as stated above. Replacing the terms evaluated in (5.152) in (5.147) and with $g_m R_{olb} >> 1$ we find that

$$\frac{V_{oD}}{2} = \frac{\Delta R_C}{2} \frac{g_{mb1}}{g_{mb2}} \frac{1}{r_{oM2//M3}} v_{cc} + \frac{R_C}{1+g_m R_E} \frac{\Delta g_m}{2} \frac{g_m r_o - g_{mb2} r_{oM2//M3}}{g_{mb2} r_{oM2//M3} g_m r_o} v_{cc} - \frac{g_m R_C}{1+g_m R_E} \frac{\Delta R_E}{2} \frac{g_{mb1}}{g_{mb2}} \frac{1}{r_{oM2//M3}} v_{cc} \simeq$$

$$\simeq \Big|_{g_m = g_{mb1}} \frac{1}{2} \frac{g_m}{g_{mb2}} \frac{R_C}{r_{oM2//M3}} \left(\frac{\Delta R_C}{R_C} - \frac{\left(g_m r_o - g_{mb2} r_{oM2//M3}\right)}{\left(1+g_m R_E\right) g_m r_o} \frac{\Delta g_m}{g_m} - \frac{\Delta R_E}{R_E} \right) v_{cc} \qquad (5.164)$$

And that the positive power supply gains to differential-mode (A^+DM) and common-mode (A^+CM) outputs are,

$$A_{+DM} \simeq \frac{g_m}{g_{mb2}} \frac{R_C}{r_{oM2//M3}} \left(\frac{\Delta R_C}{R_C} - \frac{\left(g_m r_o - g_{mb2} r_{oM2//M3}\right)}{\left(1+g_m R_E\right) g_m r_o} \frac{\Delta g_m}{g_m} - \frac{\Delta R_E}{R_E} \right) \qquad (5.165)$$

We can now compute the standard deviation of A^+DM

$$\sigma_{A_{+DM}} \simeq \frac{g_m}{g_{mb2}} \frac{R_C}{r_{oM2//M3}} \sqrt{\left(\frac{\sigma_{\Delta R_C}}{R_C}\right)^2 + \left(\frac{\left(g_m r_o - g_{mb2} r_{oM2//M3}\right)}{\left(1+g_m R_E\right) g_m r_o} \frac{\sigma_{\Delta g_m}}{g_m}\right)^2 + \left(\frac{\sigma_{\Delta R_E}}{R_E}\right)^2}$$

$$\simeq \frac{g_m}{g_{mb2}} \frac{R_C}{r_{oM2//M3}} \sqrt{\left(\frac{\sigma_{\Delta R_C}}{R_C}\right)^2 + \left(\frac{\sigma_{\Delta R_E}}{R_E}\right)^2} \simeq \pm 126 \cdot 10^{-6}\ rms \qquad (5.166)$$

Figure 5-29 shows Monte Carlo simulations for positive power supply gain to the differential-mode (A_{+DM}) and common-mode (A_{+CM}) outputs. The A_{+DM} gain is mainly due to the common-mode current induced by biasing circuit. Standard deviation of A_{+DM} is about -78 dB, the low frequency $PSRR^+$ is about 93 dB, showing the nice capabilities of differential circuits to reject common mode signals and thus power supply variations.

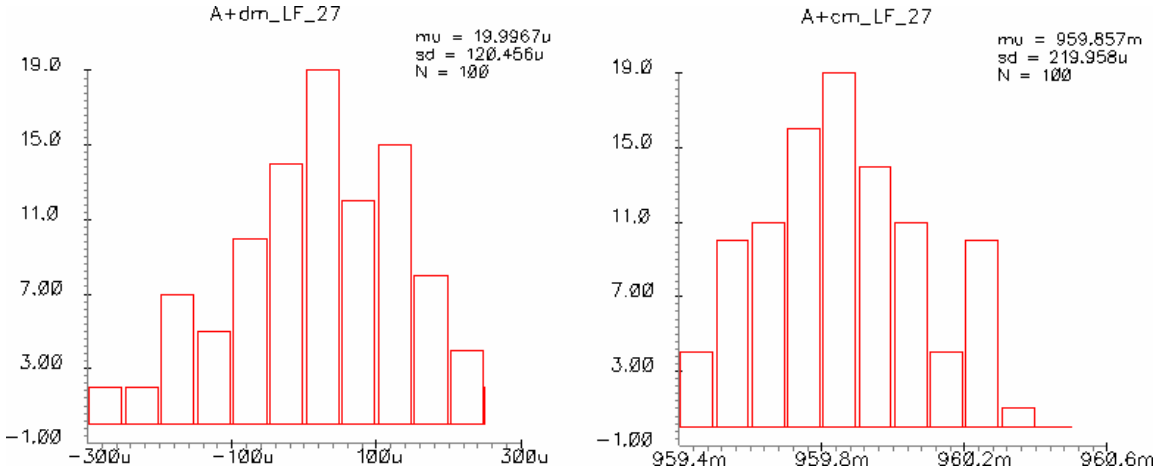

Figure 5-29 Positive power supply gain (low frequency) to the differential-mode (left) and common-mode (right) outputs.

The CM half circuit for the variations of the negative power supply is shown in Figure 5-30.

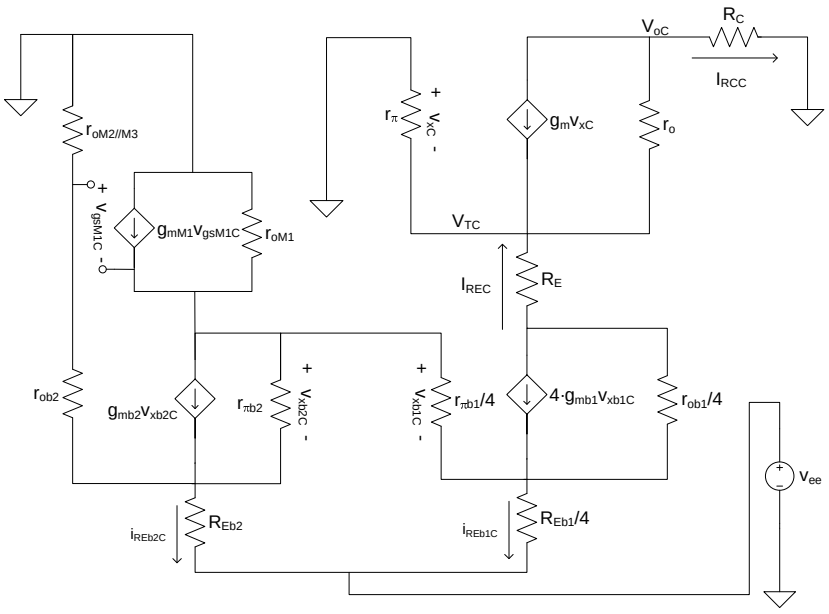

Figure 5-30. Common-mode small-signal half circuit for the analysis of the coupling of v_{ee} power supply variation.

As explained above, mismatch generators in common-mode circuit have no role with this approximation because there is no independent generator in differential-mode half circuit. The analysis is quite similar to the case of v_{ccb} generator. Following expressions can be easily derived (considering $g_{mb2} >> 1/r_{ob2}$ and $g_{mb1} >> 1/r_{ob1}$)

$$0 = v_{ee} + g_{mb2} v_{xb2C} r_{oM2} + v_{gsC} + v_{xb2C} + R_{Eb2C}\left(g_{mb2} v_{xb2C} + \frac{v_{xb2C}}{r_{\pi b2}} \right) \quad (5.167)$$

$$0 = v_{ee} + \left(\frac{v_{xb2C}}{r_{\pi b2}} + \frac{v_{xb1C}}{r_{\pi b1}} - g_{nM1} v_{gsC} \right) r_{oM1} + v_{xb1C} + R_{Eb1C}\left(g_{mb1} v_{xb1C} + \frac{v_{xb1C}}{r_{\pi b1}} \right) \quad (5.168)$$

$$v_{xb1C} + R_{Eb1C}\left(g_{mb1} v_{xb1C} + \frac{v_{xb1C}}{r_{\pi b1}} \right) = v_{xb2C} + R_{Eb2C}\left(g_{mb2} v_{xb2C} + \frac{v_{xb2C}}{r_{\pi b2}} \right) \quad (5.169)$$

As said before, from (5.155) or (5.169) ,

$$v_{xb2C} \simeq v_{xb1C} \quad (5.170)$$

Then taking $g_{mb2} >> 1/r_{ob2}$, $g_{mb2} >> 1/r_{\pi b2}$, $g_{mb2} >> 1/r_{ob2}$, $g_{mb1} >> 1/r_{\pi b1}$, $g_{mM1} >> 1/r_{oM1}$, $g_m >> 1/r_o$ and $g_m >> 1/r_\pi$ we obtain,

$$v_{xb2C} \simeq -\frac{1}{g_{mb2}} \frac{1}{r_{oM2//M3}} v_{ee} \quad (5.171)$$

Regarding the bias current controlled by v_{ee} the transistor Q_1-Q_2 is in common-base configuration, the current entering the emitter $-i_{REC} = g_{mb1} v_{xb1C}$ will be transmitted to the collector node. The approximated controlling signals of mismatch generators for v_{ee} supply are

$$\mathcal{G}_{RCC} \simeq \frac{g_{mb1}}{g_{mb2}} \frac{1}{r_{oM2//M3}} v_{ee}$$

$$\mathcal{V}_{xC} \simeq \frac{g_{mb1}}{g_m g_{mb2}} \frac{1}{r_{oM2//M3}} v_{ccb} \simeq \Big|_{g_m \simeq g_{mb1}} - \frac{1}{g_{mb2}} \frac{1}{r_{oM2//M3}} v_{ee} \qquad (5.172)$$

$$\mathcal{G}_{RCC} \simeq \Big|_{r_\pi \gg 1/g_m} \mathcal{G}_{RCC}\Big|_{v_{cca}=0} \simeq \frac{g_{mb1}}{g_{mb2}} \frac{1}{r_{oM2//M3}} v_{ee}$$

And the common-mode output due to v_{ccb} supply

$$v_{oC} \simeq \frac{g_{mb1}}{g_{mb2}} \frac{R_C}{r_{oM2//M3}} v_{ee} \qquad (5.173)$$

Therefore the common-mode gain for the negative power supply A_{-CM} is,

$$A_{-CM} \simeq \frac{g_{mb1}}{g_{mb2}} \frac{R_C}{r_{oM2//M3}} \simeq 0.038 \qquad (5.174)$$

Since there-are no differential-mode input signals, apart from mismatch generators, the differential-mode half circuit for vee is exactly the same than for v_{cc} variations and equation (5.147) is also valid. Then with (5.147) and (5.172),

$$\frac{V_{oD}}{2} = -\frac{\Delta R_C}{2} \frac{g_{mb1}}{g_{mb2}} \frac{1}{r_{oM2//M3}} v_{ee} - \frac{R_C}{1+g_m R_E} \frac{\Delta g_m}{2} \frac{1}{g_{mb2}} \frac{1}{r_{oM2//M3}} v_{ee} + \frac{g_m R_C}{1+g_m R_E} \frac{\Delta R_E}{2} \frac{g_{mb1}}{g_{mb2}} \frac{1}{r_{oM2//M3}} v_{ee}$$

$$\simeq \Big|_{g_{mb1} \simeq g_m} \frac{1}{2} \frac{g_{mb1}}{g_{mb2}} \frac{R_C}{r_{oM2//M3}} \left(-\frac{\Delta R_C}{R_C} - \frac{1}{1+g_m R_E} \frac{\Delta g_m}{g_m} + \frac{\Delta R_E}{R_E} \right) v_{ee} \qquad (5.175)$$

Then, the negative power supply differential mode gain A_{-DM} is

$$A_{-DM} \simeq \frac{g_{mb1}}{g_{mb2}} \frac{R_C}{r_{oM2//M3}} \left(-\frac{\Delta R_C}{R_C} - \frac{1}{1+g_m R_E} \frac{\Delta g_m}{g_m} + \frac{\Delta R_E}{R_E} \right) \qquad (5.176)$$

The role of the current source output resistance is less important than in the case of rejection of input common-mode signals ($A_{CM\text{-}DM}$)due to the contribution of g_{bias}, if this were not significant A_{-DM} would be exactly $A_{CM\text{-}DM}$ since the v_{ee} generator is a common-mode signal applied at point equivalent to an input common-mode signal. We can now compute the standard deviation of A_{-DM}

$$\sigma_{A_{-DM}} \simeq \frac{g_{mb1}}{g_{mb2}} \frac{R_C}{r_{oM2//M3}} \sqrt{\left(\frac{\sigma_{\Delta R_C}}{R_C}\right)^2 + \left(\frac{1}{g_m R_E} \frac{\sigma_{\Delta g_m}}{g_m}\right)^2 + \left(\frac{\sigma_{\Delta R_E}}{R_E}\right)^2}$$

$$= \frac{g_{mb1}}{g_{mb2}} \frac{R_C}{r_{oM2//M3}} \sqrt{\left(\frac{\sigma_{\Delta R_C}}{R_C}\right)^2 + \left(\frac{1}{g_m R_E} \frac{\sigma_{\Delta I_S}}{I_S}\right)^2 + \left(\frac{\sigma_{\Delta R_E}}{R_E}\right)^2} = \pm 126 \cdot 10^{-6}\ rms \qquad (5.177)$$

As in the case of A_{+DM} and $A_{DM\text{-}CM}$ and $A_{CM\text{-}DM}$ the transistor mismatch terms are mostly cancelled out, this is a benefit of the emitter degeneration circuit.

Figure 5-31 shows the negative power supply gain (low frequency) to the differential-mode (A_{-DM}) and common-mode (A_{-CM}) outputs. A_{-DM} has mean value close to zero and the standard deviation fits quite well with first order estimation of (5.177). The A_{-CM} low frequency mean value is also in agreement with (5.174). Since the relevant output is the differential one the mean $PSRR^-$ is infinite whereas the standard deviation of the low frequency $PSRR^-$ is about -87 dB.

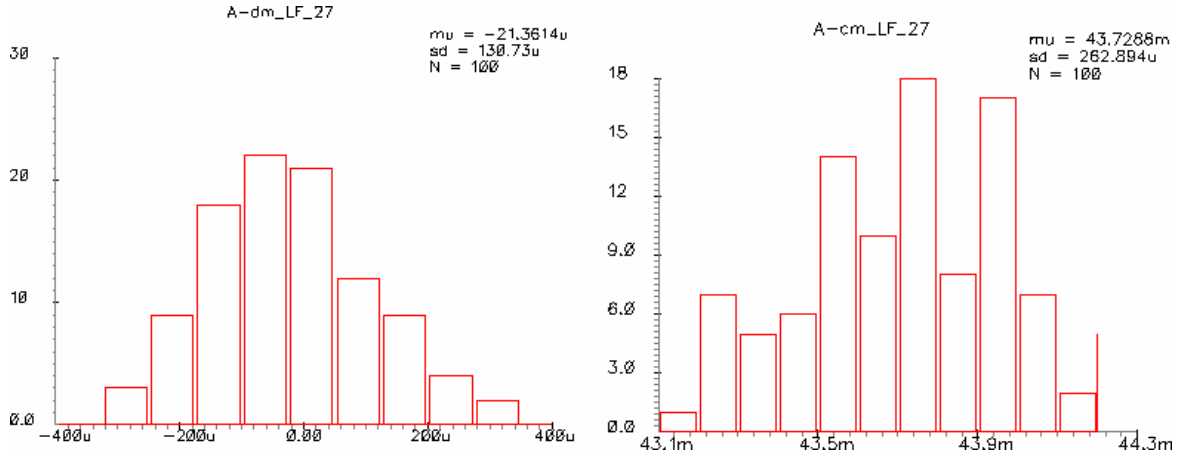

Figure 5-31 Negative power supply gain to the differential-mode (left) and common-mode (right) outputs.

Table 5-2 summarizes results for low frequency power supply rejection gains for first order approximation and for Monte Carlo simulations of matching variations.

	Calculations		Monte Carlo	
	Mean	Std. Dev.	Mean	Std. Dev.
$\mathbf{A_{+DM}}$	0	$126\cdot10^{-6}$	≈0	$120\cdot10^{-6}$
$\mathbf{A_{+CM}}$	$962\cdot10^{-3}$	-	$960\cdot10^{-3}$	$3\cdot10^{-6}$
$\mathbf{PSRR^{+}}$	∞	93 dB	∞	93 dB
$\mathbf{A_{-DM}}$	0	$126\cdot10^{-6}$	≈0	$121\cdot10^{-6}$
$\mathbf{A_{-CM}}$	$38\cdot10^{-3}$	-	$43\cdot10^{-3}$	$460\cdot10^{-6}$
$\mathbf{PSRR^{-}}$	∞	93 dB	∞	93 dB

Table 5-2. Statistical parameters of preamplifier power supply rejection gains for first order approximation and for Monte Carlo simulations of matching variations.

So far it has been analyzed the low frequency supply rejection, but this rejection worsens with frequency. Both, $A_{+CM}(s)$ and $A_{+DM}(s)$ depend on a high impedance node of bias circuitry: the source of MOS transistors M2 and M3 (depend as $1/r_{oM2//M3}$). The source to bulk capacitance at this node C_{sbM23} decreases the impedance, increasing the vee coupling. If $r_{oM2//M3}$ is replaced by the complex impedance $Z_{oM2//M3}(s) = R_{oM2//M3} \,||\, (1/sC_{sbM23})$ in (5.165),

$$A_{+DM}(s) \simeq \frac{g_m}{g_{mb2}} \frac{R_C}{r_{oM2//M3}} \left(\frac{\Delta R_C}{R_C} - \frac{(g_m r_o - g_{mb2} r_{oM2//M3})}{(1+g_m R_E) g_m r_o} \frac{\Delta g_m}{g_m} - \frac{\Delta R_E}{R_E} \right) (1 + s r_{oM2//M3} C_{sbM23}) \quad (5.178)$$

and in (5.163)

$$A_{+CM}(s) \simeq \Big|_{g_m r_o r_\pi \gg R_C} 1 - \frac{g_{mb1}}{g_{mb2}} \frac{R_C}{r_{oM2//M3}} (1 + s r_{oM2//M3} C_{sbM23}) \simeq \left(1 - \frac{g_{mb1}}{g_{mb2}} \frac{R_C}{r_{oM2//M3}}\right) \left(1 - s \frac{\frac{g_{mb1}}{g_{mb2}} R_C C_{sbM23}}{1 - \frac{g_{mb1}}{g_{mb2}} \frac{R_C}{r_{oM2//M3}}} \right)$$

(5.179)

For $A_{+DM}(s)$ there is a dominant zero at frequency $1/2\pi C_{sbM23} r_{oM2//M3} \approx 1$ MHz. For $A_{+CM}(s)$ the low frequency gain is 1 (0dB) and decrease with frequency because the term that depends on $1/r_{oM2//M3}$ increases, the -3dB frequency it is about 30MHz according to (5.179). Simulations show that current flows through the collector substrate capacitance of Q_1-Q_2 with a corner frequency of about 200kHz, however this effect is not seen in common-mode PSRR gain for reasons pointed out above and in the differential-mode PSRR because this common-mode current does not flow through the mismatched elements of Q_1-Q_2 (no mismatch generator is affected).

Doing the same for $A_{-DM}(s)$ we note the same frequency behavior as for $A_{+DM}(s)$,

$$A_{-DM}(s) \simeq \frac{g_{mb1}}{g_{mb2}} \frac{R_C}{r_{oM2//M3}} \left(-\frac{\Delta R_C}{R_C} - \frac{1}{1+g_m R_E} \frac{\Delta g_m}{g_m} + \frac{\Delta R_E}{R_E} \right) \left(1 + s r_{oM2//M3} C_{sbM23}\right) \quad (5.180)$$

and also for $A_{-CM}(s)$ there is a dominant zero in the same position,

$$A_{-CM}(s) \simeq \frac{g_{mb1}}{g_{mb2}} \frac{R_C}{r_{oM2//M3}} \left(1 + s r_{oM2//M3} C_{sbM23}\right) \quad (5.181)$$

Figure 5-32 shows the frequency dependence of power supply gains to differential and common mode outputs. For $A_{+DM}(s)$, $A_{-DM}(s)$ and $A_{-CM}(s)$ there is a dominant zero at about MHz as expected. Then, the gain increases until other parasitic capacitors cause the DM gain to fall at very high frequencies. $A_{+CM}(s)$ gain decreases with frequency and the -3 dB according simulation is at 30 MHz.

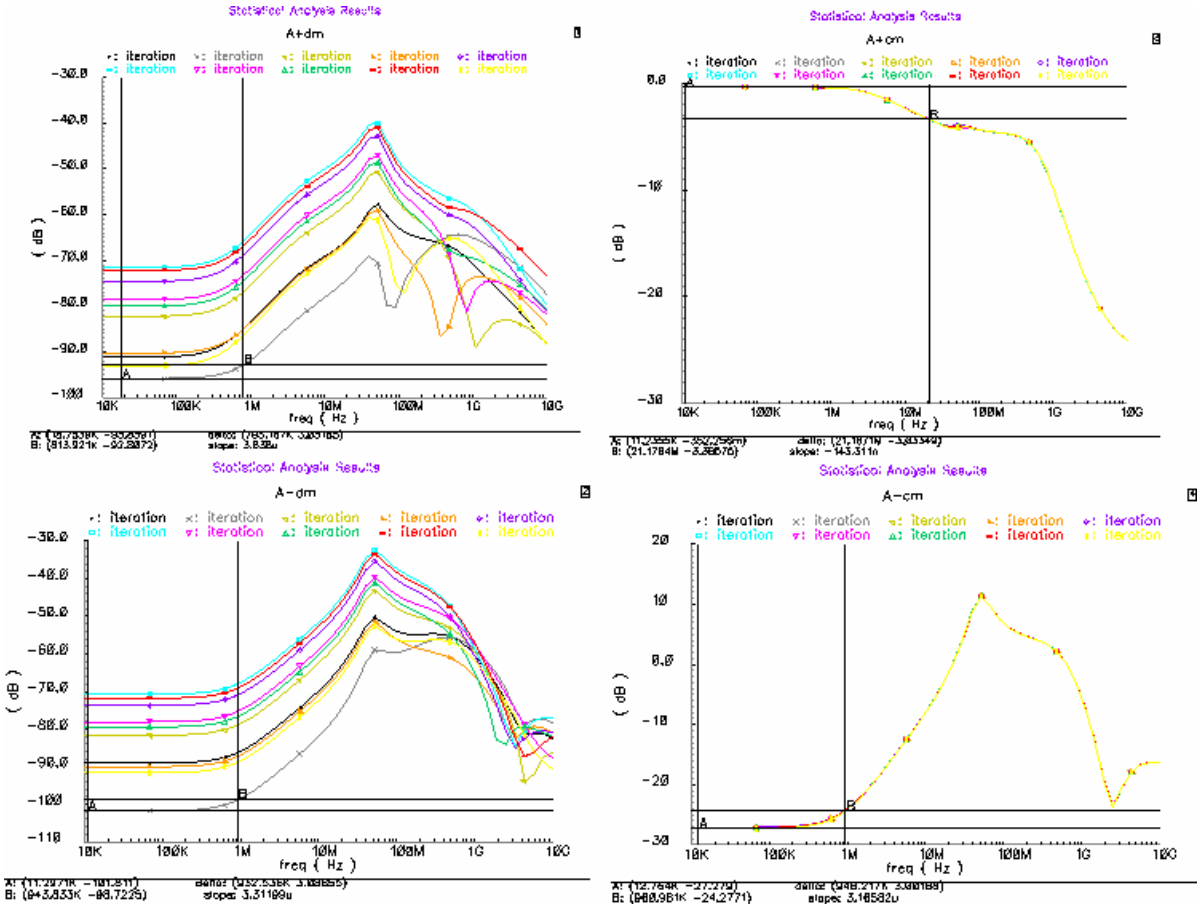

Figure 5-32. Monte Carlo simulations (Mismatch, 10 runs) of the v_{cc} gain (top) to the DM (left) and CM (right) outputs and of the v_{ee} gain (bottom) to the DM (left) and CM (right) outputs

5.3.2 PSRR of the integrator

The small signal variation on the positive (V_{cc}) and negative (V_{ee}) power supplies are v_{cc} and v_{ee}, respectively. If $v_{iC} = 0$ is assumed for simplicity, the resulting small-signal integrator's input stage output current is

$$i_{oD} = G_{DM} v_{iD} + G_{+DM} v_{cc} + G_{-DM} v_{ee} \quad (5.182)$$

where G_{+DM} and G_{-DM} are the small signal gains (or transconductances) for the positive and the negative power-supplies to the differential-mode current output, respectively. Since circuits should be

sensitive to changes in their differential mode input voltage but insensitive to changes in their supply voltages, this equation is rewritten below in a form that simplifies comparison of these gains referring all the effects to the input,

$$i_{oD} = G_{DM}\left(v_{iD} + \frac{G_{+DM}}{G_{DM}}v_{cc} + \frac{G_{-DM}}{G_{DM}}v_{ee}\right) = G_{DM}\left(v_{iD} + \frac{1}{PSRR^{+}}v_{cc} + \frac{1}{PSRR^{-}}v_{ee}\right) \qquad (5.183)$$

Positive ($PSRR^{+}$) and negative ($PSRR^{-}$) power supply rejection ratios are defined

$$PSSR^{+} = \frac{G_{DM}}{G_{+DM}} \qquad PSSR^{-} = \frac{G_{DM}}{G_{-DM}} \qquad (5.184)$$

To analyze input-output transfer functions (G_{DM}, $G_{CM\text{-}DM}$, $G_{DM\text{-}CM}$ and G_{CM}) the matching of the bias current (I_{bias1} and I_{bias2}) does not affect because the bias current does not depend on the input voltage of the differential pair. Thus, bias current matching is a constant term and it affects to the offset but not to the gain. In these cases it is only needed to consider the output impedance $Z_{olb}(s)$ of the current source. As in the preamplifier case, full bias circuit must be included in the analysis of power supply rejection. Figure 5-33 shows the band-gap current source.

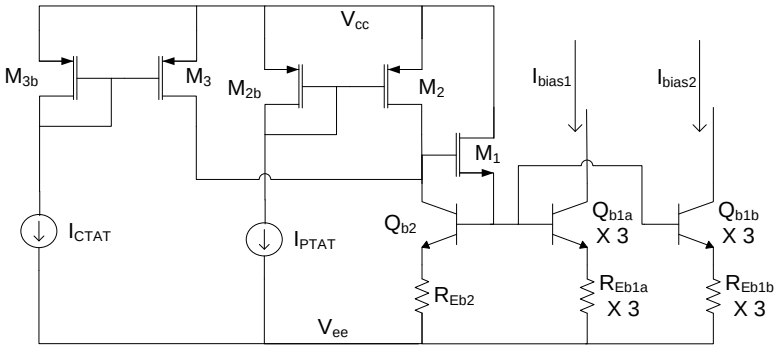

Figure 5-33. Band-Gap current source.

Each current source (I_{bias1} and I_{bias2}) is composed by three bipolar current mirror units (with emitter degeneration R_{Eb2}) in parallel. It can be shown that $\sigma_{\Delta R_{olb}} / R_{olb} = 1/\sqrt{3}\,\sigma_{\Delta R_{E_{b1}}} / R_{E_{b1}}$. Figure 5-34 shows the common-mode small-signal half circuit for coupling of v_{cc} power supply variation without mismatch generators.

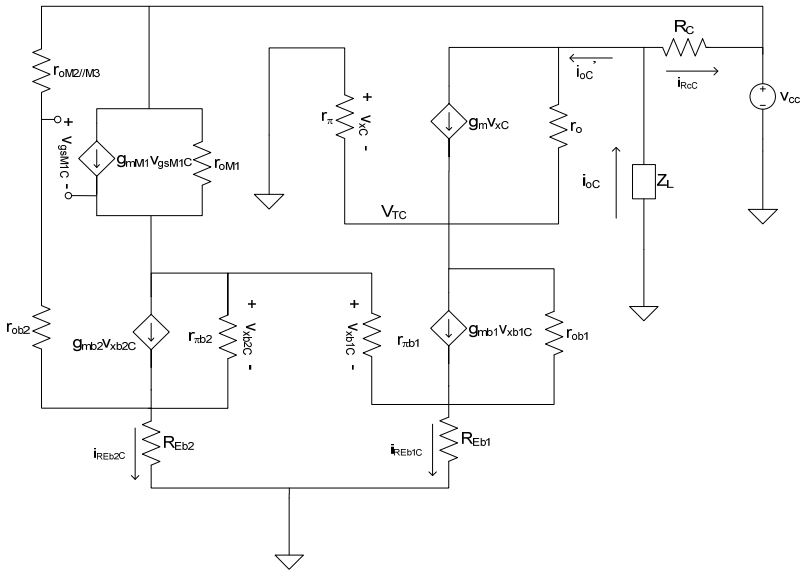

Figure 5-34. CM small-signal half circuit for the analysis of the coupling of v_{cc} variation.

It can be shown [66] that current mirrors with emitter degeneration have to be matched, having $I_{Cb1}R_{Eb1} = I_{Cb2}R_{Eb2}$ and therefore $g_{mb1}R_{Eb1} = g_{mb2}R_{Eb2}$, it can be shown that $v_{xb1C} = v_{xb2C}$. With $g_{mb2}>>1/r_{ob2}$, $g_{mb2}>>1/r_{\pi b2}$, $g_{mb2}>>1/r_{ob2}$, $g_{mb1}>>1/r_{\pi b1}$, $g_{mM1}>>1/r_{oM1}$, $g_m>>1/r_o$ and $g_m>>1/r_\pi$ we obtain,

$$i_{oC} \simeq \left(-\frac{1}{R_C + Z_L} + \frac{R_C}{R_C + Z_L}\frac{g_{mb1}}{g_{mb2}}\frac{1}{r_{oM2//M3}} \right) v_{cc} \qquad (5.185)$$

First term of (5.185) is i_{RCC} and dominates the second (i_{oC}'). In this analysis the i_{oC}' current is considered to be dependent only on v_{cc} coupling through bias generator.

Figure 5-35 shows differential-mode half circuit. The base of Q_b transistors is a virtual AC ground. Signals controlling mismatch generators in differential-mode half circuit in Figure 5-35 are v_{xC}, v_{xb1C}, i_{REb1C} and i_{RcC}. We find approximations to these quantities v_{xC}, v_{xb1C}, i_{REb1C} and i_{RcC}, using the simplified common-mode half circuit without mismatch generators,

$$\begin{aligned} i_{RcC} &= -\frac{v_{cc}}{R_C + Z_L} \qquad v_{xC} \simeq v_{xb1C} \simeq \frac{v_{cc}}{g_{mb2}\, r_{oM2//M3}} \\ i_{REb1C} &\simeq i'_{oC} \simeq G'_{+CM} v_{cc} \qquad with \quad G'_{+CM} = \frac{g_{mb1}}{g_{mb2}}\frac{1}{r_{oM2//M3}} \end{aligned} \qquad (5.186)$$

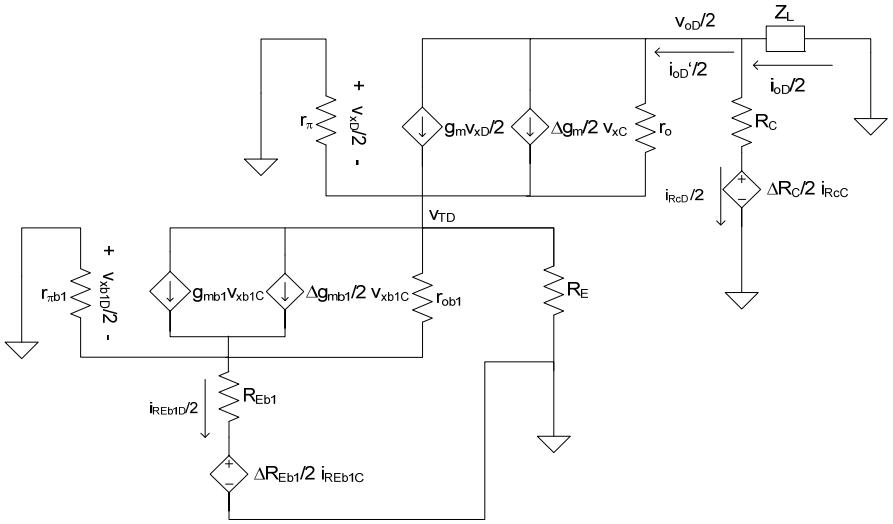

Figure 5-35. Differential-mode half circuit

Analyzing circuit in Figure 5-35 with $g_{mb1}>>1/r_{ob1}$, $g_{mb1}>>1/r_{\pi b1}$, $g_m>>1/r_o$, $g_m>>1/r_\pi$ and $g_m>>R_E$ we obtain,

$$\begin{aligned} \frac{i_{oD}}{2} = \frac{R_C}{R_C + Z_L}\Bigg(& \frac{1}{1+g_m R_E}\frac{\Delta g_m}{2} v_{xC} + \frac{1}{1+g_{mb1}R_{Eb1}}\frac{\Delta g_{mb1}}{2} v_{xb1C} + \\ & + \frac{g_{mb1}}{1+g_{mb1}R_{Eb1}}\frac{\Delta R_{Eb1}}{2} i_{REb1C} \Bigg) - \frac{1}{R_C + Z_L}\frac{\Delta R_C}{2} i_{RcC} \end{aligned} \qquad (5.187)$$

and using v_{xC} for v_{xC}, v_{xb1C} for v_{xb1C}, i_{REb1C} for i_{REb1C} and i_{RcC} for i_{RcC} in (5.187),

$$\begin{aligned} \frac{i_{oD}}{2} = \frac{R_C}{R_C + Z_L}\Bigg(& \frac{1}{1+g_m R_E}\frac{\Delta g_m}{2} + \frac{1}{1+g_{mb1}R_{Eb1}}\frac{\Delta g_{mb1}}{2} + \\ & + \frac{g_{mb1}}{1+g_{mb1}R_{Eb1}}\frac{\Delta R_{Eb1}}{2} g_{mb1} \Bigg) \frac{v_{cc}}{g_{mb2}\, r_{oM2//M3}} + \frac{1}{\left(R_C + Z_L\right)^2}\frac{\Delta R_C}{2} v_{cc} \end{aligned} \qquad (5.188)$$

Then, the positive power supply gains to differential-mode (G_{+DM}) and common-mode (G_{+CM}) outputs are,

$$G_{+DM} \simeq \frac{R_C}{R_C + Z_L}\left(\frac{\Delta g_m}{1+g_m R_E} + \frac{\Delta g_{mb1}}{1+g_{mb1}R_{Eb1}} + \frac{\Delta R_{Eb1}\left(g_{mb1}\right)^2}{1+g_{mb1}R_{Eb1}}\right)\frac{G'_{+CM}}{g_{mb1}} + \frac{\Delta R_C}{\left(R_C+Z_L\right)^2}$$
$$G_{+CM} \simeq -\frac{1}{R_C+Z_L} + \frac{R_C}{R_C+Z_L}G'_{+CM} \qquad (5.189)$$

The coupling to the common-mode output G_{+CM} has a systematic component that depends only on mean device parameter whereas the coupling to differential outputs G_{+DM} depends also on device matching and the mean value is zero (mean PSRR tends to ∞). As local matching variations usually follow a Gaussian distribution[x], a good parameter to estimate the typical PSRR of the circuit (and the yield) is the standard deviation of power supply transfer function σ_{G+DM}. Considering matching between transistors Q_1-Q_2, Q_{b1a}-Q_{b2b} and resistors R_{Eb1}-R_{Eb2}, R_{C1}-R_{C2} is not correlated,

$$\sigma_{G_{+DM}} \simeq \Big|_{\substack{Z_L \ll R_C \\ g_m R_E \gg 1}} \sqrt{\left(\frac{\sigma_{\Delta g_m}}{g_m}\frac{G'_{+CM}}{R_E g_{mb1}}\right)^2 + \left(\frac{\sigma_{\Delta g_{mb1}}}{g_{mb1}}\frac{G'_{+CM}}{R_{Eb1}g_{mb1}}\right)^2 + \left(\frac{\sigma_{\Delta R_{Eb1}}}{R_{Eb1}}G'_{+CM}\right)^2 + \left(\frac{1}{R_C}\frac{\sigma_{\Delta R_C}}{R_C}\right)^2} \qquad (5.190)$$

From (5.190), and with typical component values, it is clear that matching on collector resistor will determine the $PSRR^+$.

The common-mode half circuit for the variations of the negative power supply is shown in Figure 5-36. For a transconductance amplifier the output impedance must be much lower than the load impedance, thus $Z_L << R_C$ and R_C can be neglected in the following analysis.

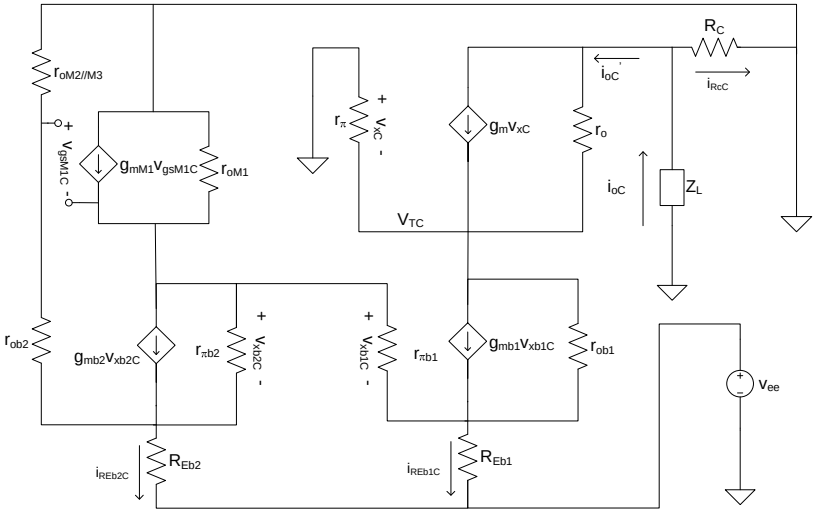

Figure 5-36. CM small-signal half circuit for the analysis of the coupling of v_{ee} variation.

Extrapolation of analysis of circuit of common-mode v_{cc} coupling (Figure 5-34) to the one of common-mode v_{ee} variations (Figure 5-36) is straightforward. We do obtain,

$$G_{-CM} \simeq -\frac{R_C}{R_C+Z_L}G'_{-CM} \qquad with\ G'_{-CM} = \frac{g_{mb1}}{g_{mb2}}\frac{1}{r_{oM2//M3}} \qquad (5.191)$$

Since there-are no differential-mode input signals, apart from mismatch generators, the differential-mode half circuit for vee is exactly the same than for v_{cc} variations (Figure 5-35). In this case the signals controlling mismatch generators in differential-half circuit (v_{xC}, v_{xb1C}, i_{REb1C} and I_{RcC}) have to

[x] The total mismatch of a parameter is caused by many separate events of the mismatch process and the sum of many independently distributed stochastic variables will tend towards a Gaussian distribution.

be determined using circuit of Figure 5-36. We find the approximations using the common-mode circuit without mismatch

$$v_{xC} \simeq v_{xbC} \simeq -\frac{G'_{-CM}}{g_{mb1}} v_{ee} \qquad i_{RcbC} \simeq i'_{oC} \simeq -G'_{-CM} v_{ee} \tag{5.192}$$

Then, the negative power supply differential mode gain G_{-DM} is

$$G_{-DM} \simeq -\frac{R_C}{R_C + Z_L}\left(\frac{\Delta g_m}{1+g_m R_E} + \frac{\Delta g_{mb1}}{1+g_{mb1}R_{Eb1}} + \frac{\Delta R_{Eb1}\left(g_{mb1}\right)^2}{1+g_{mb1}R_{Eb1}}\right)\frac{G'_{+CM}}{g_{mb1}} \tag{5.193}$$

And the standard deviation of G_{-DM}

$$\sigma_{G_{-DM}} \simeq \Big|_{\substack{Z_L \ll R_C \\ g_m R_E \gg 1}} \sqrt{\left(\frac{\sigma_{\Delta g_m}}{g_m}\frac{G'_{-CM}}{R_E g_{mb1}}\right)^2 + \left(\frac{\sigma_{\Delta g_{mb1}}}{g_{mb1}}\frac{G'_{-CM}}{R_{Eb1} g_{mb1}}\right)^2 + \left(\frac{\sigma_{\Delta R_{Eb1}}}{R_{Eb1}} G'_{-CM}\right)^2} \tag{5.194}$$

In (5.194) dominant term is matching in emitter resistance of the current mirror (R_{Eb1}). If contribution of biasing circuit were not relevant, G_{-DM} would be exactly G_{CM-DM} since the v_{ee} generator is a common-mode signal applied at point equivalent to a CM input.

Figure 5-37 shows Monte Carlo simulations for positive power supply gain to the differential-mode (G_{+DM}) and common-mode (G_{+CM}) outputs. The non-zero G_{+DM} gain due is due to the finite output resistance of differential pair transistors Q_1-Q_2. G_{+DM} standard deviation is about -165 dB, the low frequency $PSRR^+$ is about 105 dB.

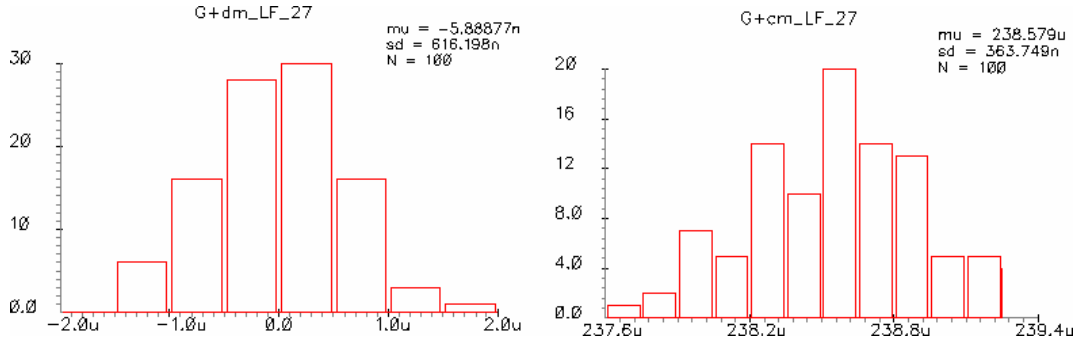

Figure 5-37 DC positive power supply gain to the differential-mode (left) and common-mode (right) outputs.

Figure 5-38 shows the negative power supply gain (low frequency) to the differential-mode (G_{-DM}) and common-mode (G_{-CM}) outputs. G_{-DM} has mean value close to zero as it is due to mismatch the standard deviation fits quite well with first order estimation of (5.193). The G_{-CM} low frequency mean value is also in agreement with (5.191). Since the relevant output is the differential one the mean $PSRR^-$ is infinite whereas the standard deviation of the low frequency $PSRR^-$ is about -89 dB.

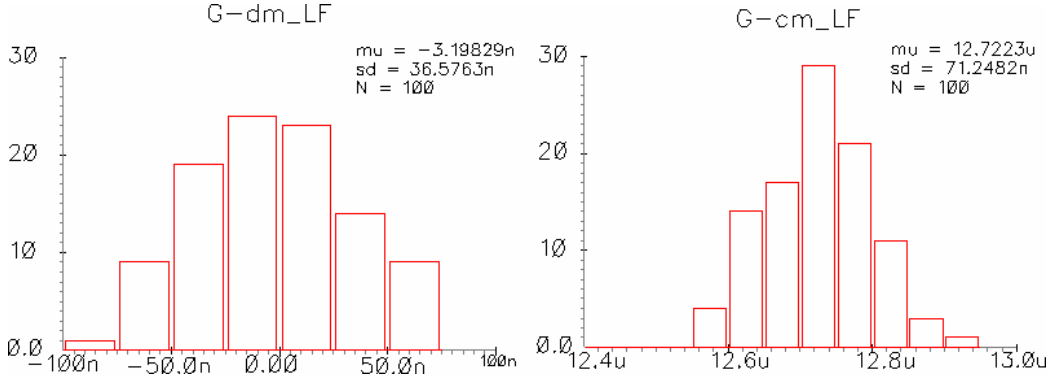

Figure 5-38 DC negative power supply gain to the DM (left) and CM (right) outputs.

Figure 5-39 shows the frequency dependence of power supply gains to differential and common mode outputs.

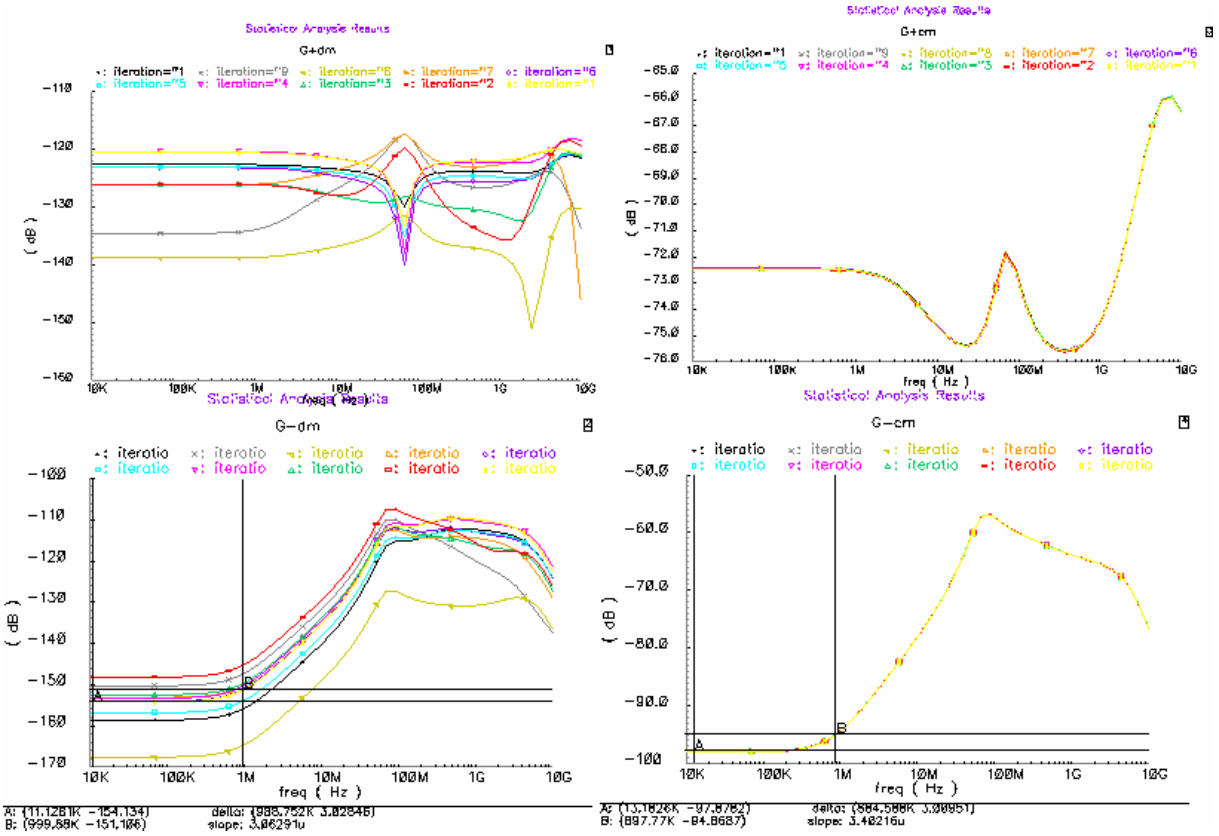

Figure 5-39. Monte Carlo simulations (Mismatch, 10 runs) of the positive power supply gain (top) to the differential-mode (left) and common-mode (right) outputs and of the negative power supply gain (bottom) to the differential-mode (left) and common-mode (right) outputs.

Both, $G_{-CM}(s)$ and $G_{-DM}(s)$ depend on a high impedance node of bias circuitry: the source of MOS transistors M2 and M3 (depend as $1/r_{oM2//M3}$). The source to bulk capacitance at this node C_{sbM23} decreases the impedance, increasing the v_{ee} coupling. If $r_{oM2//M3}$ is replaced by the complex impedance $Z_{oM2//M3}(s) = R_{oM2//M3} \,\|\, (1/sC_{sbM23})$ in (5.191) and (5.193),

$$G_{-CM}(s) \simeq \Big|_{g_{bias}R_{olb} \gg 1} - \frac{R_C}{R_C + Z_L} \frac{g_{mb1}}{g_{mb2}} \frac{1}{r_{oM2//M3}} \left(1 + s r_{oM2//M3} C_{sbM23}\right) \qquad (5.195)$$

$$G_{-DM}(s) \simeq G_{-DM}(0)\left(1 + s r_{oM2//M3} C_{sbM23}\right) \qquad (5.196)$$

$G_{-CM}(s)$ and $G_{-DM}(s)$ have a dominant zero at frequency $1/2\pi\left(r_{oM2//M3} C_{sbM23}\right)$. $G_{+CM}(s)$ and $G_{+DM}(s)$ have an approximately flat frequency response for resistive and capacitive charges in a range of hundreds of MHz. Dominating term is $1/ R_C$ and impedance Z_C is constant up to few GHz, because the only parasitic capacitances affecting Z_C are the interconnection capacitances, with values around tens of fF. However at a few tens of MHz the effect of v_{ee} coupling on bias circuitry becomes visible in G_{+CM}, nevertheless the effect is below 3dB (40 %). Figure 5-40 shows how i_{oC}' current increases when $Z_{oM2//M3}$ starts to decrease, as $G_{-CM}(s)$ does. At about 100 MHz other poles influence on i_{oC}' phase and magnitude.

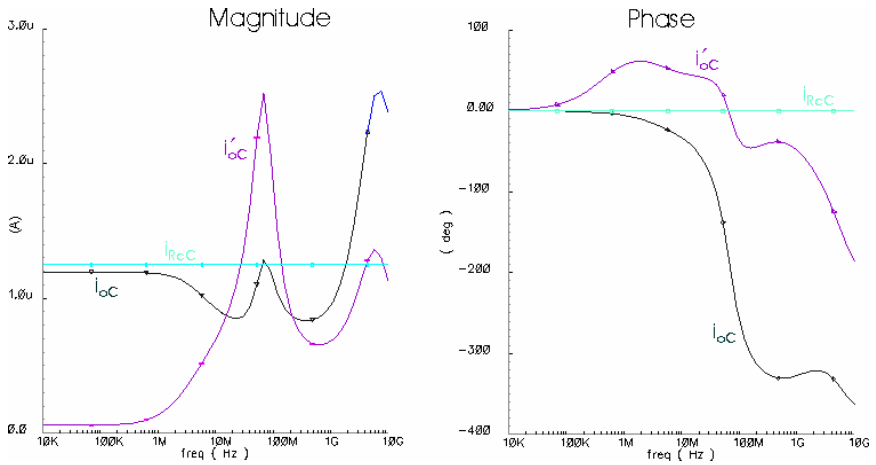

Figure 5-40. Magnitude (left) and phase (right) of currents at the collector node (CM half circuit).

A detailed comparison between calculations and Monte Carlo simulations is given in Table 5-3.

	Hand Calculation		Monte Carlo	
	Low Freq. [dB]	f-3dB [MHz]	Low Freq. [dB]	f-3dB [MHz]
G_{+DM}	- 126 r.m.s.	Flat**	- 126 r.m.s.	Flat**
G_{+CM}	- 72	Flat**	- 72	Flat**
G_{-DM}	- 150 r.m.s.	1*	- 149 r.m.s.	1*
G_{-CM}	- 99	1	- 98	1
***PSRR*$^{+}$**	**65 r.m.s.**	**Flat****	**65 r.m.s.**	**Flat****
***PSRR*$^{-}$**	**89 r.m.s.**	**1 (pole)**	**88 r.m.s.**	**1 (pole)**

Table 5-3. Hand calculation and simulation results of power supply gains with $Z_L << R_C$.

5.4 Conclusions

The absolute resolution or precision of the system is given by the random noise. The predicted noise of the system is 2.3 mV r.m.s, and for a total gain of 1.2 mV/fC (see section 4.2.2.3), it represents an ENC of about 2 fC at the input, as required in section 3.3.1. Of course it represents the minimal amount of the statistical fluctuation on the measurement, any additional source of error (interferences, drifts, etc) will degrade further the accuracy of the system. On that sense the PSRR gives encouraging results, because low frequency PSRR of sensitive input analog blocks is between 65 and 90 dB rms. Although some PSRR transfer functions present a pole at 1 MHz, the minimal PSRR in the system bandwidth is about 60 dB r.m.s; this means that a 1 V fluctuation in the power supply voltage would be translated into a 1 mV effect at the output of the circuit in the worst case. Hence, the circuit can be considered robust against power supply variations by design.

As said before, the threshold resolution of the system is given by the number of bits of the channel DAC and its full scale voltage, which has to be large enough to cover the offset spread among the 8 channels of a chip. Using expression (5.1) and results of section 5.2, we find that the absolute threshold resolution will be about 3 mV. The resolution referred to the input is 2.5 fC, and between 0.025 MIP for 100fC/MIP and 0.075 MIP for 30 fC/MIP. As the random noise is below the threshold resolution of the system, the 6 bits of the DAC are useful to set the magnitude; "available" resolution of the system is 6 bits.

The resolution and the accuracy of the system are interrelated parameters, to be meaningful they must related to the input of the system (or at least to the same point) and then, both became dependent of set of variables: system gain, electronic noise and offset. The solution presented here is the result of a trade-off and of the design and measurement of three iterations of the chip.

6 Test results

In this chapter we will present test results and laboratory measurements both of relevant analogue blocks and of the full system, the ASD channel including digital interface and control logic. When designing full custom blocks it is important to characterize each block to be able to understand the behavior of the full system and to validate the models and the results of the simulations. It is important to take into account that the models provided by the manufacturer are not completely reliable. Even if the models were fully correct, the conditions set in the simulator test bench may differ from experimental conditions and the interpretation of the results of the simulation may be biased.

For the channel measurements both electrical and optical (using MaPMT as transducer) input signals have been used. Important parameters for the system characterization are:

- Offset. It is needed to set the thresholds of each channel and to control that the resolution of the system is inside specifications (see chapter 4).
- Noise. Obviously, it determines the SNR and the minimal resolution achievable.
- Gain. The mean value of the gain is needed to calibrate, and its dispersion must be small enough.
- Linearity. Linearity error must be smaller than the one related to the MaPMT.
- Crosstalk. Electrical crosstalk must be smaller than optical crosstalk.

The influence of temperature variations have tested on sensible parameters. Burn in cycles have been performed on chip production to filter out chips that would suffer from infant mortality [175]. All the block measurements are performed in laboratory conditions whereas system measurements have been obtained also using particle beams at test areas of the SPS accelerator at CERN.

It is also worth to mention that dedicated radiation damage tests have been performed and that the chip has been qualified by the LHCb collaboration to operate in the expected radiation conditions of the experiment. We will present also a brief summary on this point.

6.1 Results related to individual blocs measurement

Some key building blocks have been tested individually to validate the performance and results of the simulation. In cases where speed is critical an output buffer consisting on a large area emitter follower has been used to drive the output pads, as depicted in Figure 6-1.

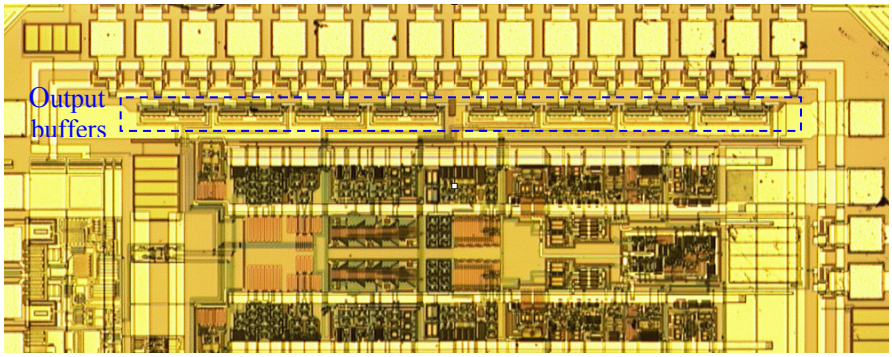

Figure 6-1. Microphotograph of a prototype with output buffers connected to output pads (top).

Differential signals have been measured using the differential probe P6146 of 1 GHz bandwidth and the digital storage oscilloscope TDS3034 of 300 MHz bandwidth and 4 GS/s, both from Tektronix. Input signals, clocks and other controlling signal have been generated through the arbitrary waveform generator AWG2021 from Tektronix, whose maximum clock frequency is 250 MHz. In Figure 6-2 we appreciate a test card designed for testing the chips including building blocks of the channels, with a differential probe and some other multimeter probes.

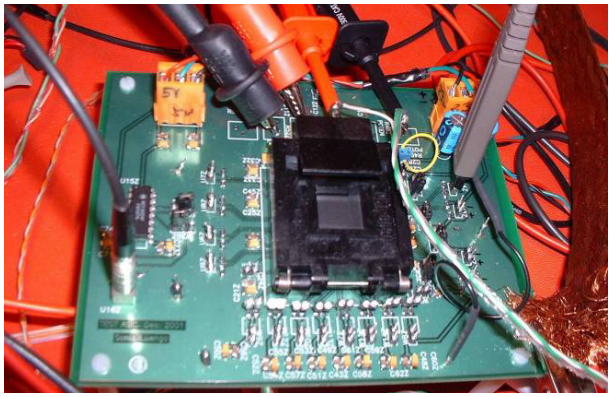

Figure 6-2. Photograph of a test card for a block chip.

6.1.1 Preamplifier

The offset of the preamplifier has been measured in 10 samples, showing a mean value of 0.7 mV ± 1.5 mV and standard deviation of 5 mV r.m.s ± 1.2 mV. Standard deviation is compatible with Monte Carlo simulation within statiscal errors, whereas mean value is not. Emitter followers acting as output followers are large devices without common centroid layout to improve matching. Gradients in parameter variation are probably the reason of this disagreement. As we will see later, measurments on the full channel agree with calaculations and simulations of the offset of the preamplifier. The gain is 4.35 whereas according to calculations and simulations it should be around 4.6. The measured bandwidth is about 100 MHz. Gain and bandwidth measurements are affected by the buffer, whose bandwidth is limited to prevent oscillations. Relative tolerance in the gain (std. deviation/mean) is about 0.9%. Figure 6-3 shows the response of the preamplifier to a 10 kHz sinusoidal DM input signal. Saturation starts to be evident for V_{oD}>500mV.

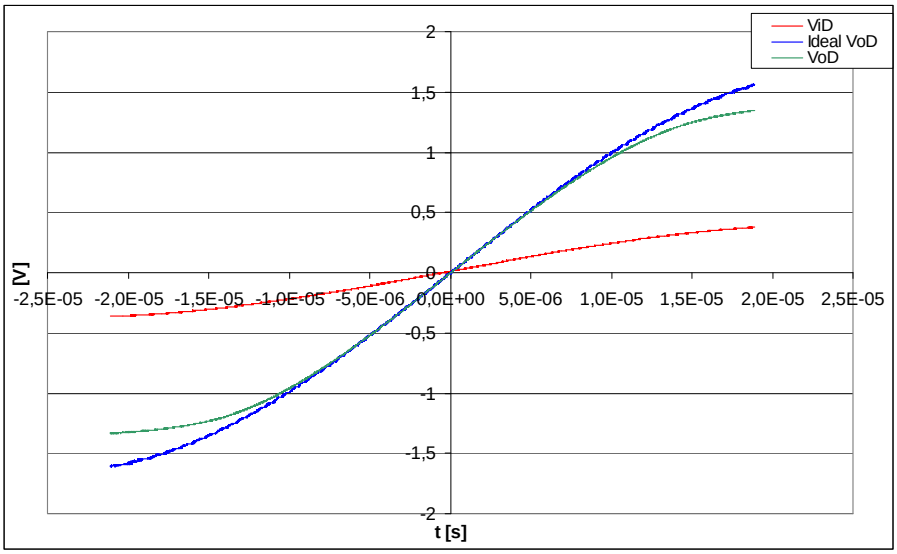

Figure 6-3. Response of the preamplifier. ViD is the DM input signal, VoD the DM output and ideal VoD the ideal response of the preamplifier A·ViD.

A detail of the linearity error is illustrated in Figure 6-4. The modulus of the linearity error is <2 mV for a range of ±300 mV in VoD. i.e., linearity error is <1%.

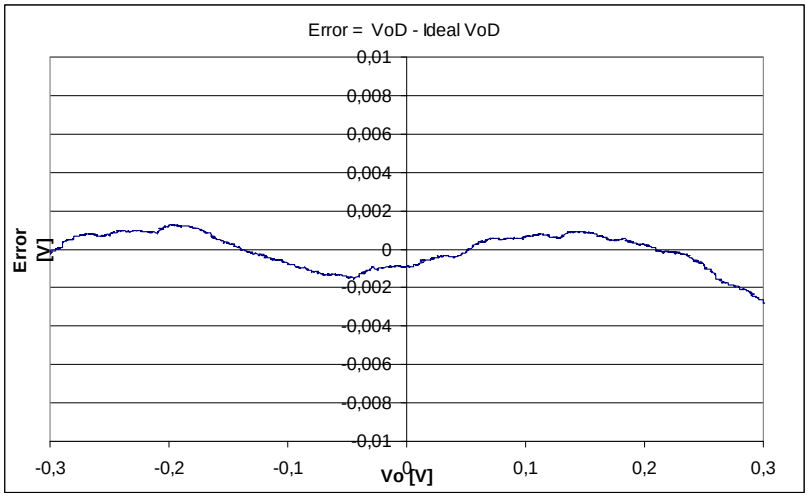

Figure 6-4. Linearity error as a function of DM output.

The temperature coefficient of the gain is about -100 ppm/K for a measurement range of 300 K to 360 K. The variation of the input referred offset with temperature is $\Delta V_{OSP}/\Delta T=5\ \mu V/K$. However, the gain variations are so small that the uncertainty in the measurement of the gain TC is quite high.

For the measurements of the dependence of the different blocks with the temperature a heater and an on-chip temperature probes have been integrated in a block prototyping chip. The heater is a poly resistor of about 70Ω. The temperature sensors are a modified version of the band gap current source. According to analysis and simulations the dependence of the sensor output voltage with temperature should be:

$$T_{SENSOR}[K] = \left(V_{SENSOR}[mV] \cdot -0.447 \frac{K}{mV} \right) + 381.45^{o}C \qquad (6.1)$$

As the foundry provides the TC of the poly resistors ($TC_R = 0.95 \cdot 10^{-3}$ %/K) the measurement of the heater resistance can be used to calibrate the temperature sensor. Figure 6-5 shows the temperature resulting of measuring the output voltage of the sensor and the resistance of the heater. Difference is always smaller than 3 K.

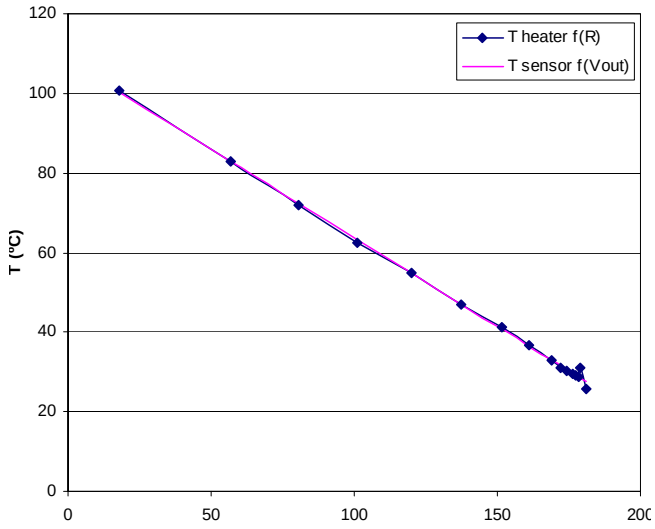

Figure 6-5. Calibration of the on-chip temperature sensor.

6.1.2 Integrator

The measurements of the integrator have been performed on a block that has a gain 1.42 times higher than the final one. Measurements affected by the gain are corrected according to this factor. In Figure 6-6 we can appreciate the output of the integrator for a typical input pulse. When the clock is at low level the integrator is in active mode and when the clock is high the integrator capacitors are discharged. Worst case (maximum signal) reset time is lower than 12 ns. As the input signal has a long decay time, a part of tail of the signal is integrated after reset.

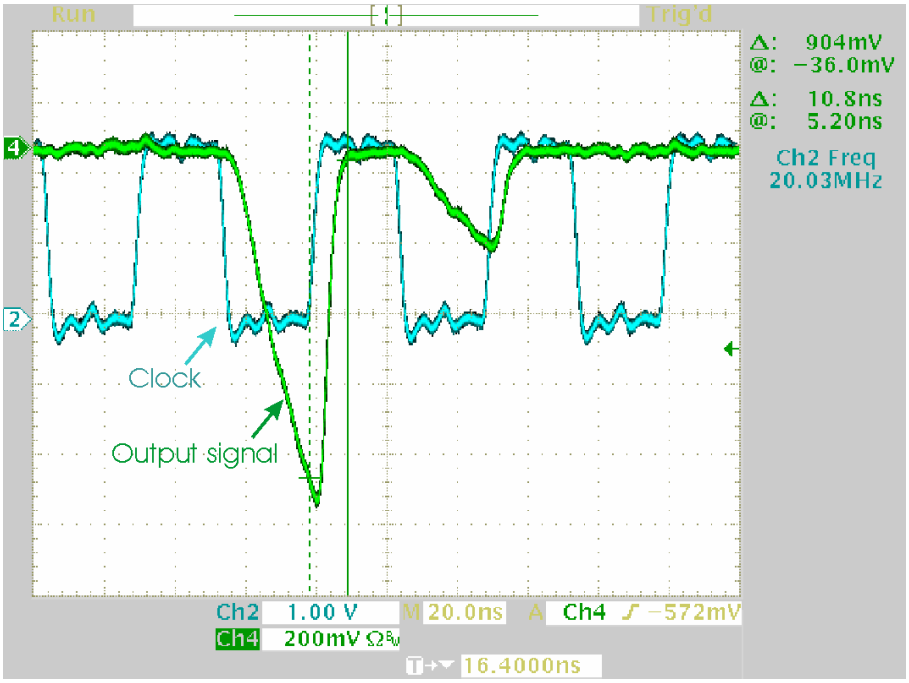

Figure 6-6. Integrator's output signal and control clock for switches.

The mean offset of the integrator measured in 10 samples is -19 ± 4.6 mV and the standard deviation 16 ± 4 mV r.m.s. Standard deviation is compatible with Monte Carlo simulation within statiscal errors, whereas mean value is not. Results of Monte Carlo post-layout simulations including parasitic capacitances and resistances do not show any evidence of such systematic offset component. There are two possible reasons that could explain this effect:

- The pad corresponding to the V_{iH} input of the integrator is adjacent to the controlling signal of the integrator "int", a controlling clock for nMOS switches. Assuming a capacitance of 500fF due to the packaging a capacitive coupling of the falling edge of the "int" signal to the V_{iH} might introduce a pulse at the input that would be integrated. This effect would be only related to the blocks test chip, and will not be present in the channel.
- As said in section 4.2.2.6.2, the nMOS and the pMOS transistors have the same size to introduce the same parasitic capacitance and are driven by two complementary clocks one working between 0 and -1.65 V for pMOS transistors and the other between 0 and +1.65 V for nMOS transistors. The feedthrough caused by the rising edge of the nMOS clock tends to cancel out with the feedthrough caused by the simultaneous falling edge of the pMOS clock. The clock circuitry has been adjusted through post-layout simulations to have both controlling signals are in phase. If any parasitic effect is not precisely modelled in post-layout simulations, either a delay between the edge of both clocks either a different coupling for nMOS and pMOS switches may happen. Then some charge will be injected in the feedback capacitors of the integrator.

There are evidences indicating that the systematic noise is present in the full ASD chain, as we will see. Nevertheless, a systematic coupling of the clock will increase the offset but not the noise. As the maximum effect is -20 mV, it is not a source of degradation the performance of the signal processing, as studied in chapter 5.

In Figure 6-7 it is shown the DM output of the integrator (10 samples) at the end of the integration period for different input signals (charge). If the curves are considered linear, the slope can be defined as the charge gain of the integrator G_Q. The mean charge gain is 0.02541 mV/fC with a tolerance (std. deviation/mean) of the 2.4 %.

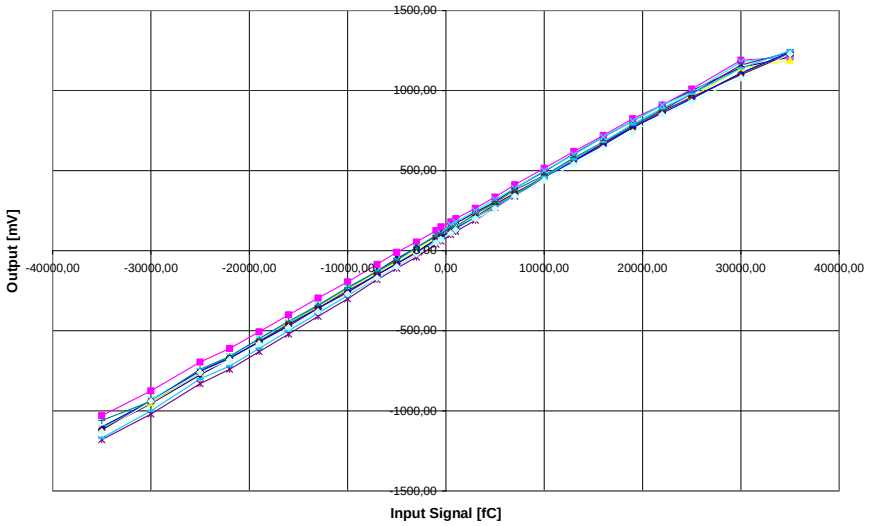

Figure 6-7. DM output of the integrator (10 circuits) as a function of the charge of the input pulse.

In section 4.2.2.3 the charge gain of the integrator was studied. Without preamplifier,

$$G_Q \equiv \frac{v_{oD}\left(t=T_m\right)}{-Q_{MIP}} \simeq \omega_i' R_{PMT}\left(1-e^{-\frac{T_m}{\tau}}\right)_{T_m=25ns} \qquad (6.2)$$

If G_Q=*0.02541* mV/fC and with R_{PMT}=50 Ω, then ω_i=560 Mrad/s and τ_i=*1.*6 ns as expected.

The linearity error is below 1% in the range of ±500 mV in VoD, see Figure 6-8. An additional factor in measurement error is clock jitter in signal versus clock of the generator. When |VoD|>1V the saturation is visible.

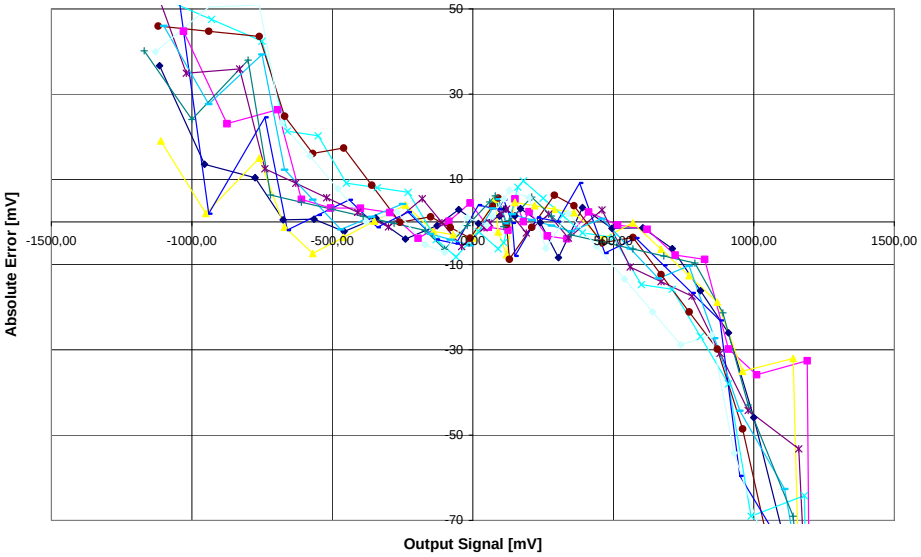

Figure 6-8. Linearity error of the integrator.

The temperature coefficient of the integrator gain is about -200 ppm/K a measurement range of 300 K to 360 K. However, the gain variations are so small that the uncertainty in the measurement of the TC of the gain is quite high.

6.1.3 Fully differential operational amplifier

In Table 6-1 we appreciate the input referred offsets and bias current measured for 10 circuit samples.

	V_{io} [mV]	I_{bias} [uA]	I_{io} [nA]
Mean	0.43	-0.951	23.34
Standard dev.	4.815	0.054	53.01

Table 6-1. Input referred offsets and bias current.

The magnitude and the phase of the frequency response of the FDOA are shown in Figure 1-1, closed loop gain is 220 and GBW is 130 MHz. According to simulations (post-layout: chip and block without parasitics) it must be about 160 MHz. If we add in simulation a 500 fF capacitor between adjacent pins (V_{iL}-V_{iH}, V_{oL}-V_{oH} i V_{iH}-V_{oL}) of FDOA then GBW is compatible with measurements. Response for frequencies beyond 100 MHz is not clearly corresponding to what is expected from simulations. However at high frequency, parasitic capacitances and inductances of the chip and of the measurement set-up start to be relevant and many transmission line effects may distort the measurements. Taking into account that results are in good agreement for the required bandwidth, no additional effot has been devoted to improve the measurement set-up for high frequency. The CMRR of the FDOA is a bout 70 dB at DC.

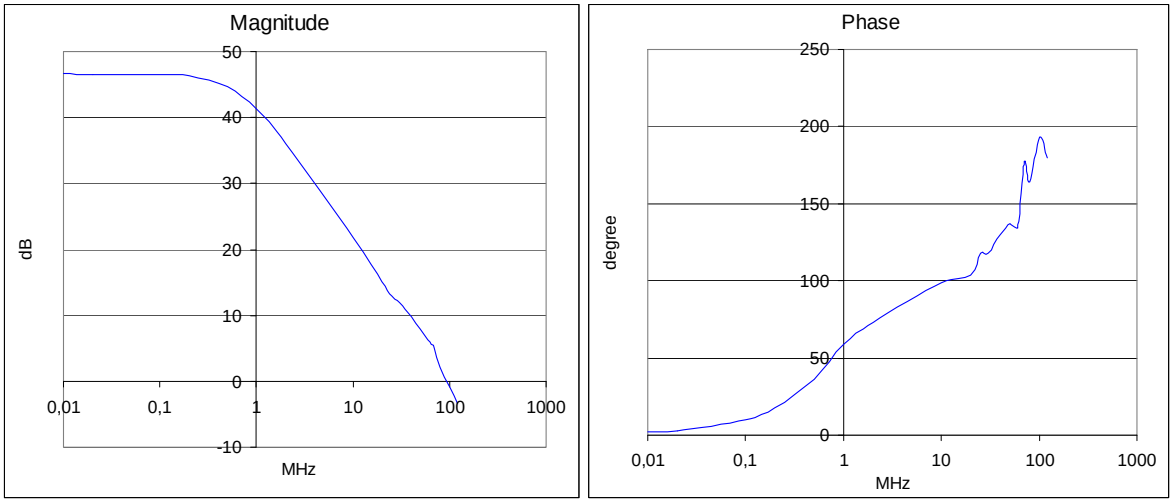

Figure 6-9. Magnitude (left) and phase (right) of the frequency response of the FDOA.

The response of the FDOA in unity gain configuration to a square waveform of 2.5 MHz is shown in Figure 6-10. FDOA is in linear operation. Fall and rise time (from 10% to 90%) are about 6 ns, which is consistent to a settling time to the 1% of 9 ns as predicted from calculations and simulations. The relatively high overshoot is probably related to excess in load capacitance introduce by the input capacitance of the large transistors of the output follower.

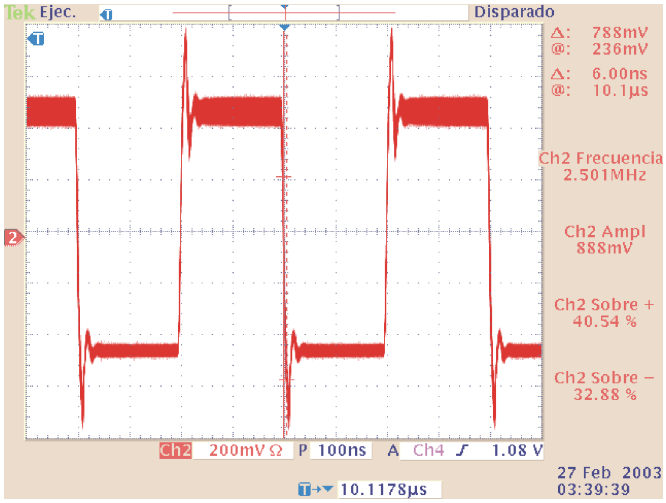

Figure 6-10. Response of the FDOA in unity gain configuration to a square waveform (2.5 MHz).

If we increase the frequency to 20 MHz (Figure 6-11) non-linear effects are evident, slew rate is about 160 V/µs, close to the simulation result 170 V/µs.

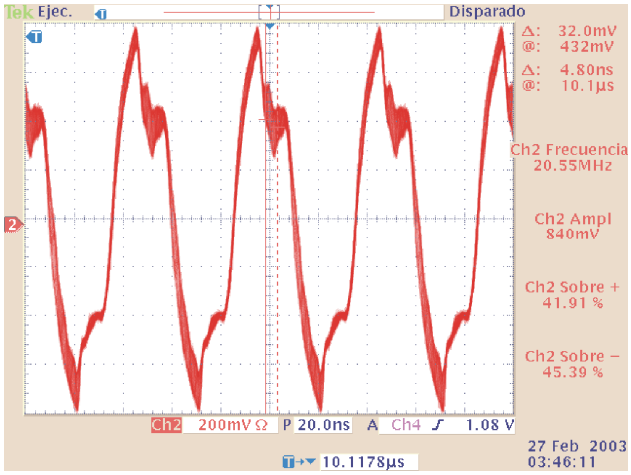

Figure 6-11. Response of the FDOA in unity gain configuration to a square waveform (20.5 MHz).

In Figure 6-12 the CM at the output (V_{oC}) as a function of the CM reference is shown. V_{oC} is measured after output buffer (emitter follower): output of FDOA is about 0.8V higher. The V_{oC} upper limit to avoid distortion on V_{oD} is V_{oC} <450mV (for a V_{oD} of 300mVpp). The V_{oC} is lower limit is V_{oC}>-0.7V, there is no distortion on V_{oD} but V_{oC} does not follow VCMref.

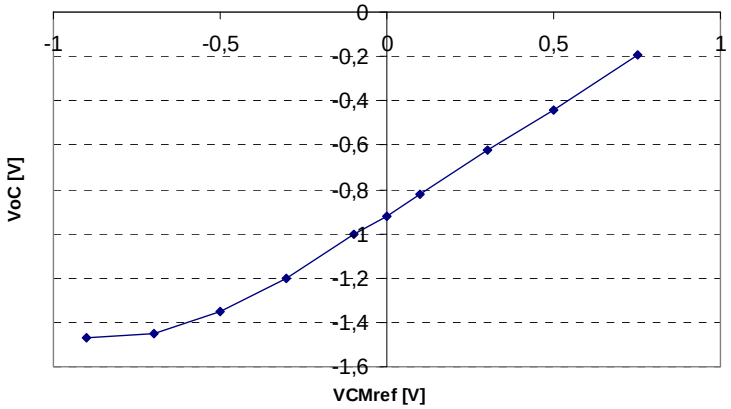

Figure 6-12. CM at the output (V_{oC}) as a function of the CM reference (VCMref).

The DM output range is ±1.35 V with V_{oC}=0 (Figure 6-13).

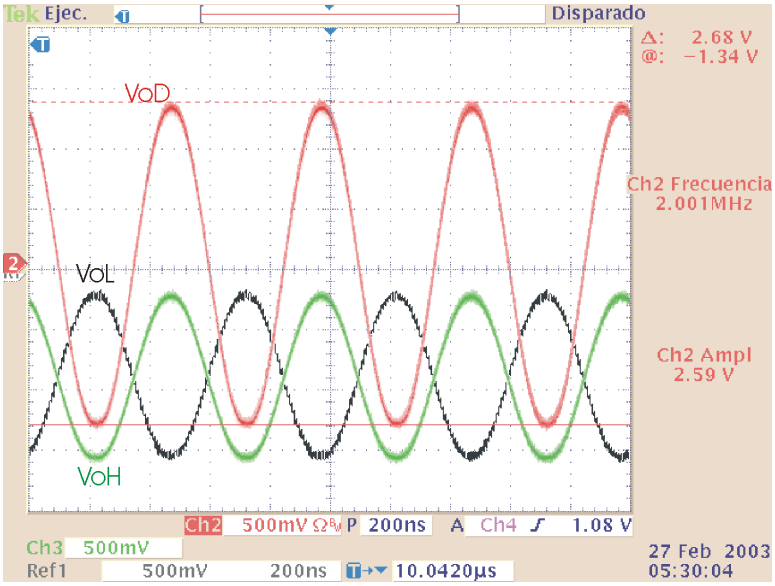

Figure 6-13. DM and CM outputs for V_{oC}=0.

6.1.4 Track and hold

In order to measure the AWG 2021 has been used to generate a synchronous clock and input signal. A differential probe has been used to measure differential output voltage of the track and hold. In Table 6-2 we appreciate OZE of the track and hold in track mode measured for 10 circuit samples.

V_{biasD} [V]	0.45	0.35	0.25	0.15	0.05	-0.05
Mean [mV]	-1.23	-1.33	-1.47	-1.52	-1.50	-1.50
Standard dev. [mV rms]	3.21	3.60	3.89	4.01	4.19	4.27

Table 6-2. OZE of the track and hold in track mode.

And in Table 6-3 the same in hold mode. The assumption that the offset of this block can be neglected on the computation of the offset of the full chain is confirmed.

V_{biasD} [V]	0.45	0.35	0.25	0.15	0.05	-0.05
Mean [mV]	-1.81	-1.90	-2.03	-2.12	-2.15	-2.14
Standard dev. [mV rms]	3.23	3.54	3.65	3.93	4.04	4.29

Table 6-3. OZE of the track and hold in hold mode.

The output signals of the cross coupled gain stage and of the track and hold stage are depicted in Figure 6-14 for 12 MHz sinusoidal input signal and a gain of about 25%. The circuit is controlled by a 40MHz clock.

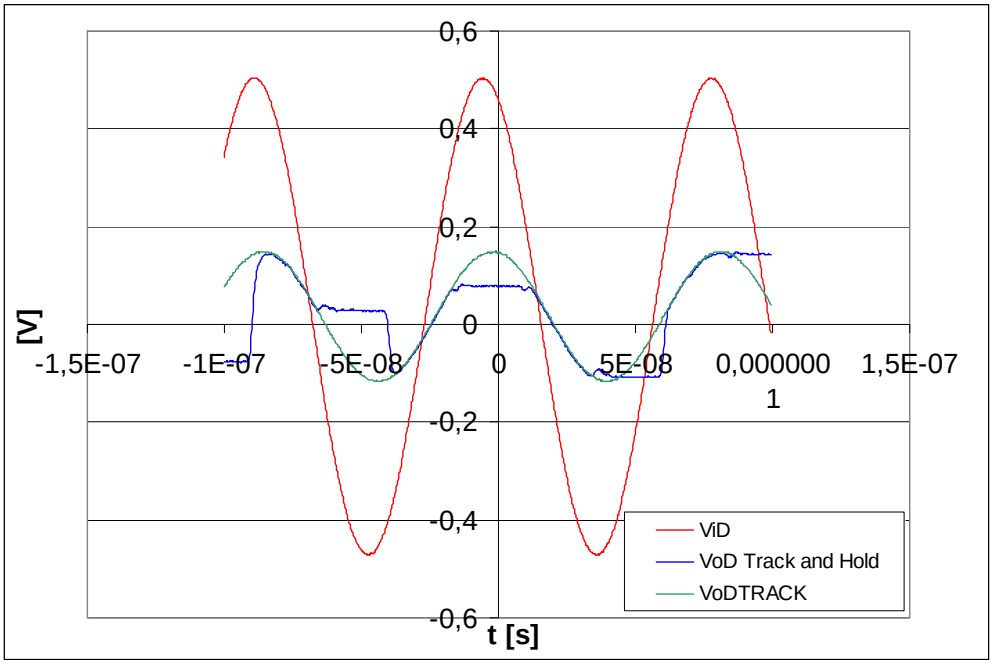

Figure 6-14. Operation of the track and hold circuit.

In Figure 6-15 the gain of the stage for different values of the gain controlling signal V_{biasD} is depicted (10 circuit samples). As analyzed in section 4.2.3 the dependence of the gain with V_{biasD} is linear in the operation range (gain from 0 to 0.3). The dispersion of the gain for different circuits is always better than the 1% (standard deviation). It has been checked that when the circuit changes to the hold mode the dispersion is still below 1%. This result is important because 16 blocks will be controlled by the same signal in an 8 channels chip and, indeed, 128 blocks in a VFE card.

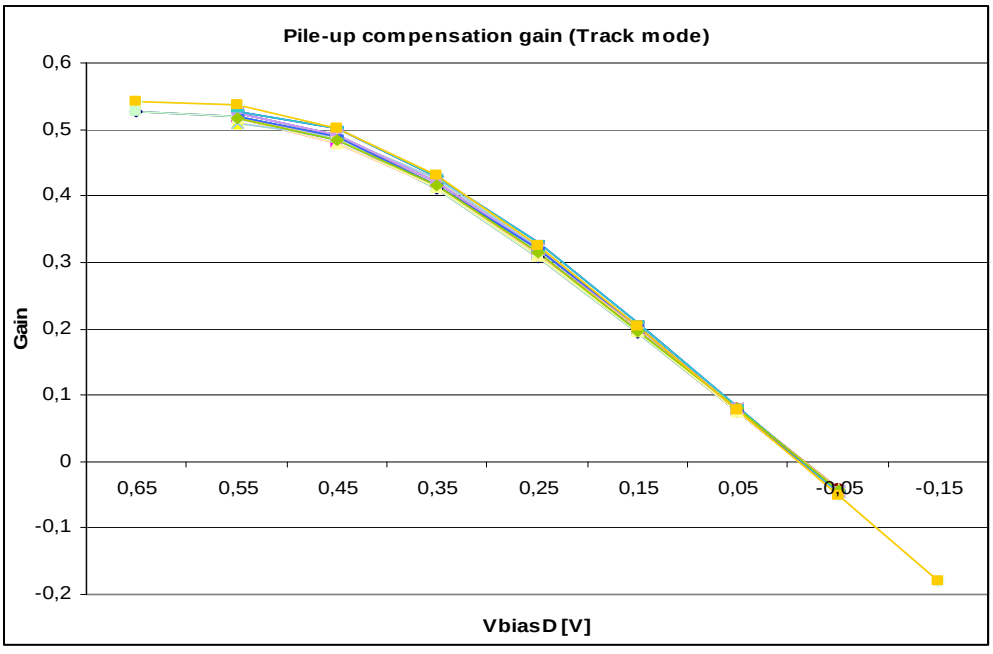

Figure 6-15. Gain in track mode for 10 circuit samples as a function of V_{biasD}.

The linearity error of the circuit is below 5 mV at the ± 500 mV range for any gain value (Figure 6-16). For a typical gain of 0.25 or less the error is below 20 mV for ± 1 V range and for a higher gain below 40 mV.

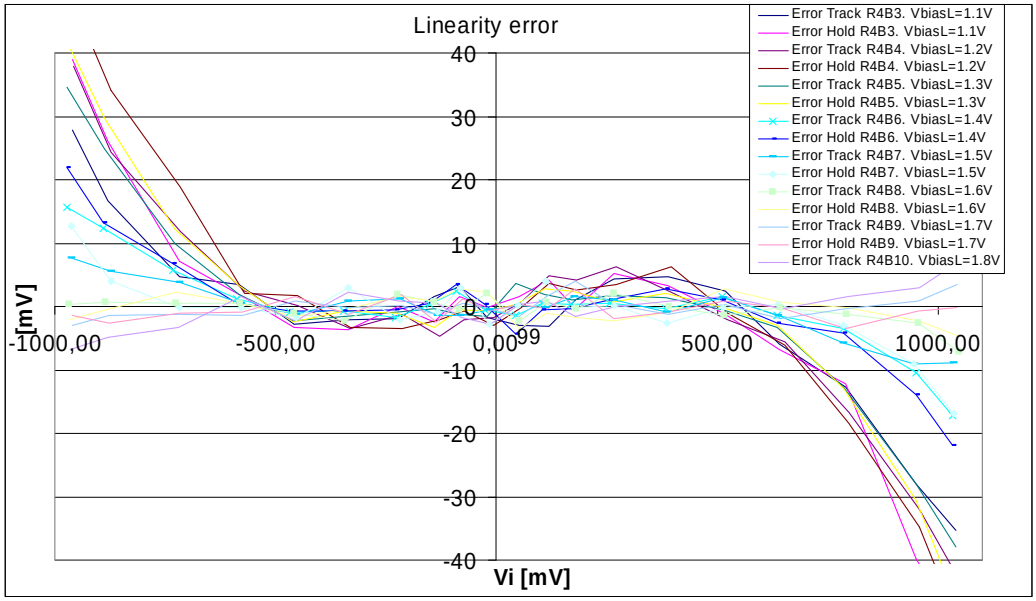

Figure 6-16. Linearity error of the circuit for different gain values.

The frequency response of the stage is depicted in Figure 6-17. The bandwidth is about 100 MHz, below the expected value (170 MHz), as said before, neither the test set-up nor the prototyping chip were prepared for high frequency measuremnts. Anyway, even a bandwidth of 100 MHz is more than sufficient because it is the bandwidth related to the PMT single electron signal, which in addition is integrated.

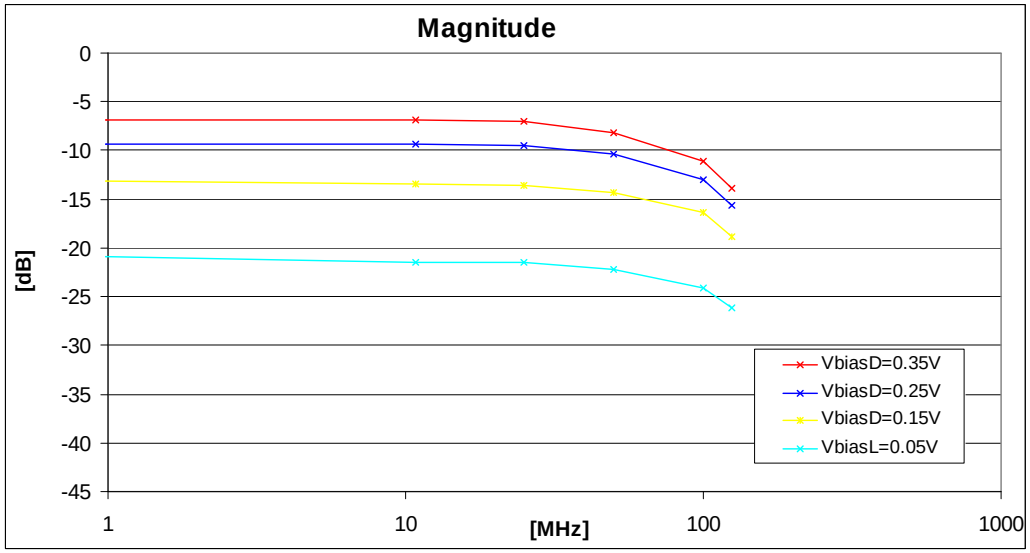

Figure 6-17. Magnitude of the frequency response for different

The measured drop rate is about 0.04 mV/ns, a little bit lower than expected (0.07 mV/ns). The input CM range is 0.55 V< V_{iC}<–0.3 V (for a V_{iD}=±0.7V). The DM input range is about 1 V for V_{iC}=0 as required. The output common mode value is V_{oC}=-1.05 V+V_{BE}≈-0.35 as needed for the open loop addition stage. V_{BE} corresponds to the output buffer, an emitter follower.

As said before, this is the most critical block in terms of temperature sensitivity. Gain dependence on temperature is shown in Figure 6-18. The temperature coefficient of the gain is about -0.29 %/ºC,

higher than what was expected from simulations (-0.15 %/ºC) but good enough for a typical temperature variation of 5 ºC.

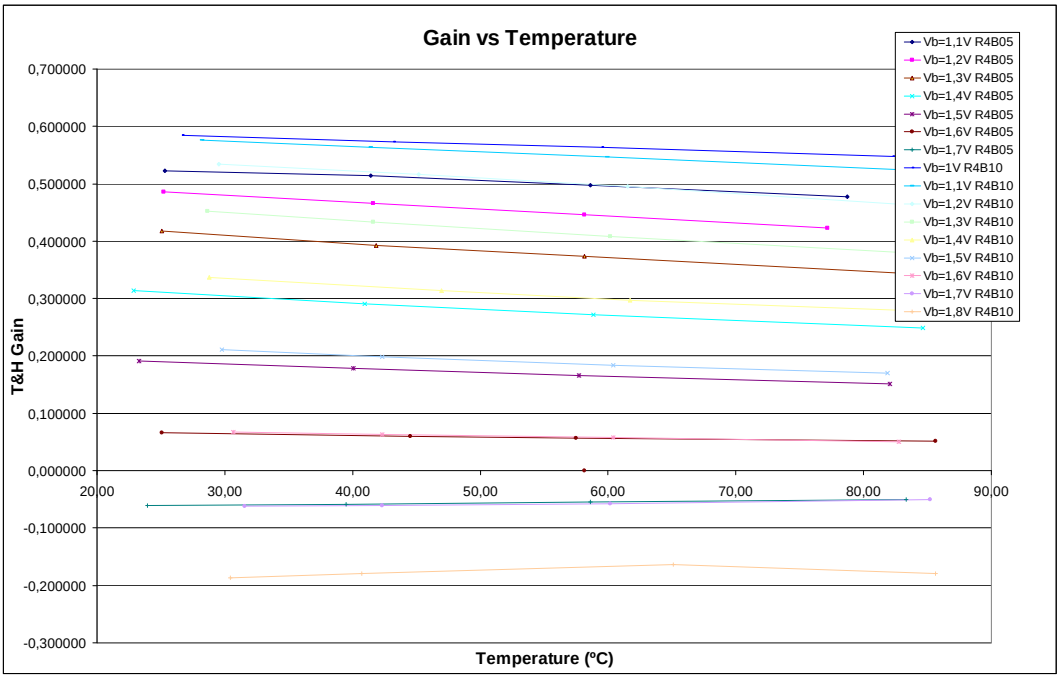

Figure 6-18. Temperature dependence of the gain of the track and hold circuit for different values of VbiasD.

6.1.5 Open loop addition

The offset of the open loop addition has been measured for 10 circuits, showing a mean value of 0.1 mV ± 0.75 mV and standard deviation of 2.5 mV r.m.s ± 0.6 mV.

The DM output corresponding to three fast (2 to 5 MHz) DM input signals is shown in Figure 6-19. The measured output follows quite well the ideal output; main difference is due to phase delay. Mean gain is 0.41 with a standard deviation of 1%.

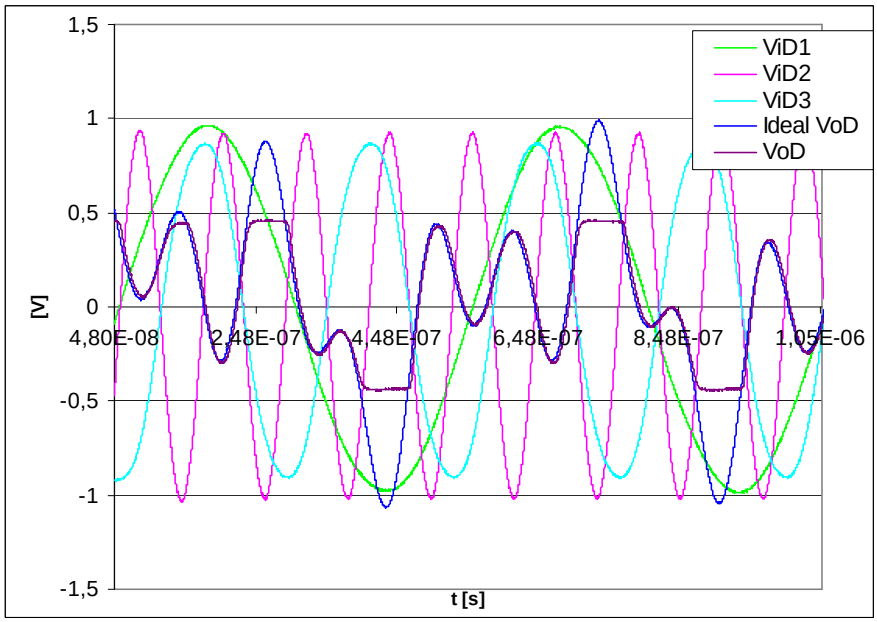

Figure 6-19. High frequency operation of the open loop addition stage.

The linearity error for a slow signal is shown in Figure 6-20, it is below 10 mV for the operation range (± 0.4 V at the output).

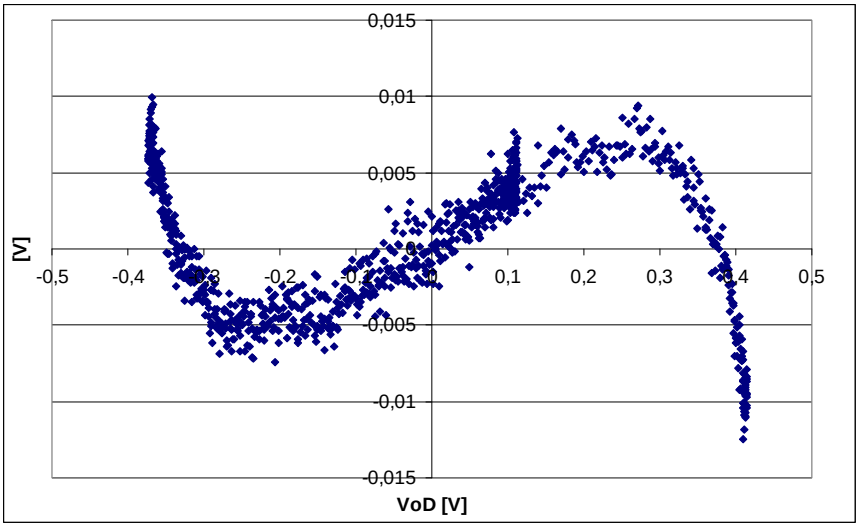

Figure 6-20. Linearity error of the open loop addition stage.

A key point to properly set the operation point of this bloc is the CM value of the input signals, the CM input range it has been checked for different combination of signals their CM has been varied until distortion is visible in the output, conclusion is 0.6 V< V_{iC}<–0.4 V.

6.1.6 Comparator

The static transfer function of the comparator is shown in Figure 6-21. The average DM output in latch state is shown as a function of the DM input signal at DC, as it is affected by the noise which is a random signal the function corresponds to a histogram. The differential of the histogram corresponds to a random signal with quasi-Gaussian shape, its standard deviation corresponds to the noise standard deviation and its mean value to the offset of the stage. Using this method we are able to measure the input referred offset and the noise of ten circuit samples, mean value of the offset is -0.02 V and standard deviation of the noise is 0.25 mV rms.

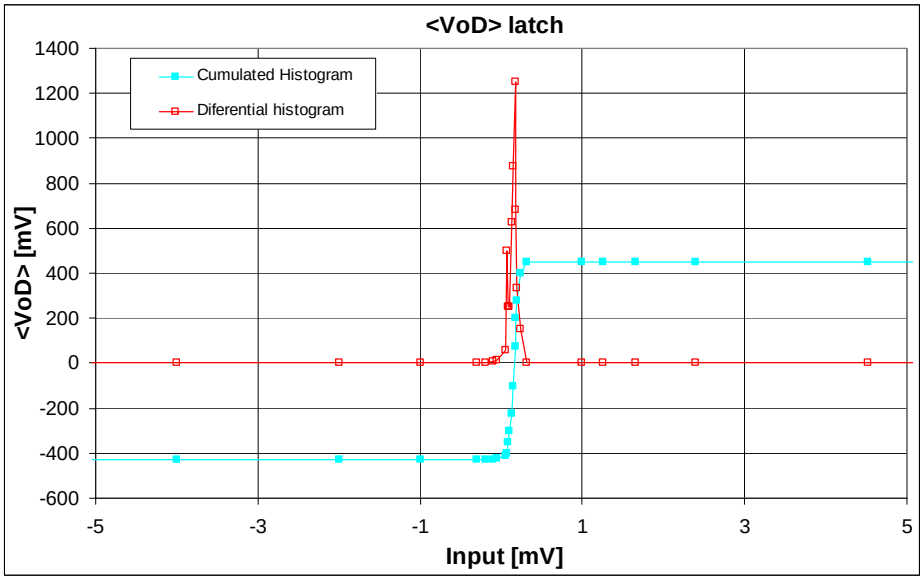

Figure 6-21. Transfer function of the comparator.

The operation of the comparator is shown in Figure 6-22. When controlling signal corresponding to Ref1 is high the circuit is in the evaluation state. In this state, the propagation delay is about 4 nanoseconds after the zero crossing of the DM input signal.

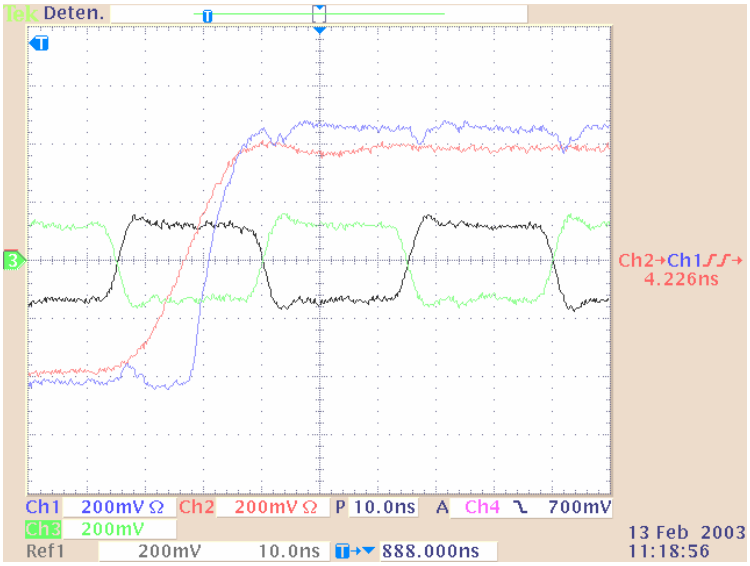

Figure 6-22. Operation of the comparator. Ch2: DM input signal, Ch1: DM comparator output, and Ch4 and Ref1 are the DM controlling signals.

The input CM range is 0.6 V< V_{iC}<–0.4 V for V_{iD}=300 mV.

6.1.7 DAC

The static transfer function of the DAC for different full scale values (Vref) is shown in Figure 6-23. It shows a linear behavior, and can be approximated with the expression,

$$V_{oD} = a\left(\frac{Dig\_code}{64}\right)Vref + offset \qquad (9.1)$$

The mean value of the slope *a*, for 10 circuits, is 0.641 and the tolerance 1%. The offset is different for negative and positive codes. The mean value for the positive ones it is -0.4 mV and +0.4 mV for the negative codes. The standard deviation of the offset is 0.25 mV rms.

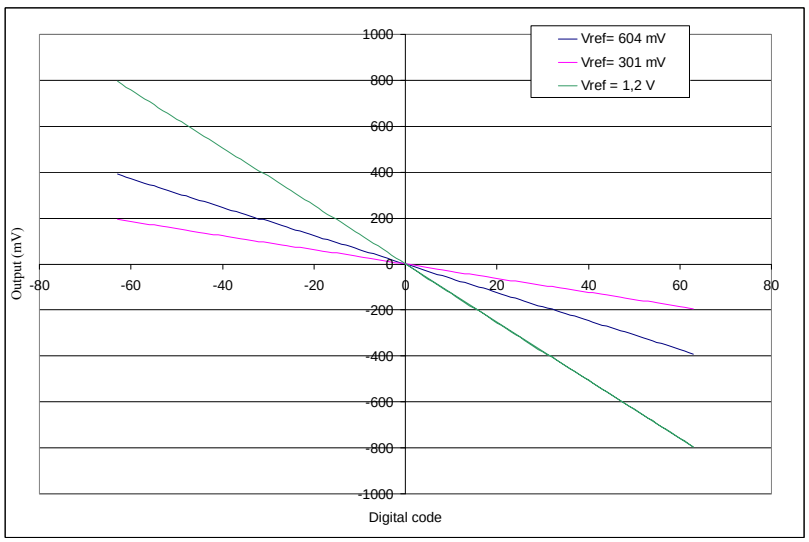

Figure 6-23. Transfer function of the DAC for different full scale values.

The differential non-linearity (DNL) and the integral nonlinearity (INL) errors are shown in Figure 6-24 and in Figure 6-25, respectively. After measuring 10 circuit samples, maximum DNL error is 1 least significant bit (LSB) and maximum INL error is 0.6 LSB. There is no influence of Vref value.

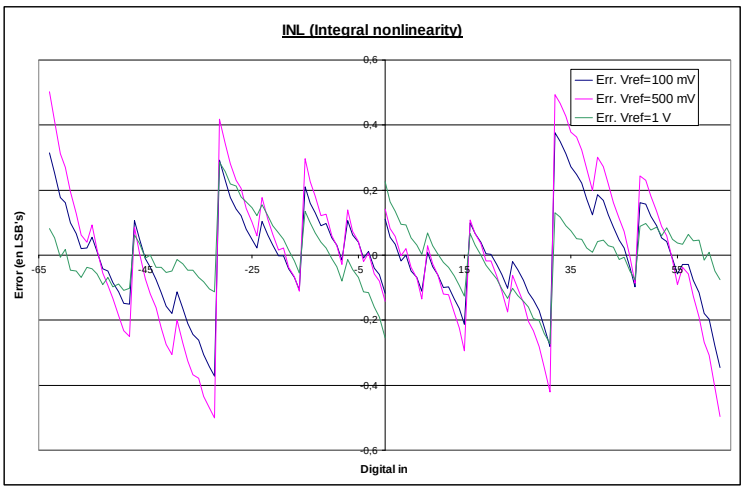

Figure 6-24. Differential non-linearity error for different values of full scale.

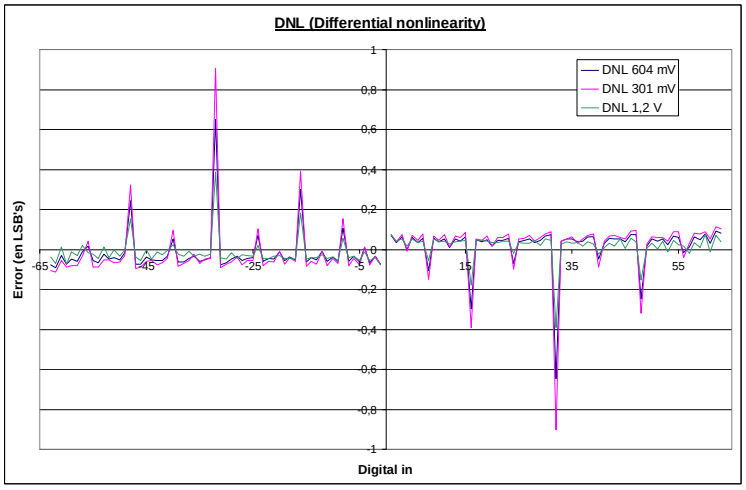

Figure 6-25 Integral non-linearity error for different values of full scale.

The settling time to the 10% is about 200 ns, see Figure 6-26. This slow response is caused by the capacitors used to reduce the bandwidth of the circuit to 2 MHz to limit the noise bandwidth.

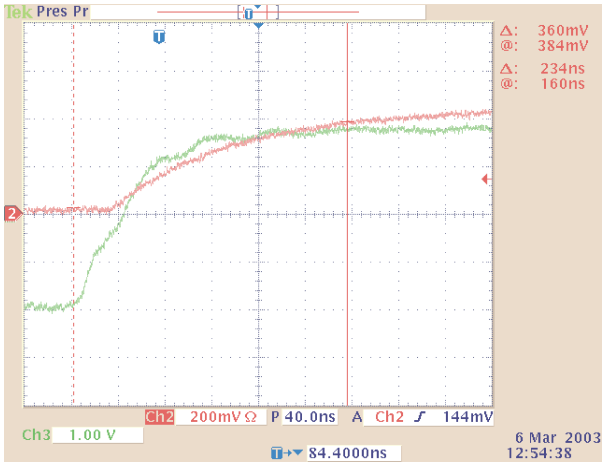

Figure 6-26. Settling time of the DAC. Ch2: DM output, Ch3: most significant bit.

The bandwidth is between 1 and 2 MHz as shown in Figure 6-27.

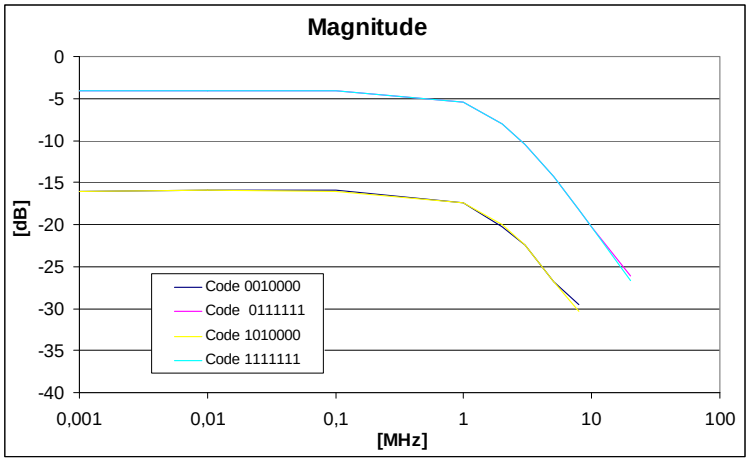

Figure 6-27. Magnitude of the frequency response of the DAC for different digital codes.

6.1.8 ECL to CMOS converter

The operation of the pseudo ECL to CMOS converter is shown in Figure 6-28. Rise time is about 15 ns, fall time about 13 nanoseconds and delay about 9 ns. Those values have been obtained from the measurement of 10 samples, standard deviation of all parameters is below 500 ps and maximum values are 15.8 nanoseconds for the rise time, 13.5 nanoseconds for the fall time and 10.5 nanoseconds for the delay. It has been also checked that the circuit tolerates variations up to the 50 % in the levels of the pseudo ECL input signal.

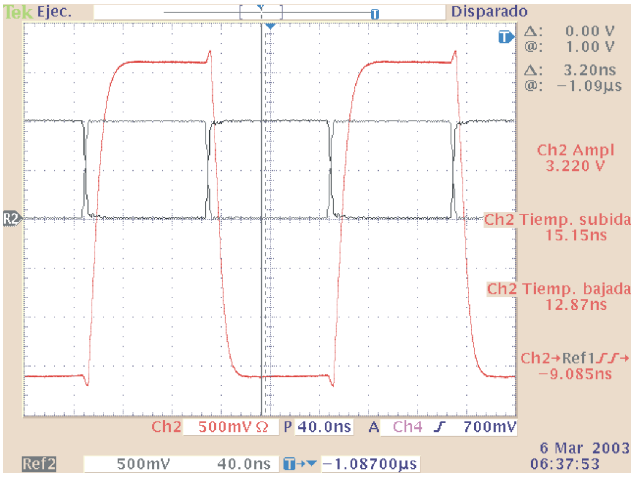

Figure 6-28. Operation of the ECL to CMOS converter. Ch2: DM output. Ref: input signal.

6.1.9 Band gap current source

The band gap sources provides two references, a current *Irefbip* of about 130 µA and a voltage *Vrefbip* for current mirrors of about -0.72 V. Mean value (10 samples) of the *Irefbip* is 129.36 µA with a standard deviation of 0.8 µA r.m.s and mean value of the *Vrefbip* is -0.725 V with a standard deviation of 2 mV rms.

Figure 6-29 shows the current as a function of the voltage at the output node of the source. A minimal drop of 200 mV in the current source is needed for a correct operation. The output impedance of the source is about $\Delta v/\Delta I \approx 1.35\ M\Omega$, close to simulation result (1.7 MΩ).

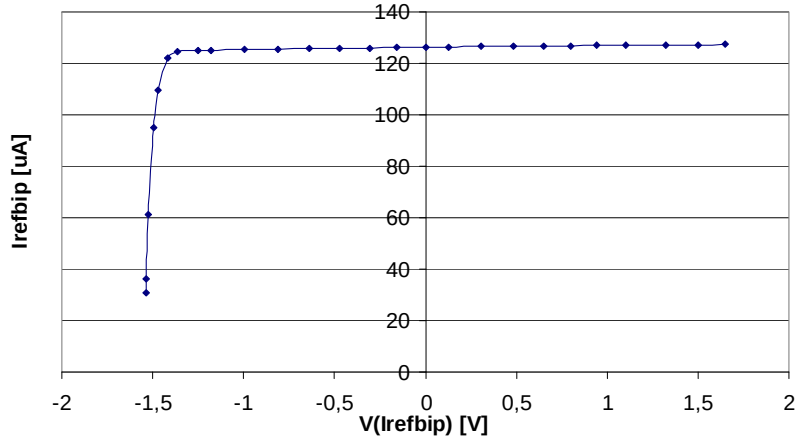

Figure 6-29. Band gap source output urrent as a function of the voltage at the output node.

The dependence of bias current with power supply variations is shown in Figure 6-30 for Vee and in Figure 6-31 for Vcc. The sensitivity to power supply variations is $\frac{\Delta Irefbip}{\Delta Vee \bullet Irefbip_{Vcc=-1.65V}} = -4\frac{\%}{\mathrm{V}}$ and $\frac{\Delta Irefbip}{\Delta Vcc \bullet Irefbip_{Vee=-1.65V}} = -3.2\frac{\%}{\mathrm{V}}$.

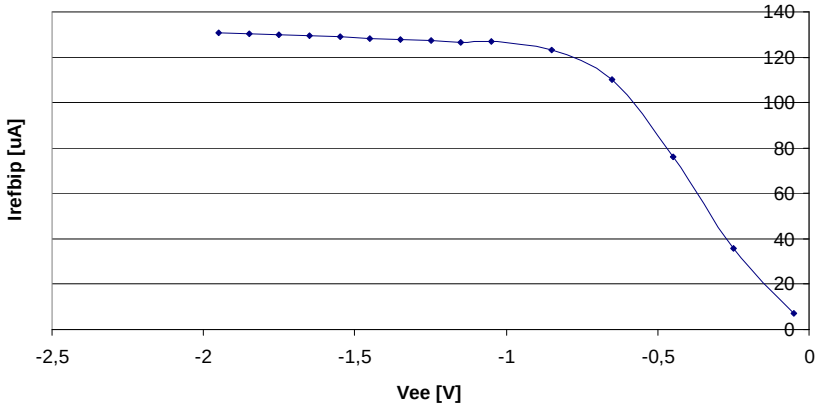

Figure 6-30. Band gap reference current as a function of Vee.

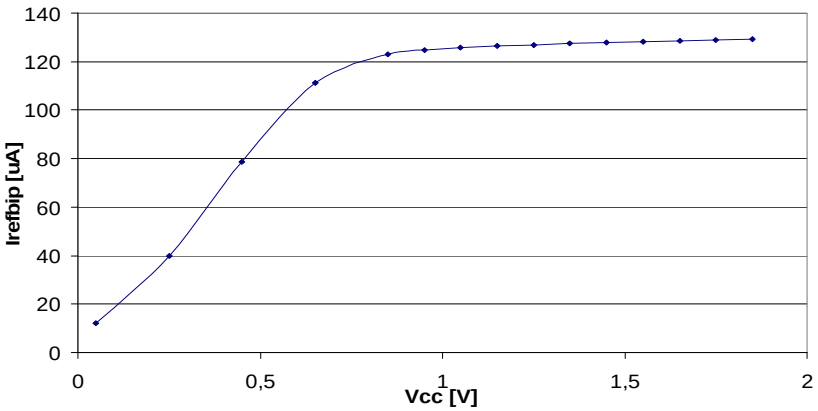

Figure 6-31. Band gap reference current as a function of Vcc.

Measurement results of the dependence bias current *Irefbip* with temperature are shown in Figure 6-32. The temperature coefficient of *Irefbip* is 277 ppm/ºC, close to expected values (300 ppm/ºC). For the voltage reference *Vrefbip* the TC is about 20 ppm/ºC.

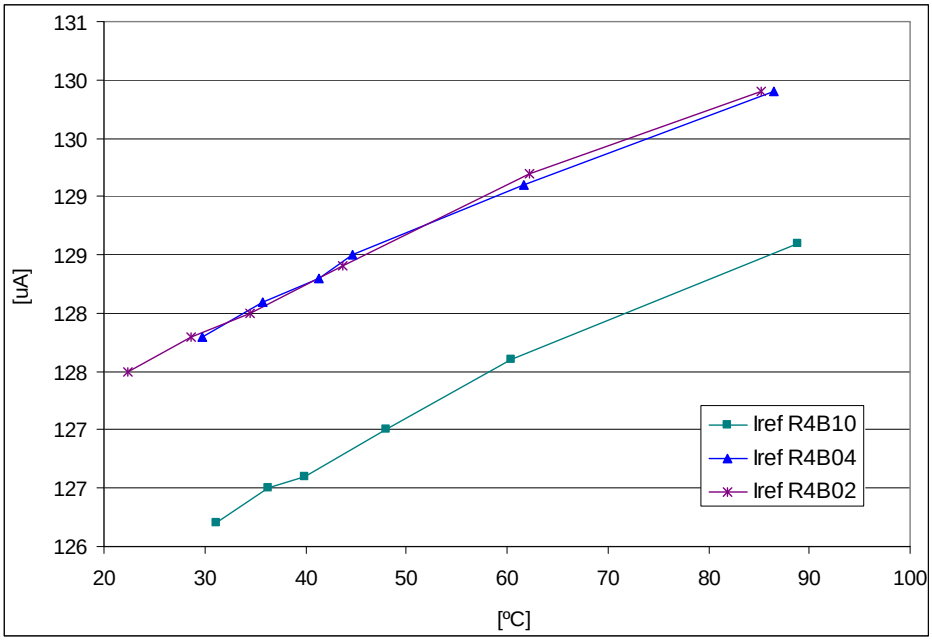

Figure 6-32. Band gap reference current as a function of temperature for three circuit samples.

6.2 Results related with system level characterization

Characterization of the full processing channel on 8 channel ASICs (Figure 6-33) includes measurements on offset, noise, linearity, pile-up correction system, consumption, stability and other.

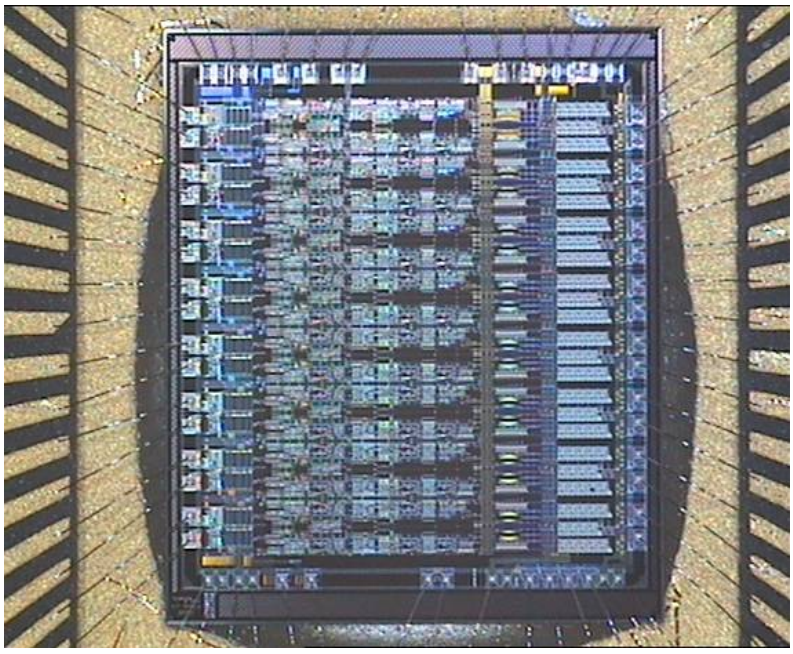

Figure 6-33. Microphotograph of the die of the 8 channel ASIC.

Figure 6-34 shows the test set-up. The ASIC test board includes:

- Generation of internal ASIC DACs reference and control signal for pile-up compensation (Vsub). The parallel port of the PC controls several I2C 12 bit DACs (MAX5822).
- Reception and division of the 40 MHz clock.
- Injection of charge pulses (using and AC coupling capacitor).
- Level adaptation.

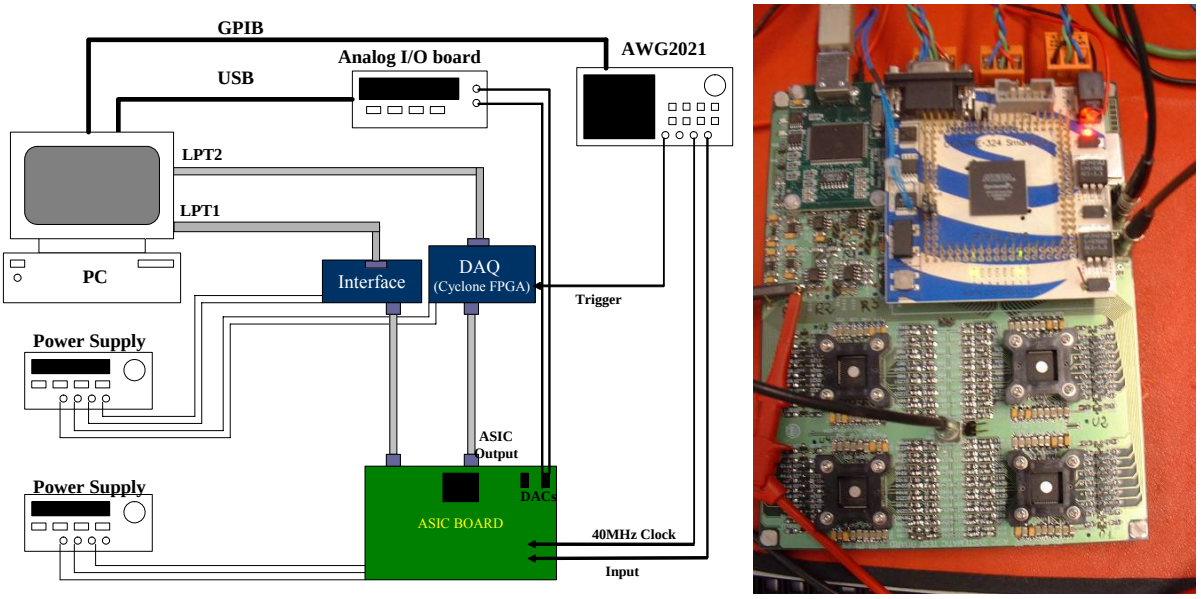

Figure 6-34. Schematic and photograph of the test set-up.

The ASIC outputs with the 20 and 40 MHz clocks are transmitted to the acquisition board [176], the core of the readout system is an Altera Cyclone FPGA. It is used to implement an 8 channel DAQ with a 32 positions buffer to synchronize with trigger and 256 events memory. Output data is transmitted to PC through parallel port.

An arbitrary waveform generator (AWG2021 of Tektronix) is used to generate clock, trigger and input signal. The input signal is a voltage step, connected to the channel input by a 1.5 pF capacitor. This generator is controlled by PC trough GPIB bus in order to perform automatic linearity tests varying the signal amplitude. Analog I/O boards are included in the system to perform automatic calibrations of analog control signals (reference for internal DACs and control signal for pile-up compensation).

In order to estimate the effect of packaging, both EDQUAD TQFP and JLCC chips have been tested with a test socket and directly soldered on a PCB. In Figure 6-34 we see the test card for EDQUAD chips.

Results concerning to noise, offset, linearity and burn in correspond to tests performed to the full production of about 1500 units in EDQUAD TQFP package and for the 10 prototypes in JLCC package; test with PMT in laboratory or in test beam or test of crosstalk have been performed only on reduced subset of chips. Some of the test and the burn in have not been performed on the ASIC test card but directly on the VFE board ([177], Figure 6-35), with 8 chips soldered.

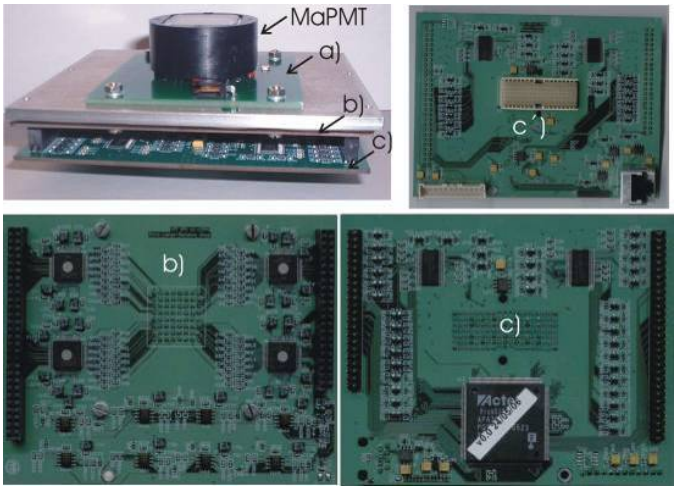

Figure 6-35. VFE card: a) PMT base board, b) ASICs board and c) FPGA board (c' is the bottom view of c).

Since the output of the channel is binary, there is no access to the analogue value of the signals before the comparator. The conventional method of measuring the performance of systems with binary output is based on a scan of the threshold whilst injecting a known charge into the amplifier, yielding the occupancy of a channel as a function of its discriminator threshold; the ''S-curve'' for that channel ([178] and [179]). An example of S-curve is shown in Figure 6-36, and has been also shown for the comparator in Figure 6-21. All the measurements of the offset, noise and with signal will be based on this procedure. Offset and signal are deduced from the mean value of the differential of the S-curve and noise from the standard deviation of the differential of the S-curve.

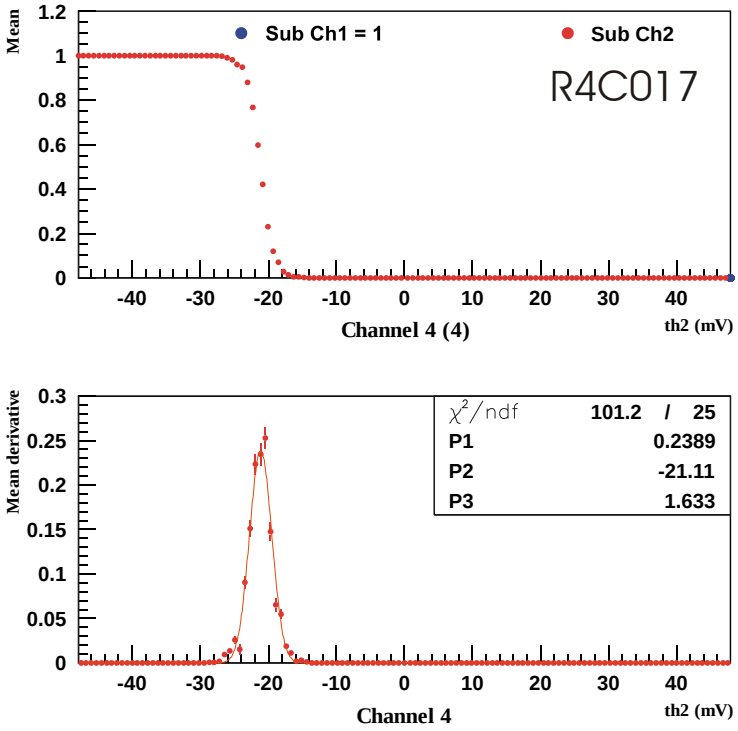

Figure 6-36. Example of S-curve obtained through threshold scan. Top: S-curve. Bottom: differential of the S-curve fitted to a Gaussian PDF.

On a prototype chip internal signals of the ASD channel have been monitored using the output buffers to be able to drive pad capacitance, a measurement of this is shown in Figure 6-37.

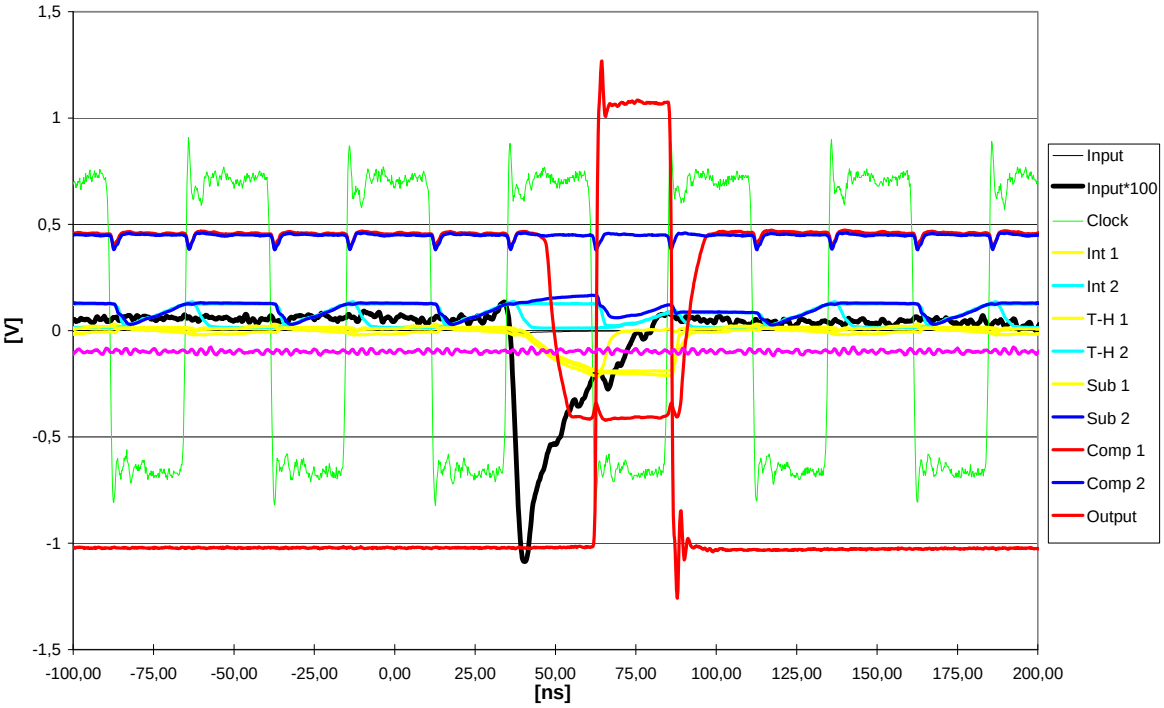

Figure 6-37. Internal signals for typical input pulse.

Table 6-4 summarizes results of the test of the engineering run of the 8 channel chip. Yield is 80 % and less than the 1% have been discarded due to high offset, which means either <-300 mV or >250 mV for V_{subD}=0.

Total	1311	100 %
Digital Error	112	8.5 %
Bias problem	38	3 %
General failure	29	2.2 %
1 dead channel	73	5.6 %
1 ch. high offset	9	0.7 %
Pass	1050	80 %

Table 6-4. Results of the test of the engineering run of the 8 channel chip.

6.2.1 Offset effect and threshold dispersion

The offset for the 8 channels (2 subchannels each) of about 500 chips is shown in Figure 6-38. Mean value is -65 mV whereas it should be around -50 mV according to hand calculations and post-layout simulations. Probably, the reason for the difference is the non-zero value of the OZE of the integrator which is about -20 mV. As said in section 6.1.2 part of this effect can be present in the full channel and could be related to clock coupling due to layout mismatches and substrate noise. The test of the 500 chips has been performed on a test socket; therefore it is possible that the additional parasitic capacitance causes some extra charge injection.

Standard deviation is 61 ± 1 mV r.m.s whereas for hand calculation and Monte Carlo simulations it should be 55 mV r.m.s. As explained in section 1.2.4.1, both hand calculations and Monte Carlo simulations assume local variations. Local parameter variations affect, at most, one single device such a transistor. Global parameter variations affecting all transistors in a given region are caused by non-

uniformities across the wafer. Best is splitting large area devices in a common centroid layout and to minimize distance between the small devices. This has been done for all relevant devices; however non-linearities in the global variations or imperfect centroid layout will mean that global variations will have some impact on the offset distribution. Anyway, value of the mean offset and standard deviation of the offset fulfill requirements.

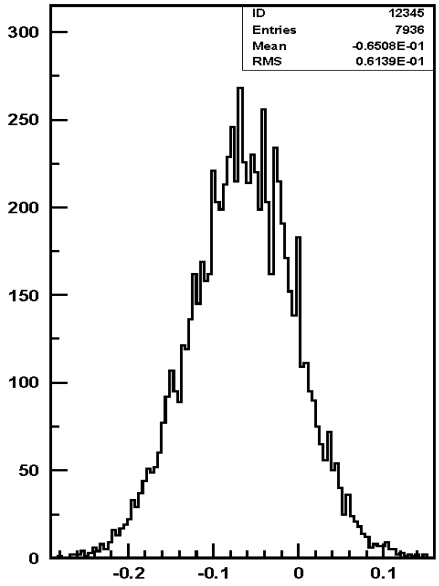

Figure 6-38. Offset distribution (in mV) for 500 chips for V_{subD}=0.

The results have been analyzed also per channel and per subchannel. Comparing 4000 upper subchannels with 4000 lower subchannels, difference between both is about 1 mV both for the mean and for the standard deviation; this is smaller than the statiscal error. Standard deviation of the difference of the offset on the two subchannels of each channel roughly corresponds to the standard deviation of the OZE of the integrator, as expected from the analysis in section 5.2.3.

The Table 6-5 shows the mean value offset per channel and per test socket for a V_{subD} of 200 mV. About 150 chips have been measured in each test socket. From these results we can conclude that there is a systematic effect according to the position in test card, but we can not conclude that there is a systematic difference between channels. Indeed some chips were measured in different sockets and the results confirm that the systematics are introduced by the test card. There is no difference in the standard deviation within statiscal errors.

Socket / Ch	1	2	3	4
1	-0.09	-0.093	-0.09	-0.096
2	-0.082	-0.092	-0.094	-0.09
3	-0.082	-0.077	-0.082	-0.084
4	-0.079	-0.087	-0.095	-0.096
5	-0.093	-0.086	-0.089	-0.079
6	-0.085	-0.074	-0.084	-0.076
7	-0.092	-0.088	-0.08	-0.085
8	-0.095	-0.1	-0.1	-0.089

Table 6-5. Mean offset (in mV) per channel and per test socket (about 150 chips per table cell).

That means that there are not relevant differences in layout or chip bonding that affect the offset between the two subchannels or between different channels.

Some measurements have been performed on the effect of the tile correction gain on the offset, see Figure 6-39. According to the analysis in section 5.2.3, the dependence of the offset of each channel on pile up compensation gain $G_{cc}(V_{subD})$ and as G_{cc} is linear for this range of V_{subD}, the offset depends linearly on V_{subD} with a slope $IZE_P A_{DD}(0) G_{0I} G_{CC}(V_{subD})$. In normal circuit operation,t G_{cc} is negative and the pile-up compensation helps to minimize the apparent offset at the input of the integrator.

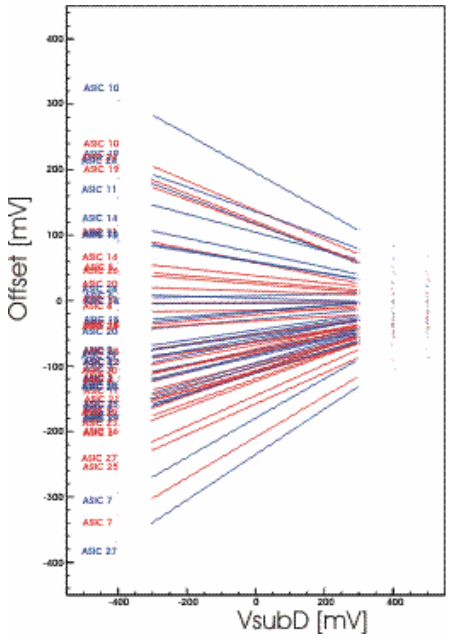

Figure 6-39. Offset for 30 channels as a function of V_{subD}.

The mean value of the offset for 64 channels as a function of the integration time is shown in Figure 6-40, and the measured data is compared with theoretical calculations and simulations (see section 5.2.3). Error bars represent statistical errors both in measurement and simulation. Agreement is quite good, although calculations and simulations seem to underestimate a little bit the offset. As said before, probably due to some charge injection phenomena in the integrator that it is not reproduced in simulation. Indeed the agreement with experimental results, it is better than it was for the measurement of the 500 chips in the test socket, it seems reasonable to think that some charge injection in the socket produce a systematic variation in the value of the mean offset.

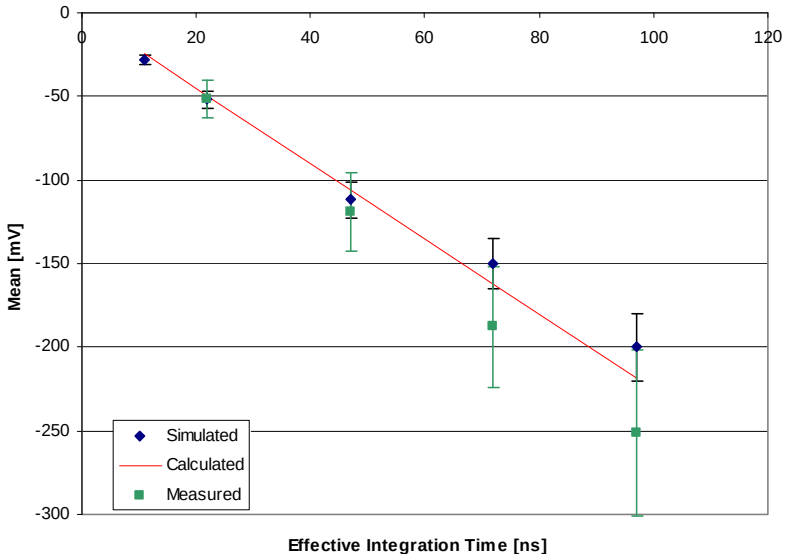

Figure 6-40. Mean value of the offset in the 64 channels as a function of integration time.

In Figure 6-41 we see that the test results are compatible with calculations and simulations, although again the offset seems to be underestimated probably for the same reason.

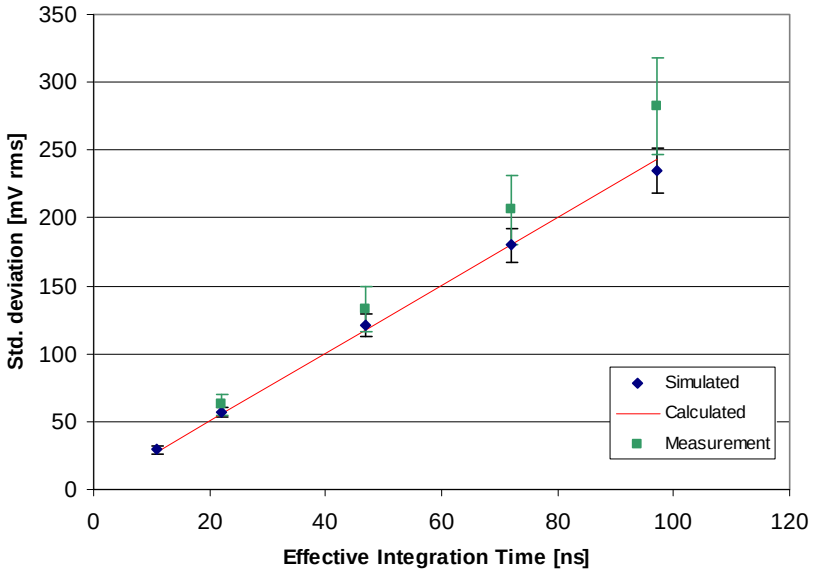

Figure 6-41. Standard deviation of the offset in the 64 channels as a function of integration time.

The effect of the mismatch on the source resistors at the input of the chip on the offset has been also studied. One of them is fixed at 400 Ω and the other one (R_{inL}) is varied from 0 to 1k5Ω. Slope is approximately -0.3 mV/Ω, and is given by the product of the DC gain of the channel, the mismatch value and the input bias current (about 5μA).

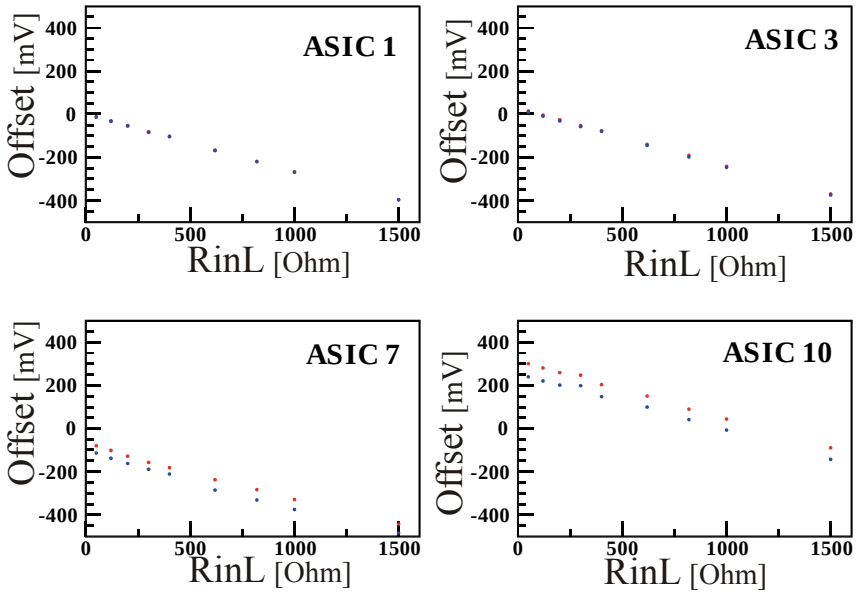

Figure 6-42. Effect of mismatch of the source resistors for 1 channel of 4 different ASICs (subchannel 1 in red and subchannel 2 in blue).

6.2.2 Noise

The noise for the 8 channels (2 subchannels each) of about 500 chips is shown in Figure 6-43. Mean value is about 2.2 mV r.m.s for a V_{subD}=-200 mV, close to the expected value: 2.3 mV r.m.s. The effect of changing V_{subD} is negligible on the noise (below 0.1 mV r.m.s). This measurement has

been obtained with ASIC test set up. Entries at bin 0 correspond to some channels that were out of range of the threshold scan.

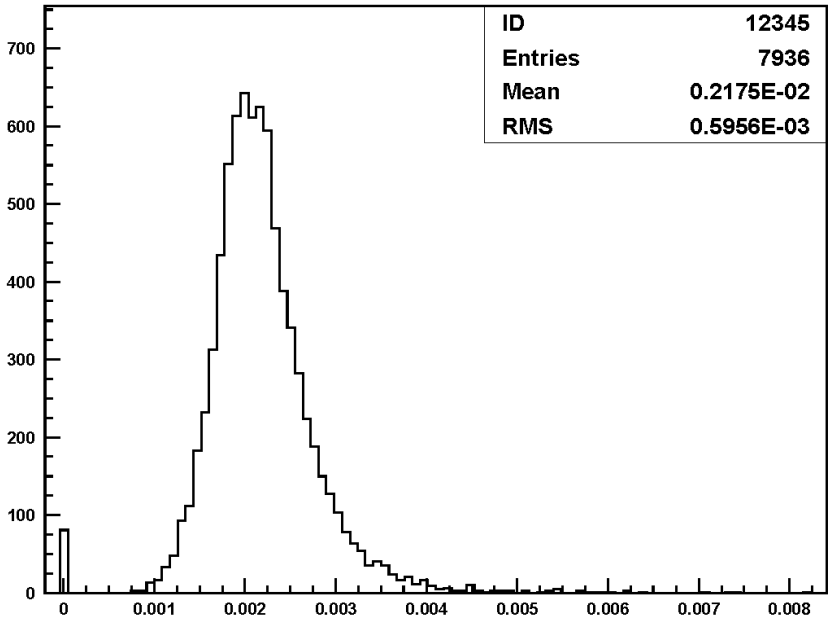

Figure 6-43. Noise distribution (in mV) for 500 chips for V_{subD}=-200 mV.

There are no relevant differences in the noise observed for the two subchannels. Again there are systematic differences according the test socket, which means pick up noise is relevant in some positions. This corresponds to the tails of the distribution in Figure 6-43. Indeed the pick-up was very high at the beginning of the test. Figure 6-44 shows a modification that was necessary to do on the test card. A copper shield was added over digital lines routed close to sensitive inputs; this action reduced the pick up noise for those channels to the level presented by other channels.

Figure 6-44. Photograph of the test card with copper shielding.

In Figure 6-45 we can observe a typical threshold scan without any evidence of pick-up noise. A good S-curve fitting has been obtained.

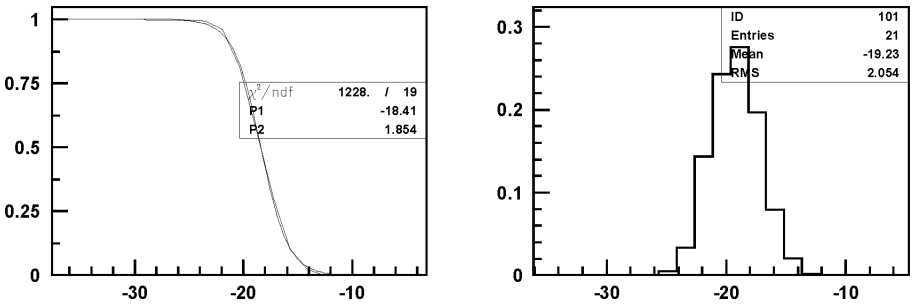

Figure 6-45. Threshold scan (left) with good fit of an S-curve and differential histogram (right).

In Figure 6-46 we see a threshold scan with pick-up noise effects, both the RMS of the differential distribution and the corresponding parameter (P2) of the S-curve reflect the excess noise.

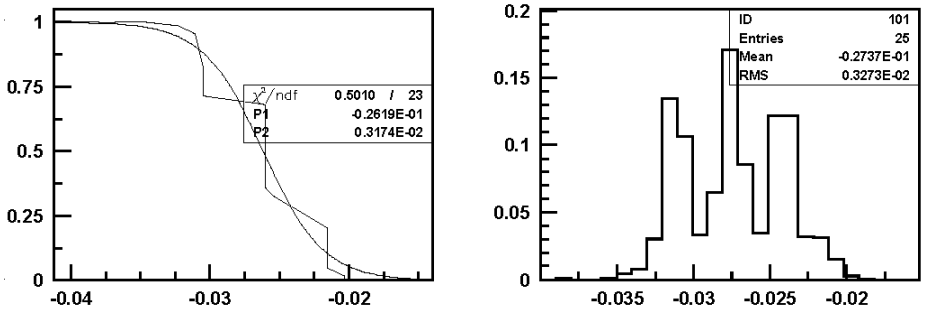

Figure 6-46. Threshold scan (left) with bad fit of an S-curve and differential histogram (right). X-axis is threshold value in V.

This kind of problem has been observed in many different set-ups and cards. It is crucial to design very carefully the PCB, with good grounding and decoupling, and also the whole system, specially the power distribution.

VFE cards have been test at the LHCb pit after installation, mean value of the noise of the 64 channels of each card is always between 2.2 and 2.5 mV rms. Typically the distribution of the noise is very narrow (Figure 6-47), but in a few cards we find a few channels with extra noise. These results are obtained with MaPMT. If grounding is good enough no excess noise is observed with MaPMT base board connected, otherwise pick up noise is observed in some situations. No excess noise is observed when the HV of the MaPMT is set to nominal value (-700 V).

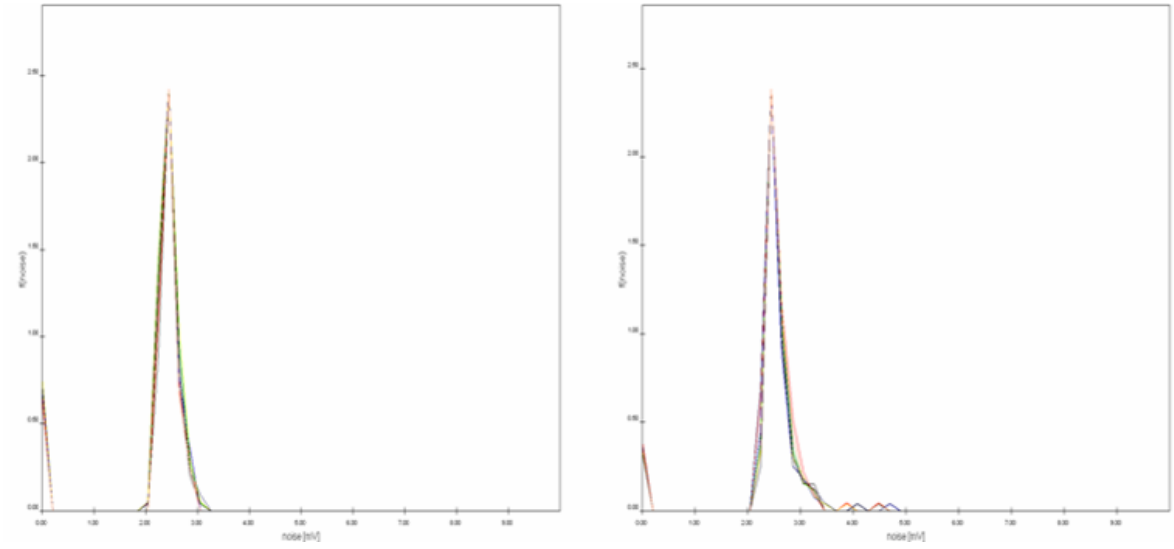

Figure 6-47. Noise distribution for the 64 channel of a VFE card without excess noise (left) and with excess noise (right) and for 8 consecutive clock periods.

Figure 6-48 shows the noise in 64 channels as a function of the integration time. Comparison with theoretical values calculated in section 5.1.3 is also shown. It is clear that for high integration times the measured noise can not be only related to thermal noise, and the slope seems to be in good agreement with the effect of *1/f* noise calculated in section 5.1.3.

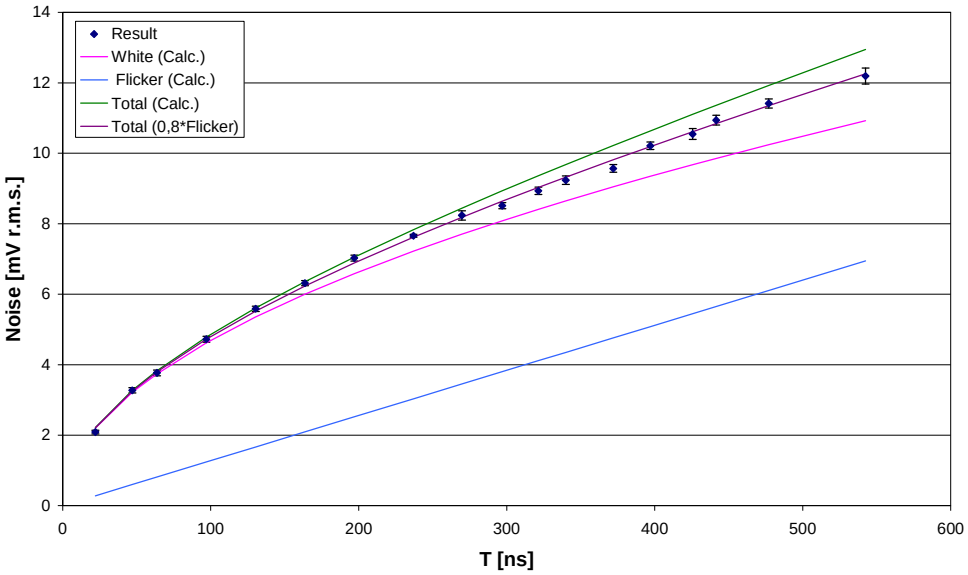

Figure 6-48. Noise in 64 channels as function of the integration time.

Nevertheless the effect of *1/f* noise is overestimated, if we take the 80 % of the calculated value of Flicker noise plus the thermal noise the agreement with experimental data is very good. The variability of *1/f* noise parameters might be a good explanation for this disagreement; it is well know that those parameters suffer from big fluctuation. Flicker noise constant K_f not only varies by orders of magnitude from one device type to the next, but it can also vary widely for different transistors or integrated circuits from the same wafer [66]. This is due to the dependence of flicker noise on contamination and crystal imperfections, which are factors that can vary randomly even on the same silicon wafer.

In section 5.1.3 it was also studied the effect of the value of the source resistance (PMT load) on the noise, a comparison between theoretical prediction and measurement is shown in Figure 6-49. As expected, when the R_s is low enough the time constant of the input node is much smaller than the integration time (25 ns here) and the noise is $\alpha\sqrt{R_s}$ but when this time constant starts to be comparable to the integration time the noise does not increase any more with R_s.

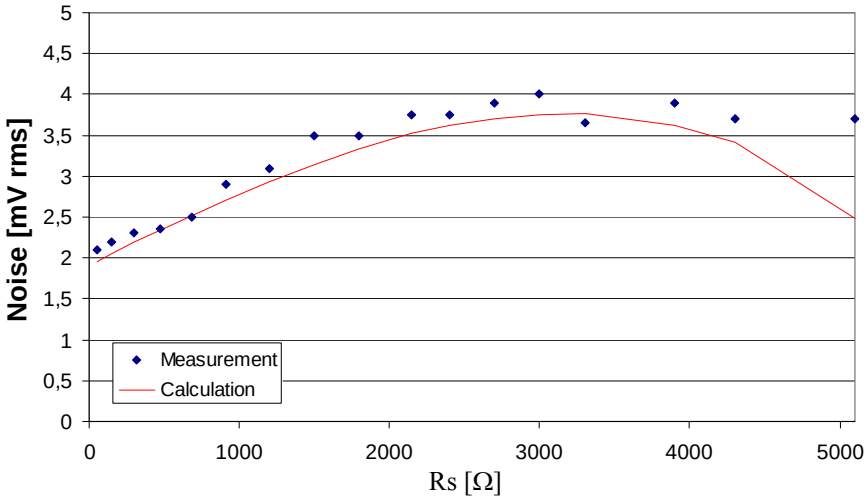

Figure 6-49. Noise as a function of the PMT load or source resistance (R_s).

6.2.3 Power consumption

There are three different voltage domains: for the analog part, for the digital part and for the clock system of the analog part.

The supply current of the analog part of the chip is about 160 mA, with fluctuations below 1% for typical variations of main circuit parameters: value of input signal, value of subtraction, state of the outputs, etc.

The supply current of the digital part is about 10 mA without activity on the channel output. The digital part is mostly CMOS, thus power consumption depends a lot on operation frequency and on the load capacitance. Nevertheless the power consumption of the logic is not zero even without IO activity. For the maximum frequency of commutation of the outputs (20 MHz), it increases to 30 mA. The influence of the serial interface of the DACs on power consumption is negligible, because their frequency of operation is low (<1 MHz) and because there is only one output pad corresponding to this part.

The supply current of the clock circuitry is about 20 mA. Thus, total power consumption is between 630 and 690 mW. This fulfills requirements resumed on section 3.4.4.

When a chip has different sets of supply voltages, it is important to test all the possible combinations of power up sequences because failures or delays in power supply system may introduce delay between the power up of supply voltages. All the combinations have been tested. Sometimes there are over consumptions when one of the voltages is not connected (protection diodes can be in forward bias), but when all get connected the consumption is inside nominal values and the chip operates as expected. No circuit gets stuck.

6.2.4 Electrical signal measurements

As said before, for signal measurements a step signal (V_{STEP}) is differentiated through a $C_{AC}R_S$ high pass filter, whose time constant must much smaller than the step duration. The circuit is shown in Figure 6-50, a differential injection method is used to cancel systematic errors (for instance parasitic capacitances) taking profit from the fact that input of the chip is differential. The resistance is the R_S or R_{PMT} resistance connected at the input of the chip. Ideally the charge injected by the coupling capacitor C_{AC} is $Q=V_{STEP}\cdot C_{AC}$. Rise time of V_{STEP} must be small enough so that all the charge pulse is concentrated in 25 ns. However, stray capacitance at the input of the chip is high (about 12 pF), and for an R_S of 470 Ω the signal spills over more than 1 clock cycle: about the 88% of the signal is in the first clock cycle and the 10% in the next one. The fraction of the signal in first clock cycle is taken into account in the charge computation, so the data has been corrected at the acquisition time. The fact that 10% of signal is in the second clock cycle it is not taken into account by the acquisition but it is taken into account in the data analysis.

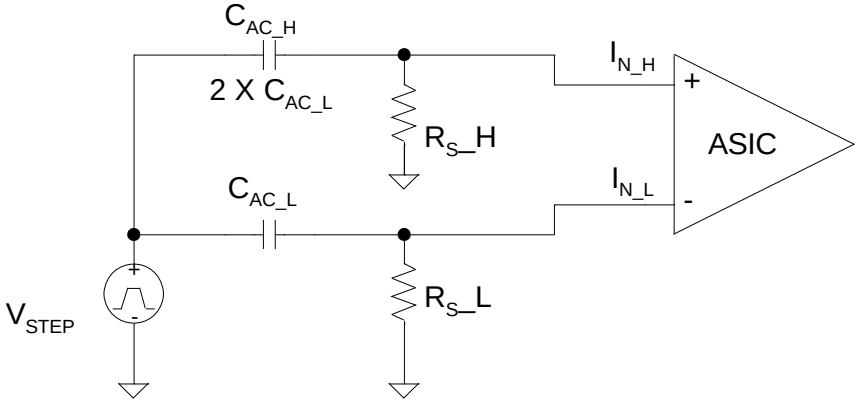

Figure 6-50. Differential signal injection.

6.2.4.1 Signal

Figure 6-51 shows the threshold offset as a function of the injected charge for R_S=390 Ω. Gain of the channel is about 0.94 mV/fC. For the nominal resistance R_S=470 Ω gain is 1.16 mV/fC. The tolerance of the C_{AC} capacitors is much higher; therefore correction of the systematic error has been needed. Some chips have been measured in the 4 sockets and the data has been used for calibration. After the corrections, the tolerance in the gain is about 3% for the full production

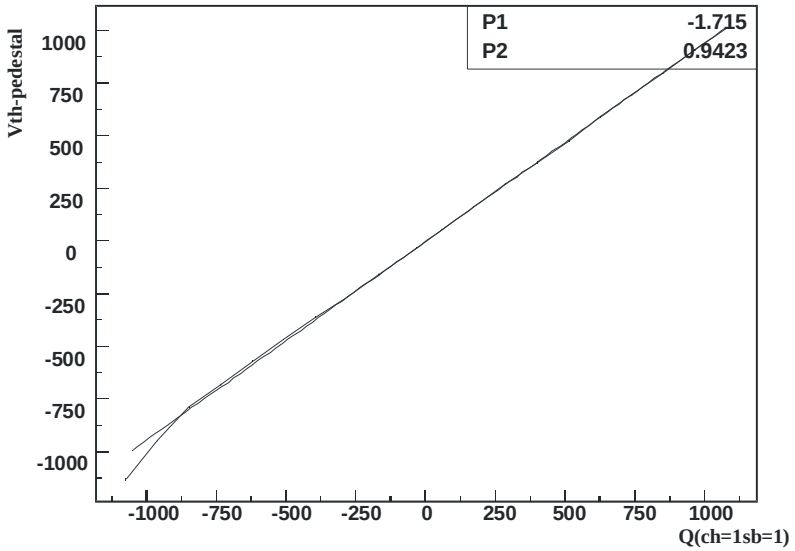

Figure 6-51. Threshold offset as function of input charge (Q) for R_S=390 Ω.

Changing the input resistance of each channel there is a modification of gain as shown in Figure 6-52. Gain variation of 2.2m/Ω.

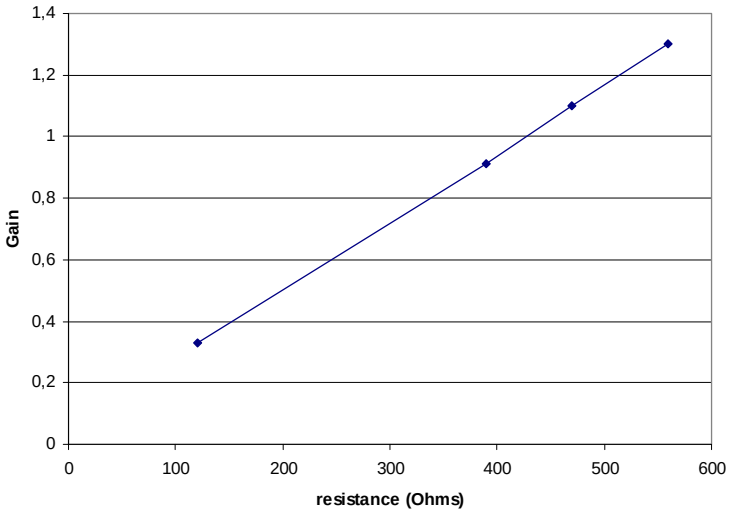

Figure 6-52. Gain as a function of the input resistance R_S.

6.2.4.2 Linearity

Figure 6-53 shows typical linearity error, it is below ±5 mV in the range of interest, although measurement seems to be limited by nonlinearity and jitter of the AWG. The acceptance criteria concerning linearity has been fixed to a linearity error < 10 mV in the range of interest.

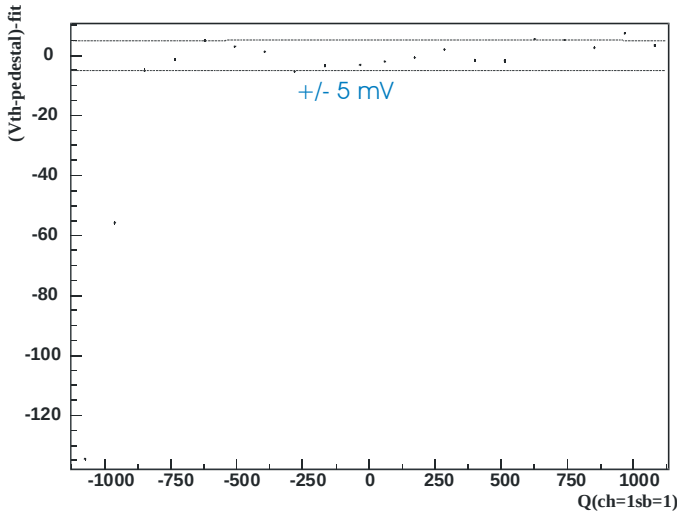

Figure 6-53. Typical linearity error of a channel computed as difference of threshold offset and fit to a linear function (in mV).

6.2.4.3 Pile-up compensation

Looking at the threshold offset in the clock period consecutive to signal injection we can study the performance of the tile correction system. As said before, it has to be taking into account that 10% of the signal spills over this period. Figure 6-54 shows the effect of the pile-up compensation system on channel output as a function of input charge and for several values of the subtraction control (Vsub) and the related linearity error, which is smaller than ±5 mV. As for linearity, the measurements seem to be limited by nonlinearity and jitter of the AWG.

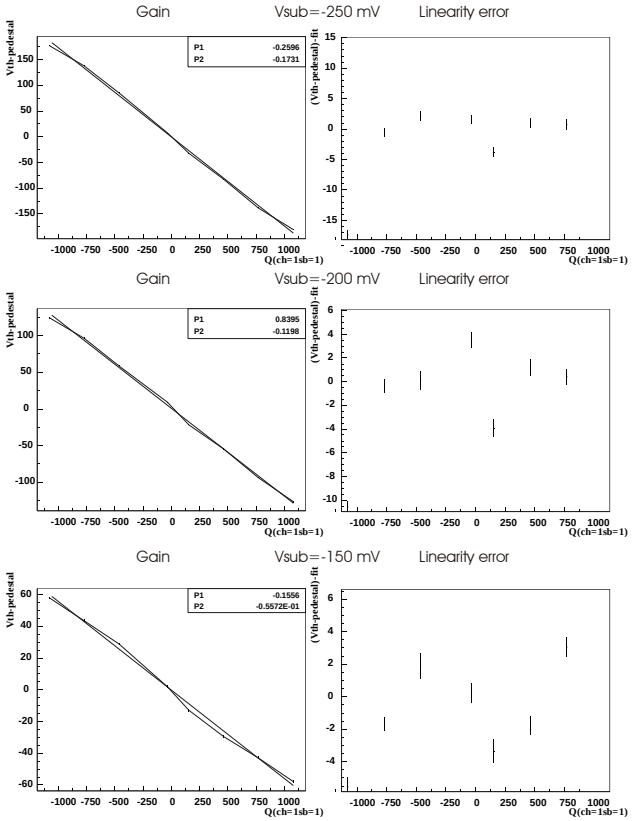

Figure 6-54. Pile-up compensation output and linearity error for several Vsub.

Figure 6-55 shows the dependence of the mean compensation gain on Vsub. Error bar indicates the RMS of this parameter for the 16 subchannels of a chip, which is below 1%.

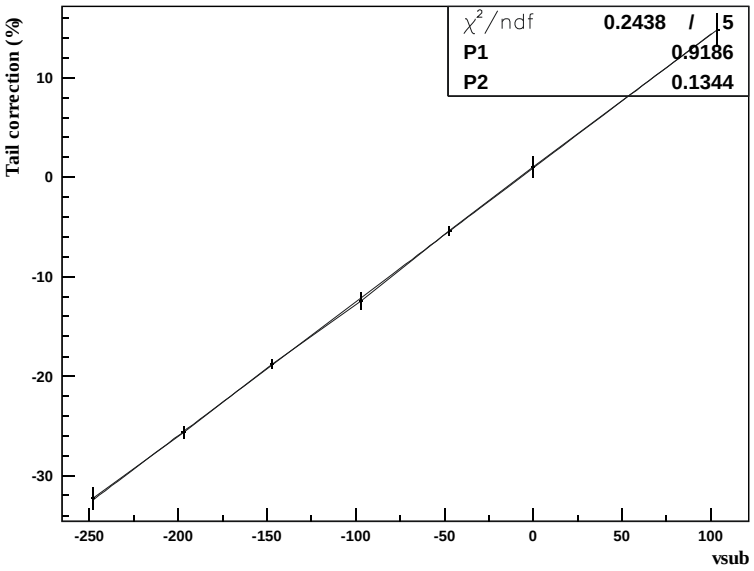

Figure 6-55. Dependence of the percentage of subtraction on Vsub. Error bar indicates the RMS of this parameter for the 16 subchannels of an ASIC.

Figure 6-56 shows the tail fraction for different Vsub. Results correspond to the measurement of the ASIC full production test. Dispersion for a given Vsub is about 2%; this allows controlling the 8 chips of a VFE card using a single DAC to set the Vsub value.

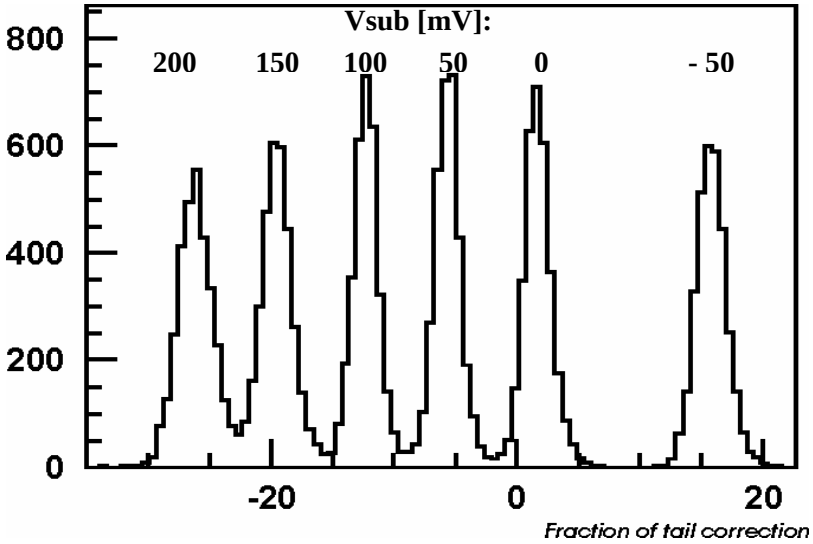

Figure 6-56. Tail correction fraction for different Vsub. Results of the ASIC full production test.

6.2.4.4 Electrical crosstalk

Figure 6-57 shows the electrical crosstalk in 64 channels of a VFE card when a current pulse is injected in channel 30. The maximum crosstalk is of the order of 1 %. As it is not optical crosstalk, the channel with maximum is not necessarily in the neighborhood of the MaPMT channel 30. Indeed, when the PCB used to inject the signal is close to the VFE card but not connected we appreciate a signal of the same order of magnitude of the crosstalk. Therefore, 1 % is an upper for the crosstalk in the VFE card and in the ASIC.

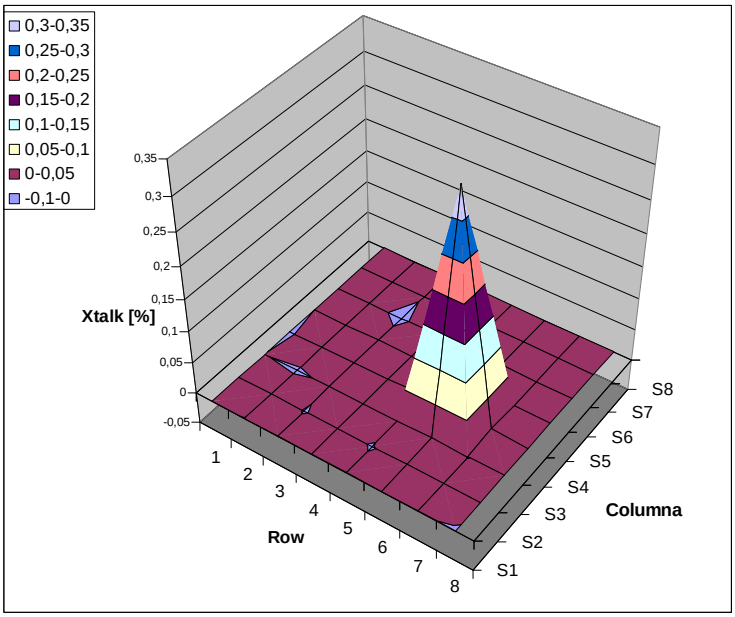

Figure 6-57. Relative threshold offset (signal) to channel 30 in the 64 channels of a VFE card (represented in the PMT channel order) when a current pulse is injected in channel 30.

6.2.5 Optical signal measurements

We will summarize the results of different tests performed to the VFE cards using light pulses in different scenarios:

- On a dedicated test bench at the UB (Figure 6-58) using a LED driver [180] through a fast pulser (decay time of about 10 ns).
- On the MaPMT test bench at the UB ([181] and [182]). The LED pulse is injected into the scintillator with a WLS fibre twisted inside. One of the fibre ends is used to scan the MaPMT surface, to perform crosstalk measurements.
- At the LHCb detector using the LED calibration system [183].

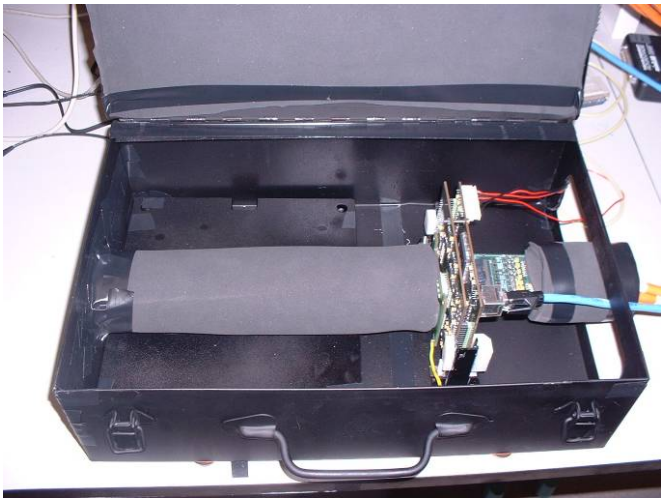

Figure 6-58. LED test set up for the VFE card.

6.2.5.1 Signal

In Figure 6-59 the temporal shape of the LED pulse can be clearly identified. The signal corresponding to the third period is drawn in Figure 6-60, following MaPMT channel distribution. Both MaPMT and illumination non-uniformities are convoluted. Channel 49 is dead.

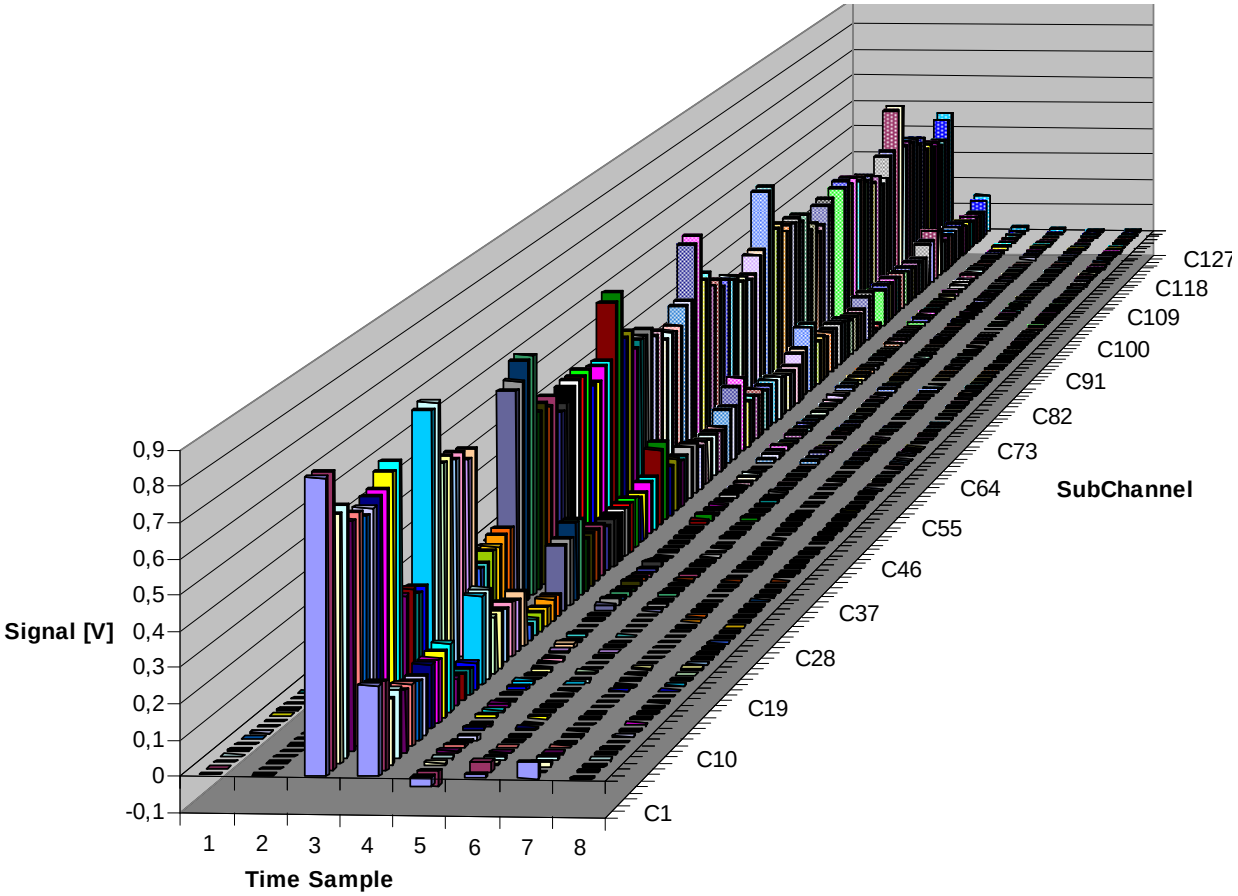

Figure 6-59. Signal for the 64 channels (128 subch) of a VFE card in 8 consecutive clock cycles.

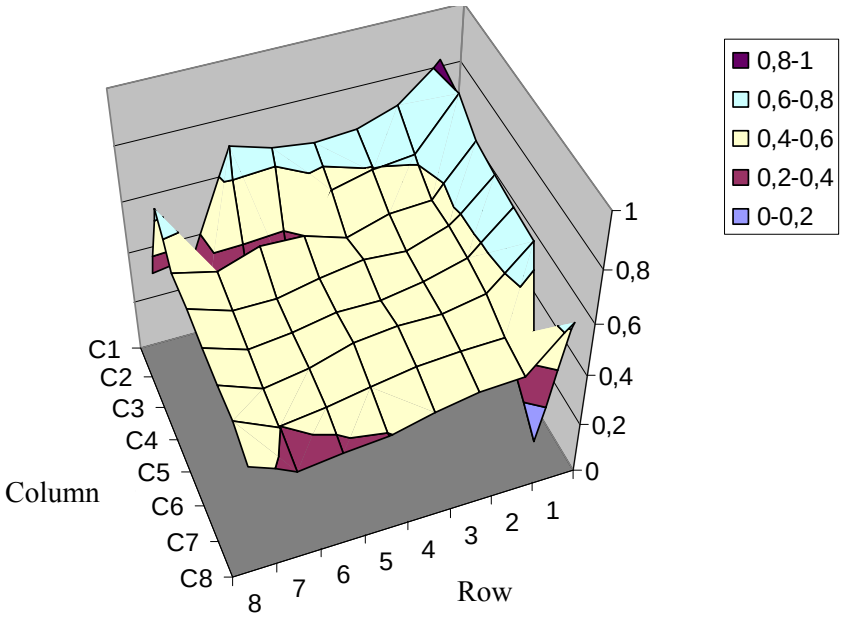

Figure 6-60. Main fraction of signal in 64 channels sorted following MaPMT pixel distribution.

The response of a VFE card as a function of the illumination is shown in Figure 6-61.

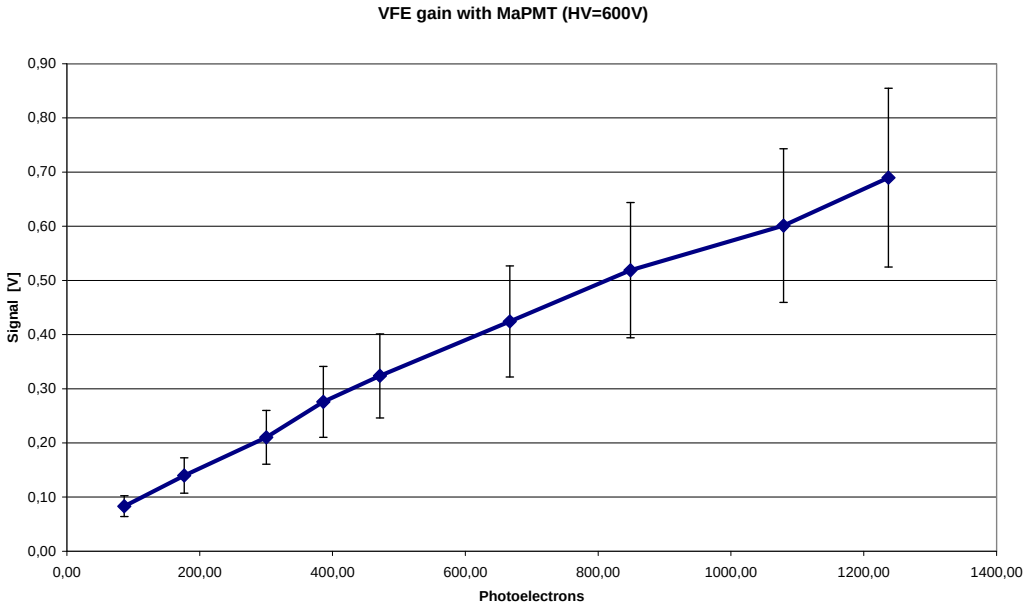

Figure 6-61. Average signal of the 64 cha of a VFE card as function of the number of photoelectrons for MaPMT HV= -600V. Error bars represent the std. dev. of the 64 channels.

6.2.5.2 Pile-up compensation

Figure 6-62 to Figure 6-65 illustrate the dependence of the tail of the signal on the V_{subD} value. Comparing Figure 6-63 (no compensation) with Figure 6-65 we see how the pile up compensation can be tunned to eliminate on average the tail of the signal.

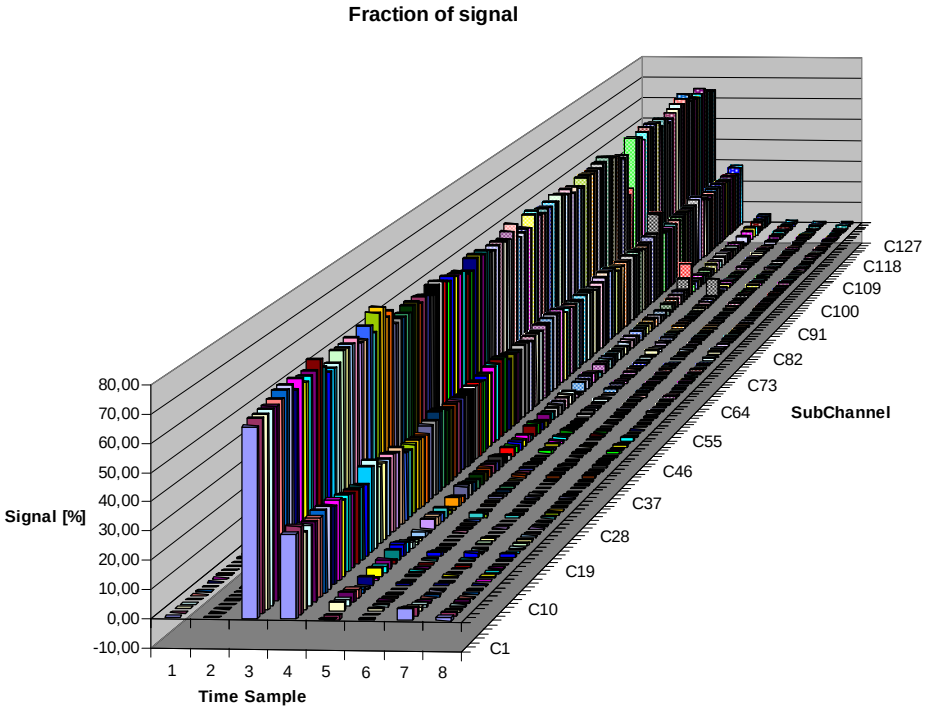

Figure 6-62. Fraction of signal on 64 channels in 8 consecutive clock cycles with V_{subD}=-100mV.

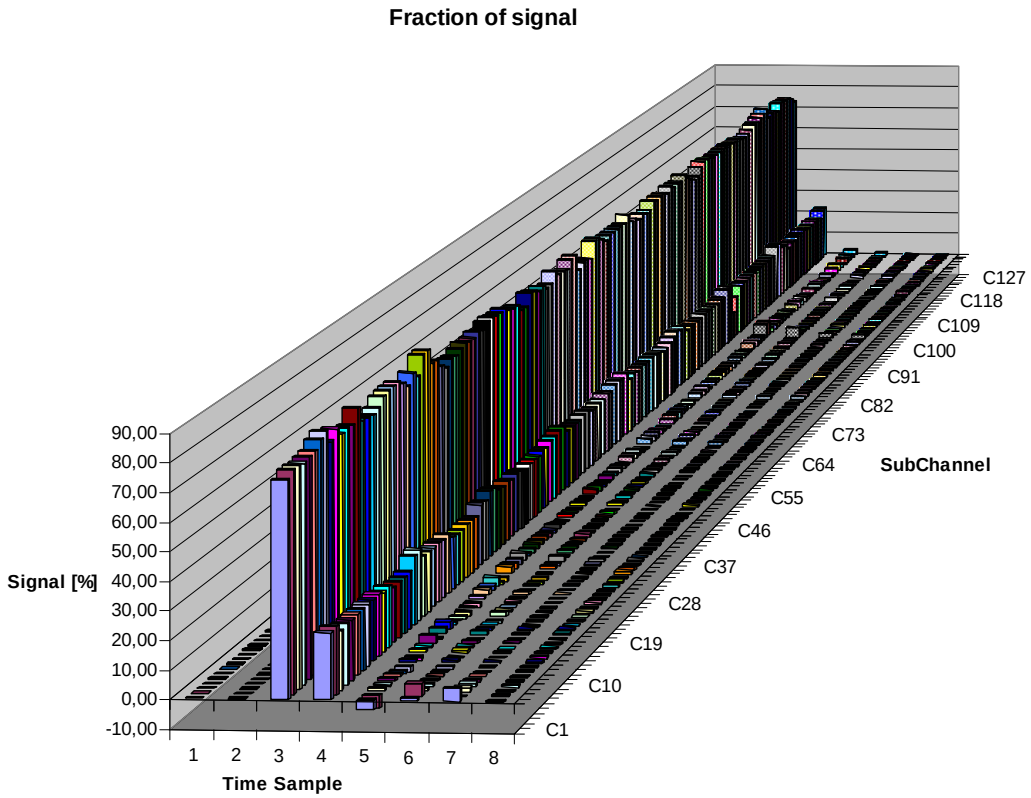

Figure 6-63. Fraction of signal on 64 channels in 8 consecutive clock cycles with V_{subD}=0 mV.

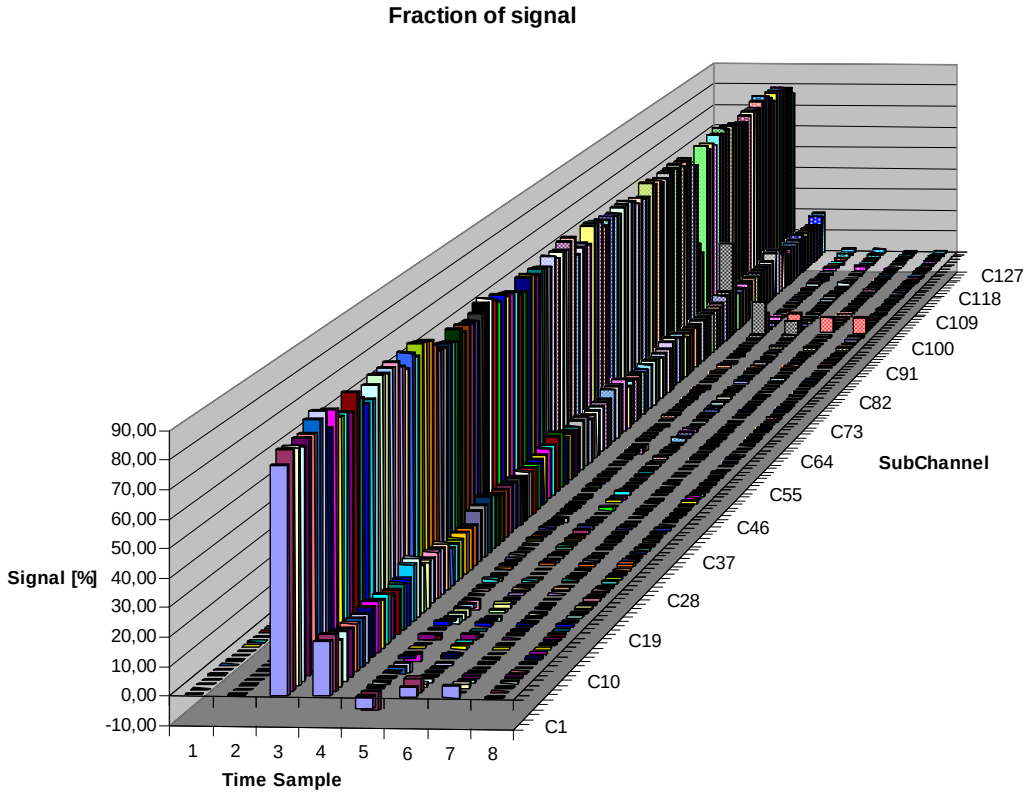

Figure 6-64. Fraction of signal on 64 channels in 8 consecutive clock cycles with V_{subD}=100mV.

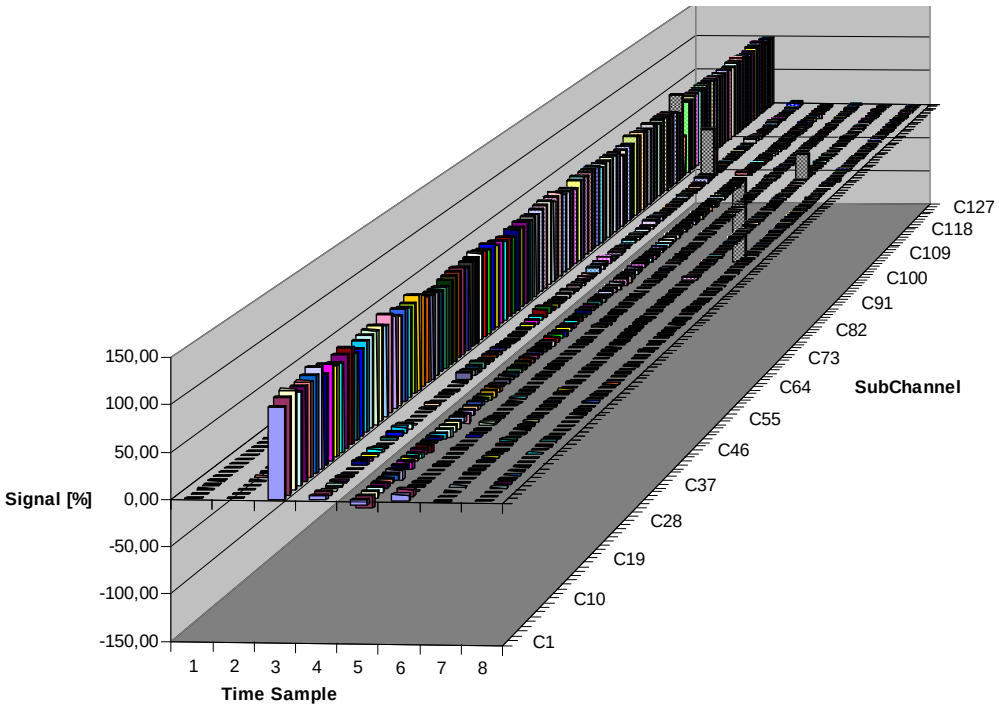

Figure 6-65. Fraction of signal on 64 channels in 8 consecutive clock cycles with V_{subD}=200mV.

6.2.5.3 Total crosstalk

The typical crosstalk is around 5% which is in good agreement with the results obtained for MaPMT test [182]. Hence we can conclude, that electrical crosstalk is negligible in front of optical crosstalk. Figure 6-66 shows a typical result for a VFE card.

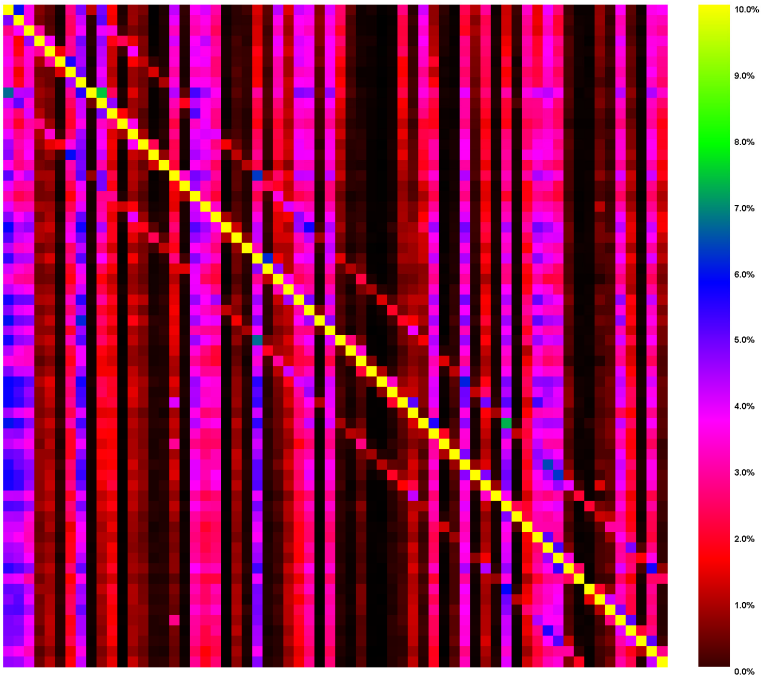

Figure 6-66. Crosstalk matrix for a VFE card.

6.2.6 Test-beam

A prototype of the card has been tested in CERN SPS test facility (X7 area) using pion and electron beams of energies up to 120 GeV. A 400 GeV/c primary proton beam is extracted from the SPS and directed on a primary target. Typical intensities of this primary beam are $2 \cdot 10^{12}$ protons per burst. From the T1 target a secondary beam is derived, called the H3 beam. Normally the H3 beam transports 120 GeV/c negative particles, mainly pions and electrons, but both the energy and polarity can be changed depending on the requirements. The H3 beam is split into two branches, each transports up to about $1.5 \cdot 10^{7}$ particles to the X5 and X7 secondary targets. The spot sizes are of the order of a few millimeters RMS in each projection.

For our tests, the beam bunch has been set on a special structure to emulate the 25 nanoseconds beam of LHC. A 25 nanoseconds clock synchronous with the beam was provided. The coincidence of two scintillator counters placed before and after the SPD cell has been used as trigger signal. The schematic of the test set up is shown in Figure 6-67.

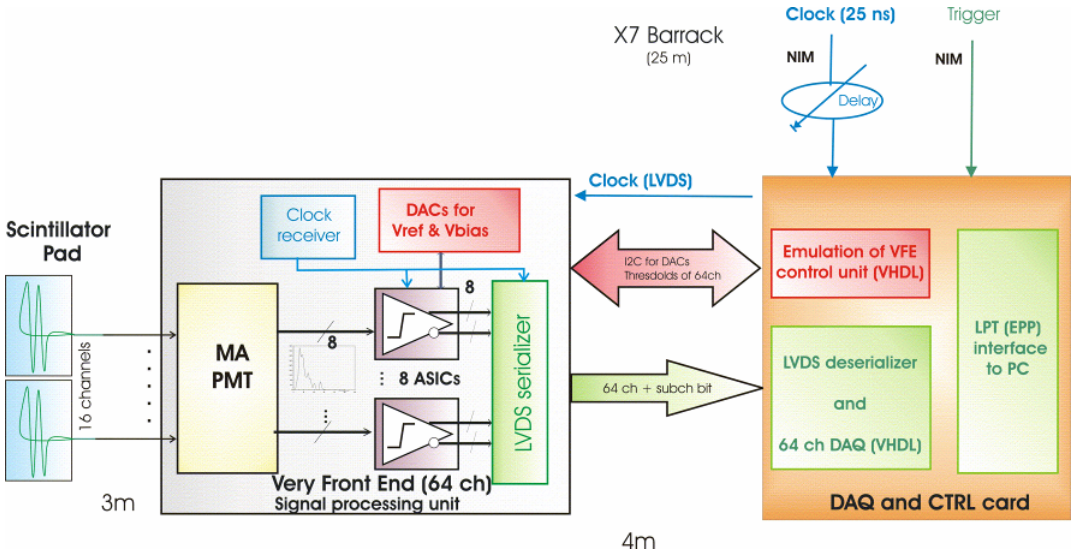

Figure 6-67. Schematic of the test set-up.

The VFE prototype with 8 ASICs and the SPD cells (a module with 4x4 outer cells) are shown in Figure 6-68. The beam has directed to the SPD cell connected to the VFE channel 18.

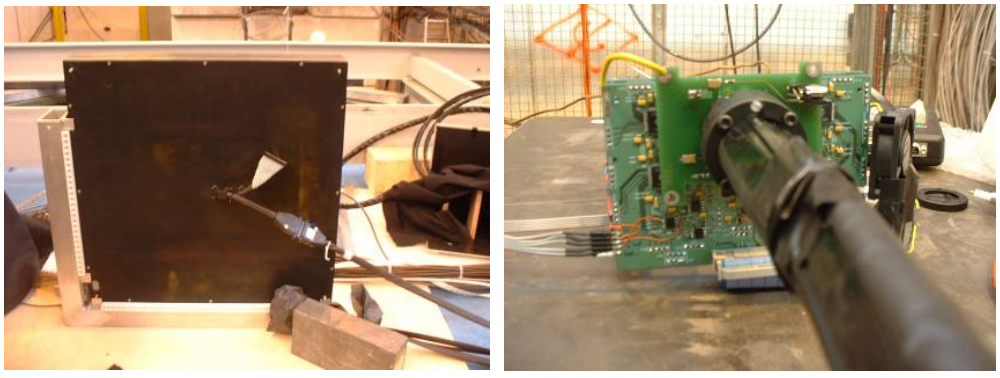

Figure 6-68. Photograph of the 4x4 SPD module (left) and of the VFE prototype (right).

First a fine phase tuning of the clock that controls integration has been performed varying the delay between this clock and the beam clock in 1 ns steps, as depicted in Figure 6-69. A clock delay of 5.5 ns was chosen.

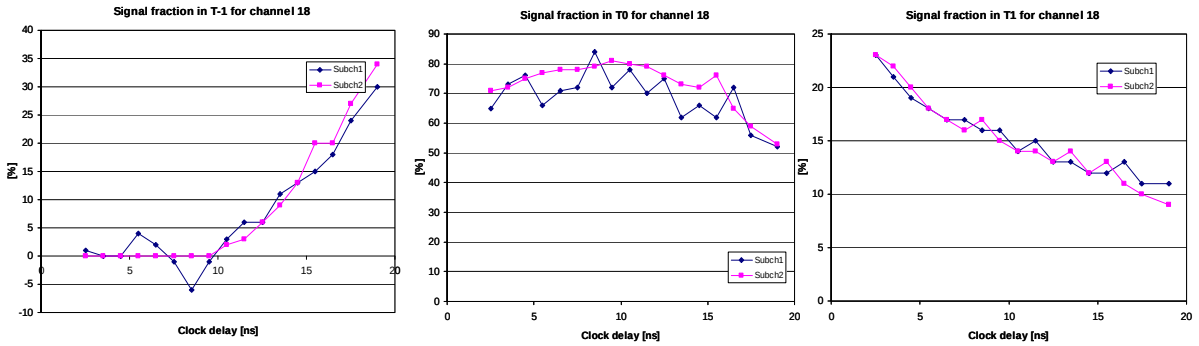

Figure 6-69. Signal fraction in three consecutive clock periods as a function clock delay. Central plot correspond to period where signal should be maximized (T=0).

First the signal shape has been measured taking 8 consecutive clock cycles for more than 1000 triggered events, results are shown in Figure 6-70. According to measurement the fraction of signal in consecutive clock cycles are T0=76%, T1=19%, T2=4% and T3=1% (T-1=0%). Input time constant τ_C is about 6 ns, see Appendix C. According to simulation results summarized in section 4.2 for τ_C = 6 ns T0=76%, T1=18%, T2=2% and T3=0% (T-1=4%). They are in agreement with test beam results.

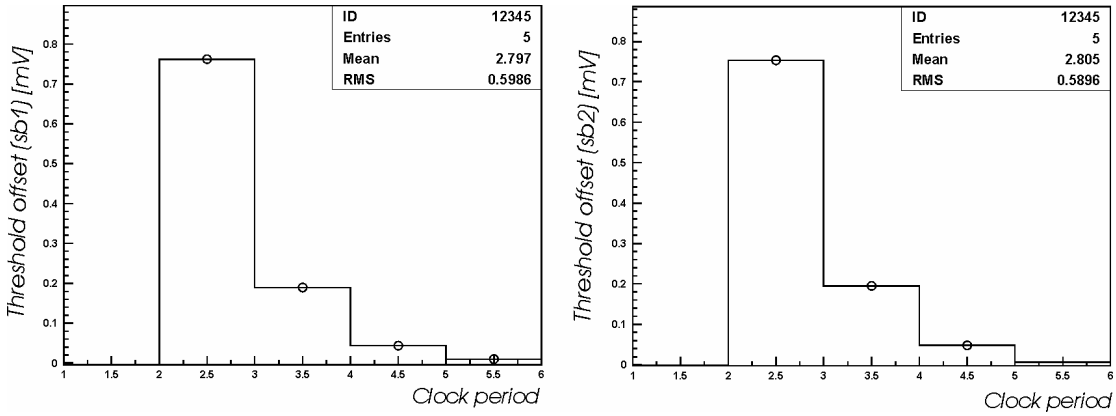

Figure 6-70. Signal fraction in 8 consecutive clocks for subchannel 1 (left) and 2 (right) of chl 18.

Differentiation of a threshold scan in T=0 yields to the MIP signal spectra Figure 6-71. The MaPMT HV is set to the nominal value (-700V). The threshold offset without signal (pedestal) is about -85 mV and the MIP signal is about 80 mV, in the expected range.

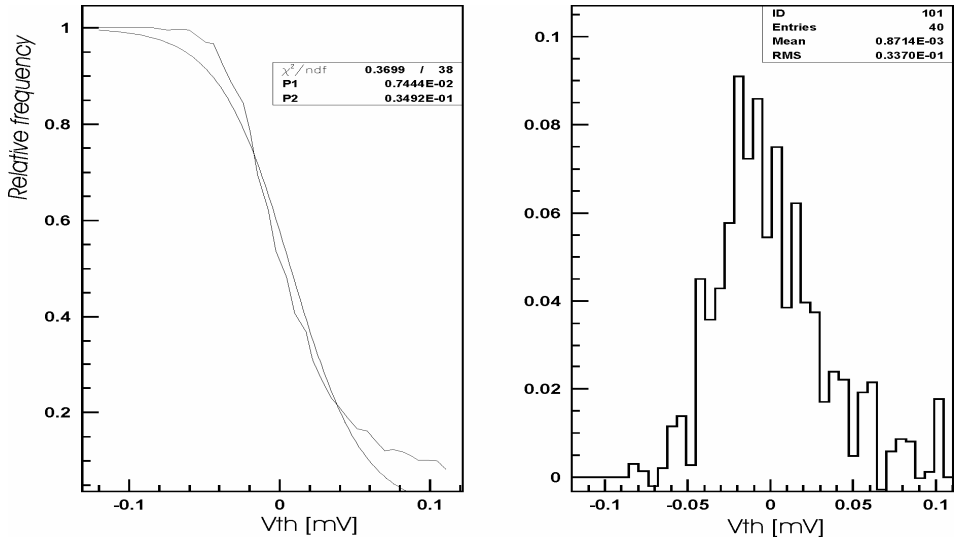

Figure 6-71. Threshold scan (left) and MIP spectra obtained through differentiation (right).

The MIP signal as a function of MaPMT HV is depicted in Figure 6-72.

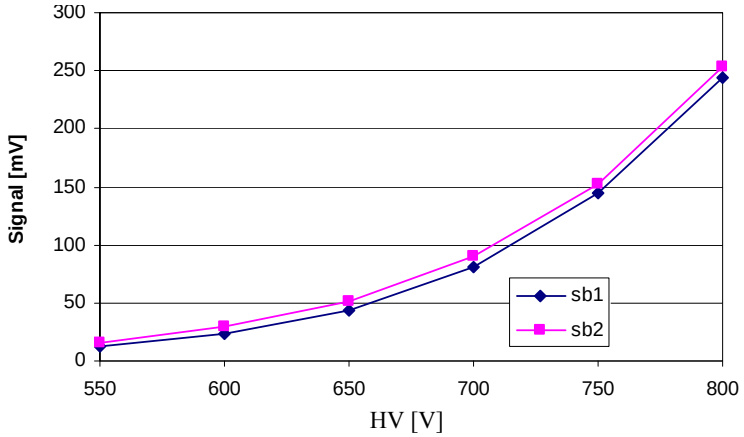

Figure 6-72. MIP signal as function of MaPMT HV.

Number of photoelectrons corresponding to the MIP signal ($nphe_{MIP}$) can be estimated from the statistics of the signal,

$$nphe_{MIP} = \left(\frac{\mu_{MIP}}{\sigma_{MIP}}\right)^2 \left(\frac{ENF}{CE}\right) \qquad (10.1)$$

As the MIP signal spills over more than one clock period,

$$nphe_{MIP} = \frac{\left(\left(\mu_{T0}-\mu_{ped}\right)+\left(\mu_{T1}-\mu_{ped}\right)+\left(\mu_{T2}-\mu_{ped}\right)+\left(\mu_{T3}-\mu_{ped}\right)\right)^2}{\left(\sigma_{T0}^2-\sigma_{ped}^2\right)+\left(\sigma_{T1}^2-\sigma_{ped}^2\right)+\left(\sigma_{T2}^2-\sigma_{ped}^2\right)+\left(\sigma_{T3}^2-\sigma_{ped}^2\right)}\left(\frac{ENF}{CE}\right) \qquad (10.2)$$

Assuming typical values for ENF=1.25 and CE=0.9, we have about 16 phe per MIP. The light yield was a bit lower than expected; problems with optical connections were identified.

Figure 6-73 shows how the tile correction system cancels on average the tail of the MIP signal.

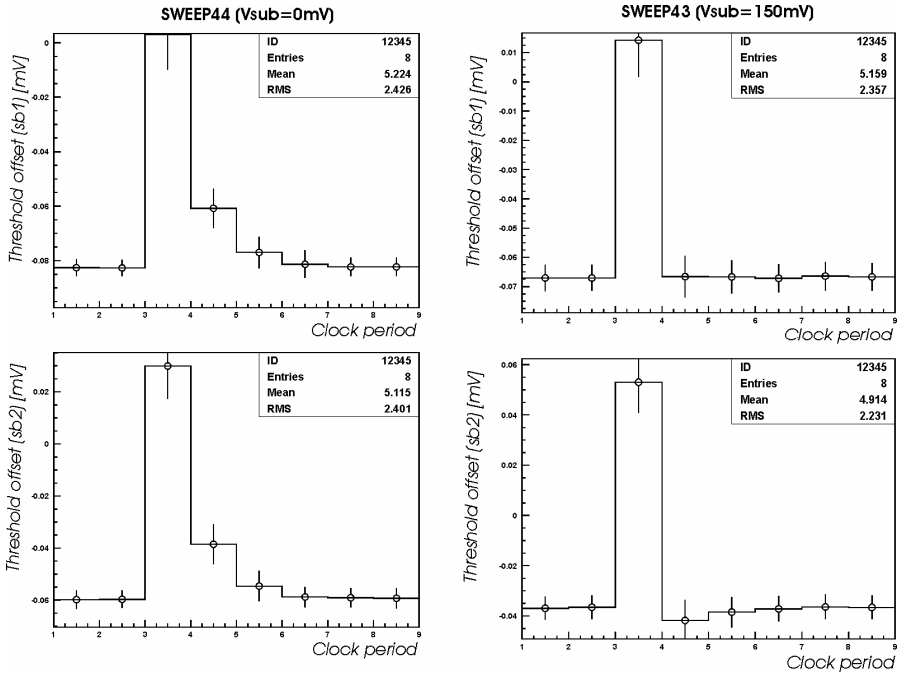

Figure 6-73. Signal in 8 consecutive clock cycles without tile correction (left) and with tile correction (right). Subchannel 1 at the top and subchannel 2 at the bottom.

The trigger efficiency as a function of the threshold has been measured comparing the counting frequency (number of 1s) to the external trigger signal, Figure 6-74. Trigger efficiency (ones in T=0) is about 93 % and fake trigger ratio (ones in T=1) is 1 % for a threshold of 0.5 MIP. Of course, a better light yield would improve trigger efficiency.

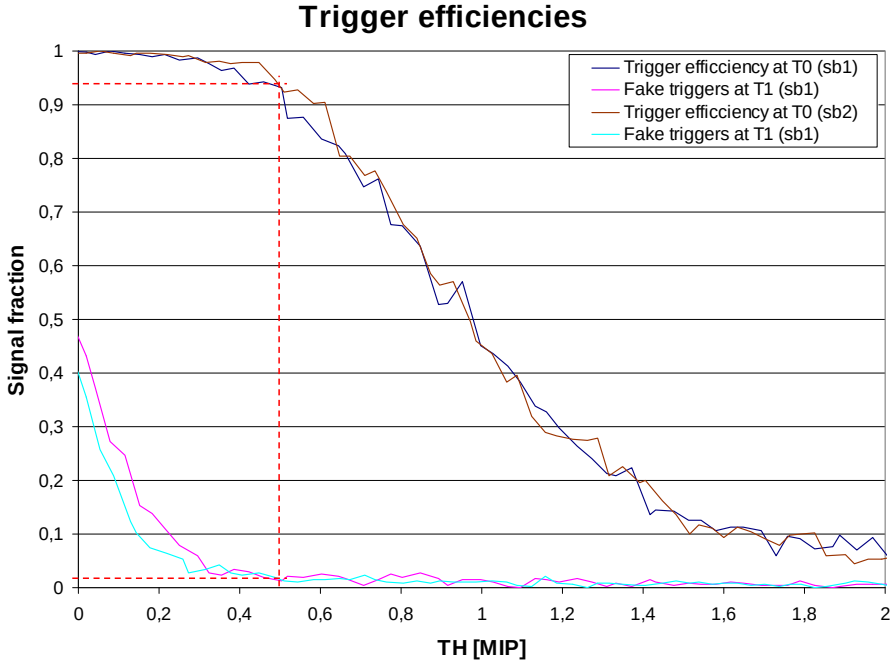

Figure 6-74. Trigger efficiency and fake trigger ratio as function of threshold..

6.2.7 Burn in and temperature dependence of noise and offset

The reliability of a component or product can be depicted by the familiar bathtub curve [175]. The bathtub curve is failure rate versus time. It has three regions: the early failures known as infant mortalities, the normal life failures where the reliability is usually the highest (lowest level of failures), and the wear out failures where reliability decreases and consequently failures increase. The goal is to remove all infant mortalities and deliver product to the customer which is in the normal life failure rate. Stress testing, also called burn-in or accelerated life test, was developed in order to shorten the length of time required to test components and sort out the potential early failures. Some of the ways to condense the stress are to exercise the component more frequently, raise or lower the operating temperature during operation, raise or lower the humidity, vibrate or shock the component, exercise the component with abnormal operating voltages and current, and many other adverse conditions and combinations of these intended to increase the stress in a short period of time compared to normal operating conditions, so as to mimic normal operating conditions for a long period of time.

A total of 9 burn-in cycles of about 8 hours between 0 to 50 º C have been performed in a climatic chamber to the VFE pre-series cards (10 cards) and no problematic component has been identified. During the cycles a card was continuously monitored; the logic was functional and the noise and the offset were varying with the temperature as expected.

Figure 6-75 shows the evolution of the threshold offset of the 64 channels of a VFE card during burn in. The offset of the preamplifier and the gain of the ASD chain have a non negligible TC as seen in section 5.2.3, this is clearly visible in Figure 6-75. Nevertheless, the off-chip electronics (DACs, OPAs, etc) have also a non-negligible TC and a numerical comparison with the TC of the ASIC offset has no sense. The extreme plateaus correspond to 50 ºC and 0 ºC, and the intermediate one to 30 ºC.

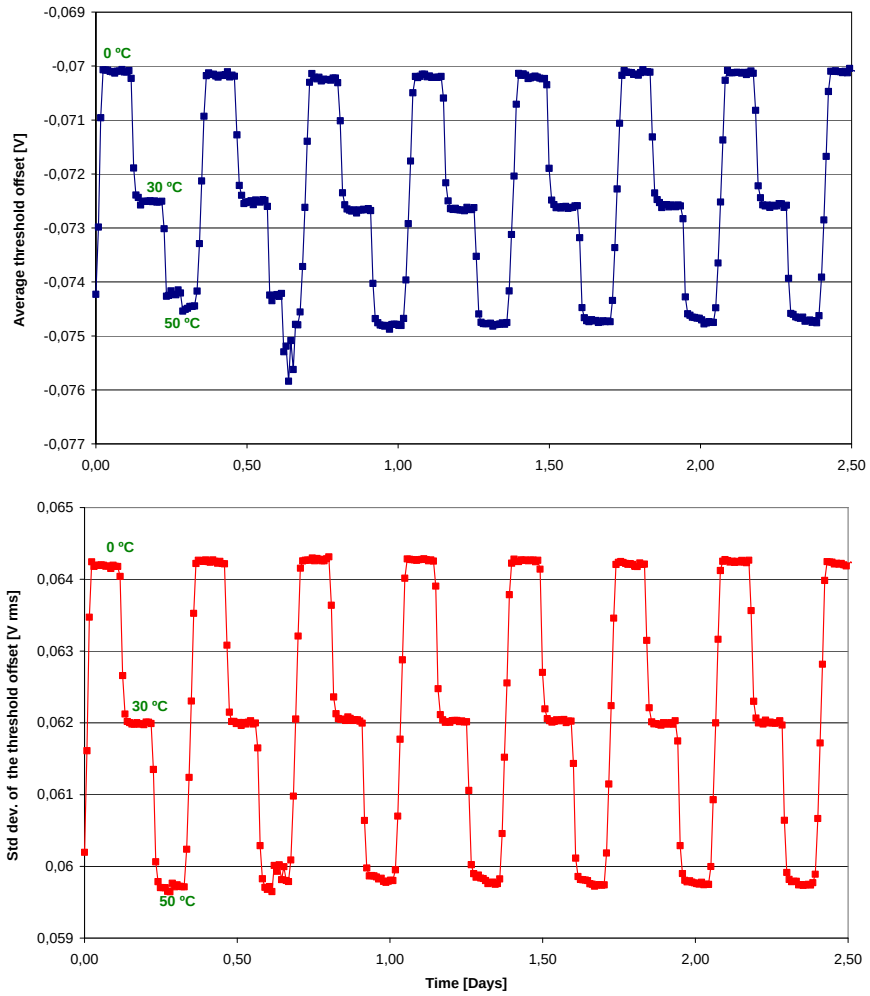

Figure 6-75. Evolution of the average (top) and standard deviation (bottom) of the threshold offset of the 64 channels of a VFE card during burn in.

The Figure 6-76 shows the evolution of the average noise in the same VFE card.

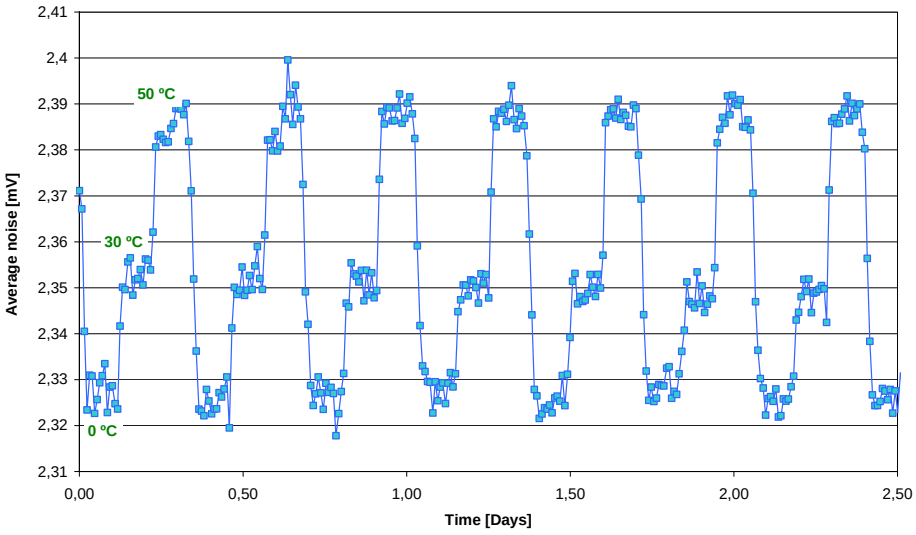

Figure 6-76. Evolution of the average noise in a VFE card during burn in.

As most of the noise of the VFE card is in origin thermal noise, the evolution of the noise tracks the evolution of the ambient temperature. Assuming that the noise depend as $\sqrt{Temp}$ a variation from 270 K to 320 K should represent an increase of an 8% (about 200 µV) of the noise. Such an increase is visible in some channels, but it is not in some others. It is probably hidden by pick-up noise affecting those channels. The resulting average increase is, , smaller than expected.

The same burn in procedure has been repeated for the VFE series (120 cards); about the 3 % of the cards presented some problem after the burn-in. Most problems where related to failures in one ASIC channel.

6.2.8 Pedestal stability

The short term stability of the pedestals or threshold offsets has been measured in different scenarios. In Figure 6-77 the results for the test bench of Figure 6-58 are shown. The pedestal short term stability for 10 hours of operation is better than 2 mV once the temperature is stable. The effect of the warm-up of the card is visible at the beginning (encircled). This kind of test has been repeated at the LHCb detector with proper cooling obtaining stability results better than 1 mV.

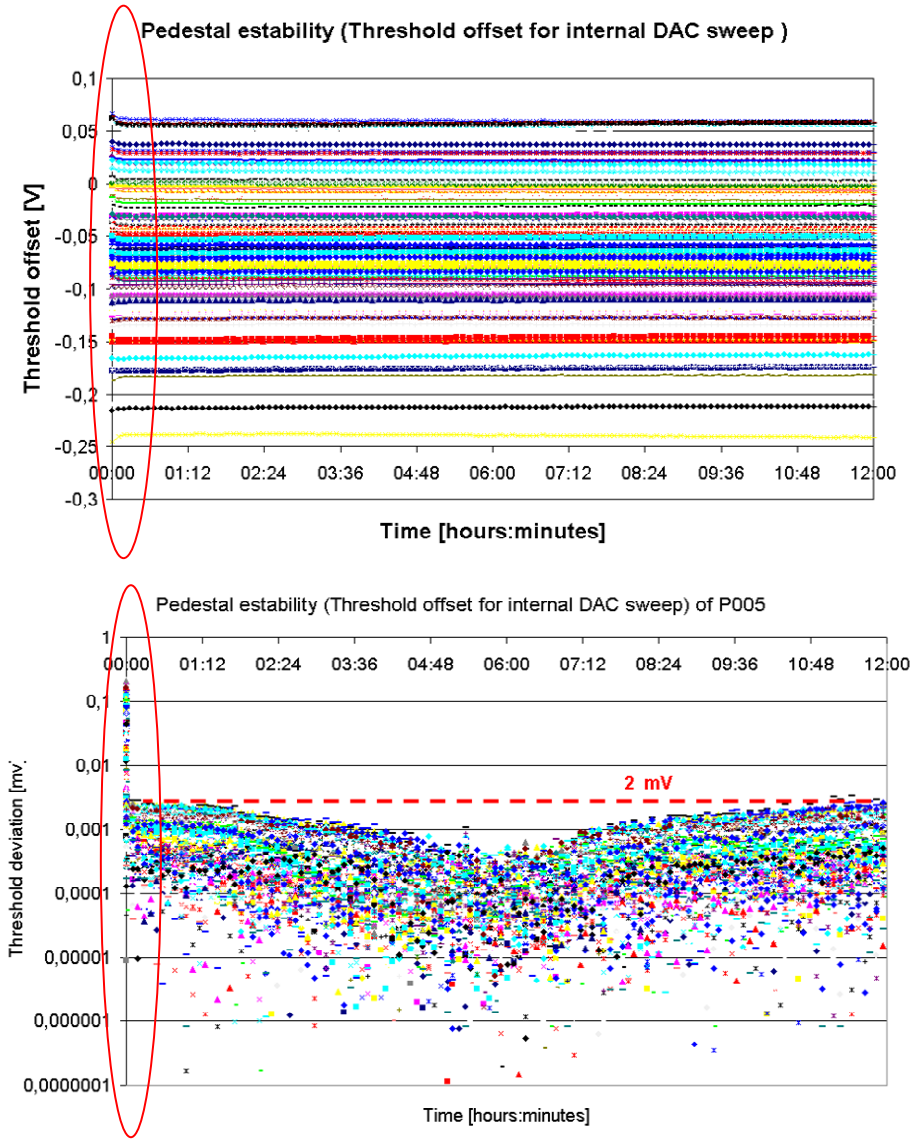

Figure 6-77. Short term pedestal stability. Top: thresholds offset. Bottom: th offset fluctuation.

6.2.9 Radiation qualification

During 2003, the 1-channel prototype version of the ASIC was irradiated with heavy ions. The experiment was carried in the Gran Accelerateur National d'Ions Lourds (GANIL) in Caen in combination with the LAL and the LPC. This procedure provides the advantage that the incident particle is directly the ionising fragment, which makes this irradiation more efficient in front of the irradiation with protons, where the ionising fragments capable of triggering a SEE are due to the interaction between incident proton and the Silicon nuclei. The measurements study the combined effect of displacement damage, total ionising dose damage and single event effects. With this method, the two first effects are not distinguishable since both appear as remaining effect once the exposure has finished, affecting the typical static and dynamic parameters of the chip.

The SEU cross section measured is plotted in the Figure 6-78, where the fitted Weibull approximation is also shown.

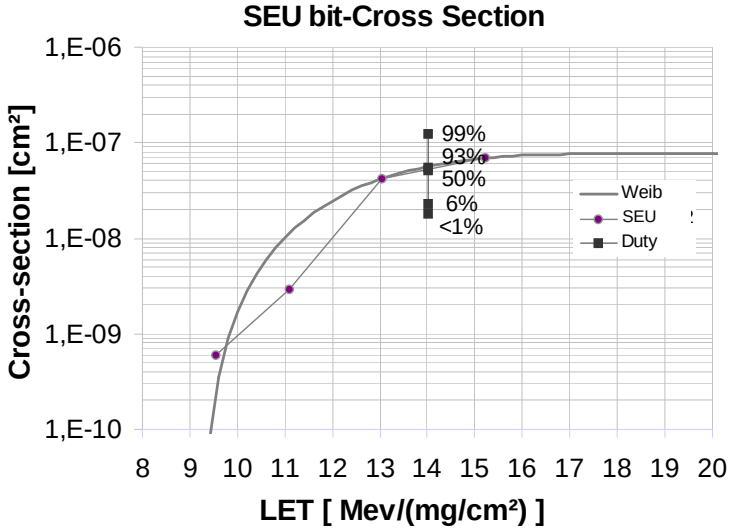

Figure 6-78. SEU Cross section for the digital circuit of the ASIC.

Summing up over the various ion species that can be obtained by collisions the maximum probability gives a result of $1.0148 \cdot 10^{-13}$ SEU.cm^2/neutron. From the previous calculus where we get the estimation of $4.2 \cdot 10^9$neutrons$\cdot$cm$^{-2}\cdot$year^{-1} we can conclude, considering that there will be 6400 channel in the detector that will have a 2.73 = 3 SEU/year, that is a very satisfactory result. Relative to the Single Event Latch-up effect and for a maximum LET of 15 MeV$\cdot$cm$^2\cdot$mg^{-1} foreseen in the LHCb none has been detected and so that with a limit of confidence of 90% the probability to find a SEL is one each 20 years, and can be considered as qualified since 10 years is the estimated LHCb lifetime.

Regarding the accumulative effects considering both together, TID and NIEL, the device kept its functionality correct after irradiation. For 10 years of operation of LHCb, the maximum dose is 58 Gy and the average one is 35 Gy, values that include the uncertainty simulation, the only safety factor that has to be considered is the component to component variation (2) and the own test uncertainty, as the ASICs will be manufactured in the same line and as sole serial. Applying such factors, we obtain a maximum of 232 Gy and an average of 140 Gy, values widely exceeded in the test where it has been accumulated a dose from 237 Gy to 459 Gy, covering broadly the margins. No degradation on any performance was observed after irradiation.

Bipolar transistors are used extensively in the design. One might be concerned about displacement damage, because the chip has not been tested directly with neutrons. Due to the fact that we have used relatively fast vertical bipolar transistors it can be expected that they will not suffer significant displacement damage in the relatively moderate environment in the SPD detector ($5 \cdot 10^{11}$ neutrons/cm^2 in 10 years). In [184] the results of a neutron test of a chip made in 1.2 µm BiCMOS technology are

reported. No effects were seen up to a fluence of $7 \cdot 10^{13}$ neutrons/cm^2. Since going to 0.8 µm should make the chip even less sensitive to neutrons and because the design does not depend on a critical way on the exact beta value, thanks to the emitter degeneration extensively used, it was not considered necessary to invest in a specific neutron test.

A more comprehensive description of test and discussion of the results can be found in [185] and [186].

6.2.10 Back-annotation

6.2.10.1 Electrostatic discharge (ESD)

A variation in the offset of some prototypes was observed. After exhaustive tests it has been found that the gain of the tail correction system changed also. After discarding other possible causes, the hypothesis of an ESD problem has been formulated. Basic pads with no protection were used for the V_{bias} control signal of the tail correction system.

A typical circuit to model human body ESD is shown in Figure 6-79.

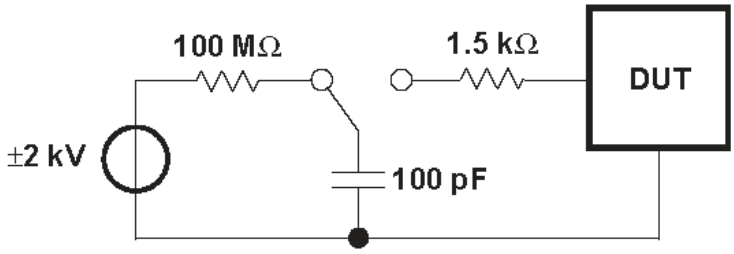

Figure 6-79. Human-body model test circuit.

A systematic series of 2 kV discharges have been applied on several channels. First a discharge on V_{biasH} was applied, then two discharges on V_{biasL}. With the first discharge the gain decreased and with the second and the third ones it increased again. The gain of four tail correction blocks before and after the discharges is shown in Figure 6-80.

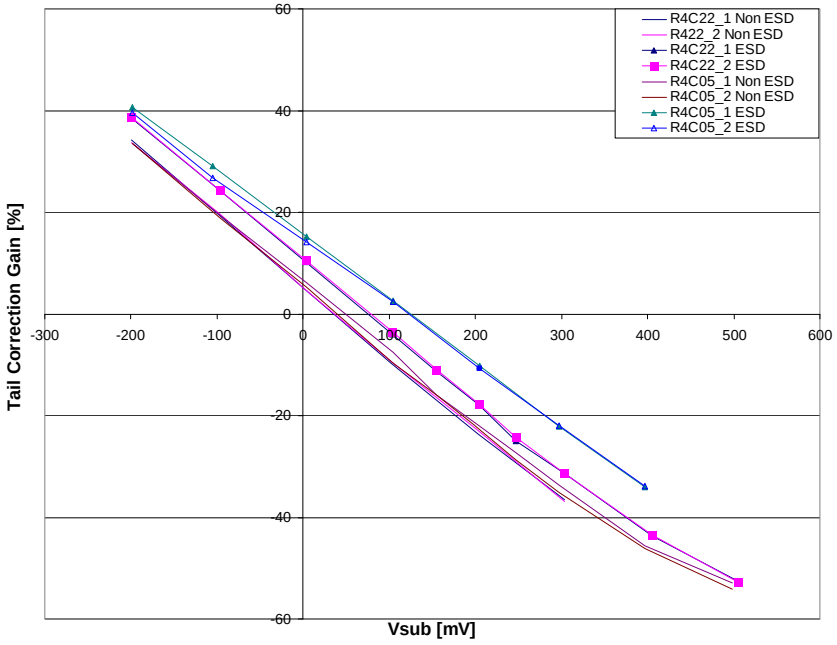

Figure 6-80. Effect of the ESD on the tail correction gain.

In following prototypes pads with ESD protection from the library of Austriamicrosystems [160] have been used for all the IOs. The ESD test has been repeated for the most sensitive pads (Vsub, Vref and inputs) and no effect has been found.

6.2.10.2 Problems with Austriamicrosystems Monte Carlo models

On first prototypes, a serious disagreement between Monte Carlo simulations results and offset measurements was detected. The problem was confirmed with the colleagues of the LPC at Clermont Ferrand who were using the same technology. After reporting the problem to Austriamicrosystems, correct models have been provided (HitKit_3.31 ENG#124 REV_2).

6.2.10.3 Gain corrections

As reported in previous sections, measurement often provide second order corrections to the value of the gain or other relevant parameters calculated with first order models or even simulated. However, it is important to take into account that measurement artifacts also introduce errors on those values (for instance, the effect of the output buffer reported in some of the block measurements). For this reason, measurement performed on the full ASD chain is of prominent importance.

7 Conclusions

7.1 Main achievements

An ASIC for the front end electronics of the SPD has been designed, produced and tested. The ASD architecture of the circuit is well adapted for high luminosity experiments where no dead time is allowed and where collection time of the signal is comparable to the bunch crossing period. We would like to remark some key characteristics of the analogue processing that are essential to achieve this goal:

- The flat top of the gated integrator shaping is very useful to minimize the effect of ballistic deficit in such situations where ballistic deficit is relevant.
- The use of two interleave sub-channels avoids any dead time.
- This allows also to perform pile-up correction in a complete VLSI design manner, without external components.
- All the analogue blocks are DC coupled to avoid any baseline shift. A fast return to the baseline is achieved thanks to the switched integration.
- The use of differential circuitry is ideal to get rid of the problems related to signal integrity on switched systems.

The requirements for the SPD have been achieved: noise below 2 fC r.m.s, dynamic range of 9 bits, linearity error below 1% and pile up correction system. This block is a fully differential circuit based on topology not previously reported.

Radiation tolerance for the LHCb environment is achieved following some design strategies:

- Extensive usage of feedback to minimize the effect of beta degradation on bipolar transistors. Even the stages we consider as “open loop” stages rely on differential pairs with emitter degeneration, which acts as a local feedback.
- Prevention of single event latch up through guard rings where CMOS circuits are present.
- Majority voting between triple redundant integrated circuits is used in order to provide a SEU hardened logic.

The design of the ASIC is not merely a “proof of principle”; more than 1000 units have been produced and tested. In that sense, the study of the effect of the parameter variability has a paramount importance to achieve an acceptable yield, about the 80% in this case. In addition to functional characterization, many different tests and checks have been performed: tests on complex systems in different environments, burn in cycles in a climatic chamber, radiation tests and ESD tests.

We would like also to point out some methodological achievements. In first place, a method to study the PSRR (and any transfer function) in fully differential circuits taking into account the effect of parameter mismatch has been proposed [171]. Concerning noise analysis, a method to study time variant circuits in the frequency domain has been presented and justified. This opens the possibility to study the effect of *1/f* noise in time variant circuits if the method and its theoretical justification presented in this work are accepted. We think it is worthwhile to point out, that this would be an important achievement as reference publications in the field tend to discard the frequency domain analysis for time variant shapers ([94], [126]).

7.2 Possible improvements and outlook

As said above, the ASD architecture presented here is optimal for high luminosity experiments, with a bunch crossing period comparable to the collection time of some detectors, and when the occupancy of those detectors is high. Thus, it is thinkable to study the use of such a system in SLHC, as one option for the upgrade of the LHC is to reduce the bunch crossing period to 12.5 nanoseconds and scintillating, gaseous detectors or even silicon detectors where charge is collected by diffusion often exhibit comparable or longer collection times. On a larger time-scale, even shorter bunch crossing times are considered, for instance 1 nanosecond for the current CLIC design [188].

For future applications of this ASD architecture, very deep submicron technologies will have to be used. On these technologies the parameter variability and the *1/f* noise are crucial issues. Nevertheless, the methods presented here to study the effect of mismatch in fully differential circuits and to analyze time variant networks in the frequency domain, should provide a tool to face this challenge.

Possible improvements in the circuit should probably start by transforming the input stage to a current mode version, as in [190], [191] and [192]. Signal of most detectors can be modeled as a current source, thus it would natural to think on a low impedance current input. In addition, a low impedance input is interesting to minimize the capacitive coupling (crosstalk and pick up noise). Second step would be trying to reduce the ENC of the circuit, so it could be used with APDs or other silicon or gaseous detectors. Then, it is possible to think on using such architecture for tracking or for calorimetry, replacing the discriminator by and ADC.

More ambitious future lines can be envisaged. It has been shown that it is possible to fabricate single photon counting devices with commercial CMOS technologies [189]; then, it could be possible to integrate this ASD together with a Silicon Photomultiplier.

According to our experience regarding the realibility of complex multichannel systems such LHCb, it would be useful to integrate as much as possible the control or interface electronics surrounding the chip, that is to say to go for a System on Chip solution.

Some groups are also investigating the possibility to fabricate LEDs with CMOS technologies; if a solution is found this would open the possibility to have ASICs in standard CMOS technologies with optical outputs. The “dream” could be integrate the typical full front end system in a single die, from the Silicon Photomultiplier or radiation sensor, to the LED that drives the optical fibre to transmit the information to DAQ system.

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List of abbreviations

Abbreviation	Meaning
AC	Alternating Current
ADC	Analog to Digital Converter
APS	Active Pixel Sensor
ASD	Amplifier Shaper and Discriminator
ASIC	Application Specific Integrated Circuit
AWG	Arbitrary Waveform Generator
BiCMOS	Bipolar and CMOS technology
BJT	Bipolar Junction Transistor
BW	Bandwidth
CB	Control Board
CE	Collection Efficiency
CERN	European Laboratory for Particle Physics
CLIC	Compact Linear Collider
CM	Common Mode
CMFB	Common Mode Feedback
CMOS	Complementary Metal Oxide Semiconductor
CMRR	Common Mode Rejection Ratio
CTAT	Complementary to absolute temperature
DAC	Digital to Analogue Converter
DAQ	Data Acquisition
DC	Direct Current
DEPFET	Fully Depleted Field Effect Transistor
DM	Differential Mode
DNL	Differential Non-Linearity
DSM	Deep Sub-Micron
ECAL	Electromagnetic Calorimeter
ECL	Emitter Coupled Logic
ECS	Experiment Control System
ENC	Equivalent Noise Charge
ENF	Excess Noise Factor
ESD	Electrostatic Discharge
FE (FEB)	Front End (Front End Board)
FDOA	Fully Differential Op Amp
FPGA	Field Programmable Gate Array

FWHM	Full Width Half Maximum
GANIL	Gran Accelerateur National d'Ions Lourds
g_m	Transconductance
GBW	Gain-Bandwidth (product)
HCAL	Hadronic Calorimeter
HEP	High Energy Physics
HLT	High Level Trigger
HPD	Hybrid PhotoDiode
HV	High Voltage
ILC	International Linear Collider
INL	Integral Non-Linearity
IO	Input-Output
IT	Inner Tracker
IZE	Input Zero Error
JFET	Junction Field Effect Transistor
KCL	Kirchoff´s Current Law
KVL	Kirchoff´s Voltage Law
L0	Level 0 trigger
LAL	Laboratoire de l'Accélérateur Linéal
LED	Light Emitting Diode
LET	Linear Energy Transfer
LHC	Large Hadron Collider
LHCb	Large Hadron Collider beauty experiment
LPC	Laboratoire de Physique Corpusculaire
LSB	Least Significant Bit
LVDS	Low Voltage Differential Signaling
MAP	Monolithic Active Pixel
MaPMT	Multi-anode photomultiplier
MIP	Minimum Ionizing Particle
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MWPC	Multi Wire Proportional Chamber
NIEL	Non-Ionising Energy Losses
OT	Outer Tracker
OpAmp (OPA)	Operational Amplifier
OZE	Output Zero Error
PCB	Printed Circuit Board
PM	Phase Margin
PMT	Photomultiplier
PS	Preshower
PSD	Power Spectral Density
PSRR	Power Supply Rejection Ratio
PTAT	Proportional to absolute temperature

RHP	Right Half Plane
r_i	Input resistance
RICH	Ring Imaging Cherenkov detector
r_o	Output resistance
r.m.s.	Root Mean Square
R_S	Source resistance
SPD	Scintillator Pad Detector
SEE	Single Event Effect
SEL	Single Event Latch Up
SEU	Single Event Upset
SiPMT	Silicon Photomultiplier
SLHC	Super Large Hadron Collider
SNR	Signal to Noise Ratio
SPECS	Serial Protocol for Experiment Control System
SPS	Super Proton Synchrotron
Std. dev.	Standard deviation
SR	Slew Rate
TC	Temperature Coefficient
TFC	Timing and Fast Control system
TH (T&H)	Track and Hold
TID	Total Ionizing Dose
TQFP	Thin Quad Flat Package
TT	Trigger Tracker
TVR	Triple Voting Register
V_A (VAF)	Early voltage
VELO	Vertex Locator
VFE	Very Front End
VLSI	Very Large Scale of Integration
XTALK	Crosstalk
WLS	WaveLenght Shifting Fibre

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A Appendix: calculation of device parameters.

Some general considerations on using the models have to be taken into account. The multiplication factor (*M*) puts m devices in parallel; *m* is an instance parameter and need not be an integer. All devices have the multiplication factor capability.

If you specify *M* in an instance statement, all currents and capacitances of that device are multiplied by m, and all resistances are divided by m. The multiplication factor, however, does not affect short-channel or narrow-gate effects in MOSFETs.

Some devices—such as BJT, JFET, and diode—have an area factor parameter (*AREA*). The area parameter has identical effect on devices as the multiplication factor. Important process parameters of the AMS 0.8 μm BiCMOS technology are summarized in [73].

A.1 Front End Amplifier

The BJT model based on the Berkeley-Spice Gummel-Poon model of Spectre Simulator [163] will be used for hand calculations too. The device parameters are obtained from the HSPICE models for the AMS BICMOS 0.8μm technology [164].

A.1.1 Base-Emitter Depletion capacitance for Q1-Q2

According to [165] the base-emitter depletion capacitance C_{je} for a forward biased junction (transistor in active region) can be computed as $C_{je} = CJE_{eff}\left(1 + MJE\frac{vbe}{VJE}\right)$ where $CJE_{eff} = CJE \cdot M \cdot AREA$, using information of [73], then CJE_{eff}= 39 fF and C_{je} = 56 fF

A.1.2 Base-Collector Depletion capacitance for Q1-Q2

According to [165] the base-collector depletion capacitance C_{jc} for a reverse biased junction (transistor in active region) can be computed as $C_{jc} = XCJC \cdot CJC_{eff}\left(1 - \frac{vbc}{VJC}\right)^{-MJC}$ where $CJC_{eff} = CJC \cdot M \cdot AREA$, using information of [73], then CJC_{eff}= 66 fF and C_{jc} = 12 fF.

A.1.3 Substrate-Collector capacitance for Q1-Q2

According to [165] substrate-collector depletion capacitance C_{js} for a reverse biased junction (always for substrate) can be computed as $C_{js} = CJS_{eff}\left(1 - \frac{vsc}{VJS}\right)^{-MJS}$ where $CJS_{eff} = CJS \cdot M \cdot AREA$, using information of [73], then CJS_{eff}= 180 fF and C_{js} = 113 fF.

A.1.4 Base Resistance for Q1-Q2

According to [67] $r_b = RBM_{eff} + (RB_{eff} - RBM_{eff})\left(\Big/ 1 + \frac{I_C}{IKF_{eff}} \right)$ where $RBM_{eff} = \frac{RBM}{AREA \cdot M}$, $RB_{eff} = \frac{RB}{AREA \cdot M}$ *and* $IKF_{eff} = IKF \cdot M \cdot AREA$.Using information of [73], RBM_{eff}=4,2 Ω and RBM_{eff}=100 Ω.The collector current I_C for is about 0.5e-3 A and the value of base resistance r_b is 180 Ω.

A.1.5 Substrate-Collector capacitance for the transistors of the current source

According to [165] substrate-collector depletion capacitance C_{js} for a reverse biased junction (always for substrate) can be computed as $C_{js} = CJS_{eff}\left(1 - \frac{vsc}{VJS}\right)^{-MJS}$ where $CJS_{eff} = CJS \cdot M \cdot AREA$, using information of [73], then CJS_{eff}= 480 fF and C_{js} = 350 fF.

A.1.6 Base-Collector Depletion capacitance for the transistors of the current source

According to [165] the base-collector depletion capacitance C_{jc} for a reverse biased junction (transistor in active region) can be computed as $C_{jc} = XCJC \cdot CJC_{eff}\left(1 - \frac{vbc}{VJC}\right)^{-MJC}$ where $CJC_{eff} = CJC \cdot M \cdot AREA$, using information of [73], then CJC_{eff}= 420 fF and C_{jc} = 100 fF.

A.2 Integrator

A.2.1 Substrate-Collector capacitance for the transistors of the current source of the input stage

According to [165] substrate-collector depletion capacitance C_{js} for a reverse biased junction (always for substrate) can be computed as $C_{js} = CJS_{eff}\left(1 - \frac{vsc}{VJS}\right)^{-MJS}$ where $CJS_{eff} = CJS \cdot M \cdot AREA$, using information of [73], then CJS_{eff}= 180 fF and C_{js} = 130 fF.

A.2.2 Base-Collector Depletion capacitance for the transistors of the current source of the input stage

According to [165] the base-collector depletion capacitance C_{jc} for a reverse biased junction (transistor in active region) can be computed as $C_{jc} = XCJC \cdot CJC_{eff}\left(1-\frac{vbc}{VJC}\right)^{-MJC}$ where $CJC_{eff} = CJC \cdot M \cdot AREA$, using information of [73], then CJC_{eff}= 160 fF and C_{jc} = 40 fF.

A.3 Fully differential OpAmp

A.3.1 Small signal parameters

In this section we will compute small signal parameters of some transistors of the FDOA. The value of the areas and the quiescent currents in FDOA transistors is indicated in Table (app) 1.

Device	Size		Current	
	Area	Multiplier	Name	Value [μA]
$Q_{1(d)}$	3 (3·L0)	2	$I_{CQ1(d)}$	116
$M_{2(d)}$	W= 60 μm L = 1,5 μm	1	$I_{DM2(d)}$	33
$M_{3(d)}$	W= 10 μm L = 1,2 μm	1	$I_{DM3(d)}$	33
$M_{4(d)}$	W= 10 μm L = 1,2 μm	1	$I_{DM4(d)}$	33
$M_{5(d)}$	W= 40 μm L = 1 μm	1	$I_{DM5(d)}$	150
$Q_{6(d)}$	3 (3·L0)	2	$I_{CQ6(d)}$	40
$Q_{7(d)}$	3 (3·L0)	2	$I_{CQ7(d)}$	120
$Q_{8(d)}$	3 (3·L0)	2	$I_{CQ8(d)}$	350
$Q_{9(d)}$	3 (3·L0)	2	$I_{CQ9(d)}$	150
$M_{10(d)}$	W= 40 μm L = 1 μm	1	$I_{DM10(d)}$	150
$M_{b4(d)}$	W= 120 μm L = 1 μm	1	$I_{DMb4(d)}$	80

Table (app) 1. Areas and quiescent currents of FDOA transistors.

Table (app) 2. shows the value of device parameters of some transistors, indicating the expression used to compute the small signal parameter. Parameters are calculated for a temperature of 300 K.

For the bipolar transistors:

- Early voltage (V_A) is calculated as in the Spice models used for the simulation for the npn 121 bipolar transistors.
- The forward current gain β is calculated as in the Spice models used for the simulation for the npn 121 bipolar transistors.

For the MOS transistors see [73]. The source of PMOS transistors is connected to the bulk to avoid body effect. Body effect is neglected for NMOS transistors.

Device	Parameter (with expression)	Value
Q_1	Transconductance: $g_{mQ1}=I_C/(k(T/q))= I_C/V_T$	4.46 mA/V
Q_1	Output resistance : $r_{oQ1}=V_A/I_C$	328 kΩ
M_2	Transconductance (strong inversion) : $g_{mM2}=(2I_DK_{PP}(W/L))^{1/2}$	0.3 mA/V
M_2	Output resistance : $r_{oM2}=1/\lambda_P I_D$[y]	150 kΩ
M_3	Transconductance (strong inversion) : $g_{mM2}=(2I_DK_{PN}(W/L))^{1/2}$	0.23 mA/V
M_3	Output resistance : $r_{oM3}=1/\lambda_N I_D$	300 kΩ
M_4	Output resistance : $r_{oM4}=1/\lambda_N I_D$	300 kΩ
M_5	Output resistance : $r_{oM5}=1/\lambda_P I_D$	33 kΩ
Q_6	Transconductance: $g_{mQ6}=I_C/(k(T/q))= I_C/V_T$	1,5 mA/V
Q_6	Input resistance : $r_{\pi Q6}=\beta/g_m$	90 kΩ
Q_7	Transconductance: $g_{mQ7}=I_C/(k(T/q))= I_C/V_T$	4.46 mA/V
Q_7	Input resistance : $r_{\pi Q7}=\beta/g_m$	30 kΩ
Q_7	Output resistance : $r_{oQ7}=V_A/I_C$	328 kΩ
Q_8	Transconductance: $g_{mQ8}=I_C/(k(T/q))= I_C/V_T$	9 mA/V
Q_8	Input resistance : $r_{\pi Q8}=\beta/g_m$	15 kΩ
Q_8	Output resistance : $r_{oQ8}=V_A/I_C$	115 kΩ
M_{b4}	Output resistance : $r_{oMb4}=1/\lambda_P I_D$	60 kΩ

Table (app) 2. Small signal parameters of some FDOA transistors.

A.3.2 Gate to source and drain to source capacitances of MOS transistors in saturation

In saturation region the gate to source capacitance (C_{gs}) of a MOS transistor is $C_{gs}=\frac{2}{3}WL_{eff}C_{ox}+WL_DC_{ox}=\frac{2}{3}WL_{eff}C_{ox}+WC_{GS0}$ and the gate to drain (C_{gd}) capacitance is only due to overlap: $C_{gd}=WL_DC_{ox}=WC_{GD0}$.

In Table (app) 3. the gate to source and drain to source capacitances of relevant transistors in FDOA are computed, using information of [73] and Table (app) 1.

[y] A first order model for r_o in MOS devices is taken, assuming typical values of λ_P=0,2 and λ_N=0,1.

Transistor	C_{gs} [fF]	C_{gd} [fF]
M_2	195	21
M_5	88	14
M_3	30	3.5
M_{b4}	260	42
M_{cas1}	285	36
M_{cas2}	150	33

Table (app) 3. Gate to source and drain to source capacitances of relevant FDOA MOS transistors.

A.3.3 Drain or source to bulk capacitances of MOS transistors

According to [169] the drain to substrate or source to substrate capacitance of a MOS transistor for a linear structure is: $C_{DB} = C_{SB} = A_{S(P)}Cj + P_{S(P)}$ Cjsw, where $A_{S(P)}$ is the area of the source or drain of the transistor and $P_{S(P)}$ is the perimeter. For a typical "linear" layout $A_{S(P)}$=WE and $P_{S(P)}$=2(W+E), where W is the channel width and E is the width of source and drain, for transistors used in this design E=2.3 μm. But the expressions to compute the area and the perimeter depend on the number of gates or fingers, the transistor layout, etc.

In Table (app) 4. the relevant C_{DB} /C_{SB} capacitances are calculated as function of transistor perimeter and area.

Name	Area [m^2]	Perimeter [m]	Value [fF]
C_{dbM2}	$9.2\ 10^{-11}$	$8.92\ 10^{-5}$	60 fF
C_{sbM2}	$9.2\ 10^{-11}$	$8.92\ 10^{-5}$	0 [z]
C_{dbM3}	$2.3\ 10^{-11}$	$2.46\ 10^{-5}$	15 fF
C_{sbM5}	$6.2\ 10^{-11}$	$6.24\ 10^{-5}$	40 fF
C_{sbMb4}	$1.38\ 10^{-10}$	$1.292\ 10^{-4}$	90 fF

Table (app) 4. Drain or source to bulk capacitances of MOS transistors in FDOA.

A.3.4 Input capacitances (C_π) of bipolar transistors

C_π is composed by the base-charging capacitance C_b and the emitter-base depletion layer capacitance C_{je}.

The base-charging or diffusion capacitance is an apparent input capacitance. The variation in v_{BE} causes a variation of the injected charge Q_F in the base which is accumulated in the base and then diffuses to the collector [67]. The ratio of the variations has the dimension of a capacitance $C_b = \frac{dQ_F}{dv_{be}} = \frac{dQ_F}{di_c}\frac{di_c}{dv_{be}} = \tau_F g_m$, where i_c is the collector current and τ_F is the base transit time.

The BE junction is forward biased in the operation of the amplifier, therefore C_{je} corresponds to the capacitance of a forward biased PN junction. Using the Gummel-Poon model $C_{je} = CJE_{eff}\left(1 + MJE\frac{vbe}{VJE}\right)$ where $CJE_{eff} = CJE \cdot M \cdot AREA$.

[z] The source of PMOS transistors is connected to the N well.

In Table (app) 5. the input capacitances of relevant transistors in FDOA are computed, using information of [73] and Table (app) 1.

Transistor	C_b [fF]	C_{je} [fF]	C_π [fF]
Q_1	37	28	55
Q_6	12	28	40
Q_8	75	28	100

Table (app) 5. Input capacitances of relevant FDOA bipolar transistors.

A.3.5 Substrate-Collector capacitance of bipolar transistors.

According to [165] substrate-collector depletion capacitance C_{js} for a reverse biased junction (always for substrate) can be computed as $C_{js} = CJS_{eff}\left(1-\frac{vsc}{VJS}\right)^{-MJS}$ where $CJS_{eff} = CJS \cdot M \cdot AREA$.

In Table (app) 6. the collector to substrate capacitances of relevant transistors in FDOA are computed, using information of [73] and Table (app) 1.

Transistor	v_{sc} [V]	C_{js} [fF]
Q_1	-2.2	60
Q_6	-2.5	55
Q_7	-2.5	55

Table (app) 6. Collector to substrate capacitances of relevant FDOA bipolar transistors.

A.3.6 Base-Collector depletion capacitance of bipolar transistors.

According to [165] the base-collector depletion capacitance C_{jc} for a reverse biased junction (transistor in active region) can be computed as $C_{jc} = XCJC \cdot CJC_{eff}\left(1-\frac{vbc}{VJC}\right)^{-MJC}$ where $CJC_{eff} = CJC \cdot M \cdot AREA$, with M = 2, AREA = 3, using information of [73], then CJC_{eff} = 66 fF and C_{jc} = 12 fF.

In Table (app) 7. the base-collector capacitances of relevant transistors in FDOA are computed, using information of [73] and Table (app) 1.

Transistor	v_{bc} [V]	C_{js} [fF]
Q_6	-1	15
Q_7	-1.8	10

Table (app) 7. Base-collector capacitances of relevant FDOA bipolar transistors.

B Appendix: Common-mode range of different configurations of differential pair with emitter degeneration.

The classical configuration for an emitter-coupled pair with emitter degeneration resistor R_E is shown in Figure (app) 1.

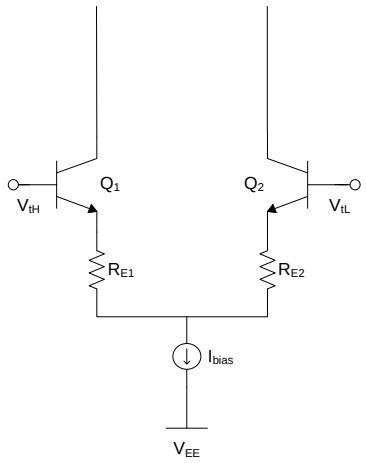

Figure (app) 1. Classic emitter resistor and power supply configuration.

The minimum level of an input signal V_{iMIN} is given by the minimum voltage drop required by the bias current source $V_{Ibias(MIN)}$,

$$V_{iMIN} \geq V_{be\_Qi(ON)} + I_{e_{Qi}} R_{E_i} + V_{Ibias(MIN)} + V_{EE} \qquad \text{(B.1)}$$

The required input DM signal range is V_{iDMAX}, therefore constraints given by (B.1) will apply on the input CM range. Then, and approximating the emitter current by the collector current ($\alpha \approx 1$), the minimum input CM for any input (V_{iCMIN}) is

$$V_{iCMIN} \geq V_{be\_Qi(ON)} + I_{c_{Qi}}\Big|_{V_{iDMAX}} R_{E_i} + V_{Ibias(MIN)} + V_{EE} + \frac{V_{iDMAX}}{2} \qquad \text{(B.2)}$$

For a fully balanced circuit, only the DM component of the collector current changes as function to V_{iD} (for $V_{iD}<0$):

$$I_{c_{Qi}} = \frac{I_{bias}}{2} - \frac{\Delta I}{2} \qquad \text{(B.3)}$$

It can be shown (see 4.2.3.1) that,

$$V_{iD} = R_E \Delta I + V_T \ln\left(\frac{I_{c_{Q1}}}{I_{c_{Q2}}}\right) \qquad \text{(B.4)}$$

where $\Delta I = I_{cQ1} - I_{cQ2}$ and $R_E = R_{E1} = R_{E2}$. Neglecting the non-linear term in (B.4) for typical operation ($\Delta I \ll I_{bias}$), and combining previous expressions we obtain the CM input range for the classical configuration:

$$V_{iCMIN\_CLASSIC} \geq V_{be\_Qi(ON)} + \frac{I_{bias}}{2} R_{E_i} + V_{Ibias(MIN)} + V_{EE} \qquad \text{(B.5)}$$

Figure (app) 2 shows an improved input CM range configuration for a differential pair with emitter degeneration. The current source is split into two current sources of half value comparing to classical configuration. The value of the emitter resistor is twice the previous one (drawn here as two resistor in series R_{E1}=R_{E2}= R_E of the same value R_{E1}=R_{E2}= R_E for convenience).

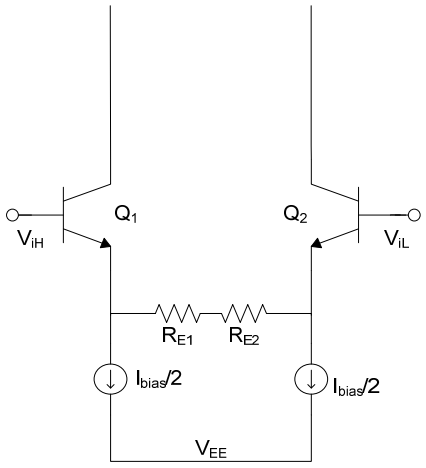

Figure (app) 2. Improved input CM range configuration for a differential pair with emitter degeneration.

In this case the minimum level of an input signal V_{iMIN},

$$V_{iMIN} \geq V_{be\_Qi(ON)} + V_{Ibias(MIN)} + V_{EE} \qquad \text{(B.6)}$$

Then,

$$V_{iCMIN\_IMPROVED} \geq V_{be\_Qi(ON)} + V_{Ibias(MIN)} + V_{EE} + \frac{V_{iDMAX}}{2} \qquad \text{(B.7)}$$

According to expressions (B.5) and (B.7) the lower limit forV_{iC} of the improved configuration is smaller, closer to V_{EE}, than the classical one if $\frac{I_{bias}}{2} R_{E_i} \geq \frac{V_{iDMAX}}{2}$. This should be the case, since the DM input range in both configuration introduce this constraint.

C Appendix: Measurement of parasitic capacitance at the ASIC input

Figure (app) 3 shows the circuit to make the measurement. A current pulse is injected using a step function with fast rise time. The decay time constant τ_C of the pulse is τ_C=Rpmt*(Cpar+Cac+Cprobe)), neglecting the effect of the small source resistance of the pulse generator.

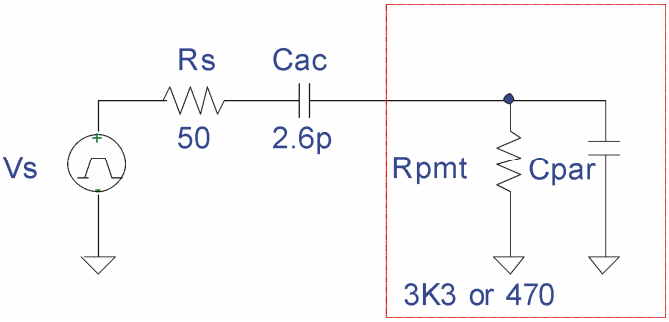

Figure (app) 3. Circuit to measure the input capacitance.

We need to estimate parasitic capacitances (Cpar). We replace the usual PMT load (470 Ω) by a higher resistor (3K3 Ω) for better resolution. The resulting time constant τ_C is 62ns, as shown in Figure (app) 4. The active probe parasitic capacitance is 3pF. The capacitance seen at the VFE input (PMT output) is around 12.4 pF. The τ_C of the input will be 6 ns for a 470 Ω PMT load

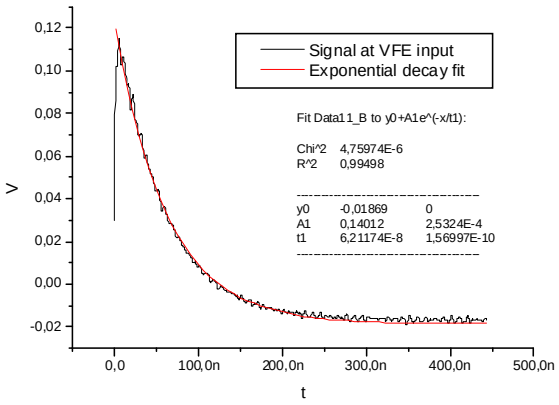

Figure (app) 4. Decay time constant τ_C.